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# Flex-PCB board design for SiPM readout at cryogenic temperatures

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During the High-Luminosity LHC phase, the LHCb RICH detector will face challenges arising from increased particle multiplicity and high occupancy. Therefore, enhancing the detector granularity and introducing sub-100ps time information will be crucial to maintaining its excellent particle identification (PID) performance. The 150 ps intrinsic time resolution of the Multi-Anode Photomultiplier Tubes (MAPMTs), currently installed in the detector, will not be sufficient during LHC Run 5. Consequently, the LHCb RICH collaboration is exploring new photodetector options with improved timing and smaller pixel sizes. A strong candidate is the silicon photomultiplier (SiPM). However, radiation damage to SiPMs poses a significant challenge, necessitating operation at cryogenic temperatures.

This work presents a PCB design for the readout of a Hamamatsu 64-channels SiPM. The PCB is a 3-layer fully flexible board that will be integrated into a liquid-nitrogen cryostat demonstrator, currently under development at CERN. The board employs high-density long traces to separate the SiPM (to be cooled at cryogenic temperatures) from the readout electronics (operating at room temperature). The aim is to prove the principle of a small-scale SiPM module at cryogenic temperatures with flex-PCB technology to bring the signals to the front-end readout electronics at higher temperatures. The high-density traces (with 200 $\mu$m of width and spacing) have been designed to match the requirements to scale the prototype to the RICH detector dimensions. Furthermore, the board implements features to ensure compatibility with the RICH upgrade readout electronics and its integration into the cryostat. The overall thickness of the board is 450 $\mu$m, with a stack-up designed to match 50-100 $\Omega$ impedance. The SiPM bias has negative polarity with an RC-filter per channel for decoupling purposes. The board implements two pulse injection circuits: one near the SiPM and one at the front-end connectors. These circuits will be used to evaluate the difference in signal integrity between a long and a short trace. Then, the board will be coupled to the RICH testbeam electronic chain, a FastIC+picoTDC-based readout, and tested in a picosecond pulsed laser setup. The time resolution and signal integrity of the SiPM pulses will be measured, first at room temperature and then in a cold chamber at -20$^{o}$C. Finally, the PCB will be integrated into the cryostat demonstrator, anticipated for the second half of 2025.

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