ALICE ITS3 WAFER-SCALE ON-CHIP READOUT ARCHITECTURE

Manuel Viqueira Rodriguez

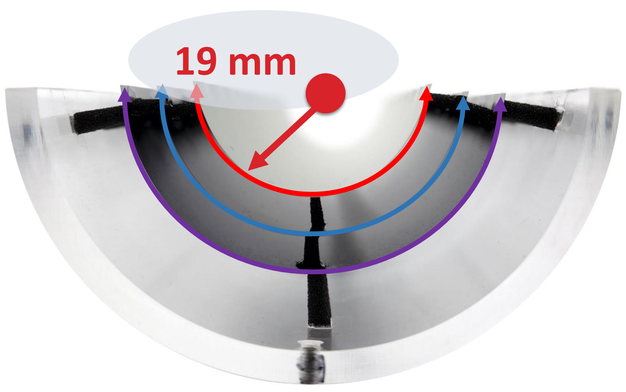
INTRODUCTION

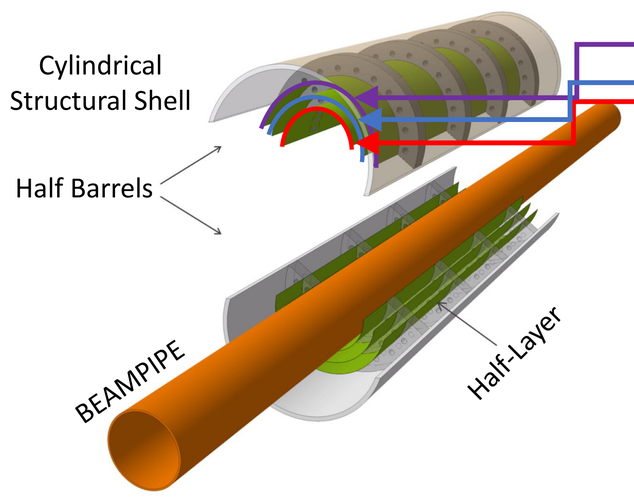
- **The ITS3** is a novel monolithic pixel detector that replaces the **3 innermost layers** of the ALICE tracking system at LHC.
- Each half-layer of ITS3 consists of a single large monolithic pixel sensor curved to a **cylindrical shape**.

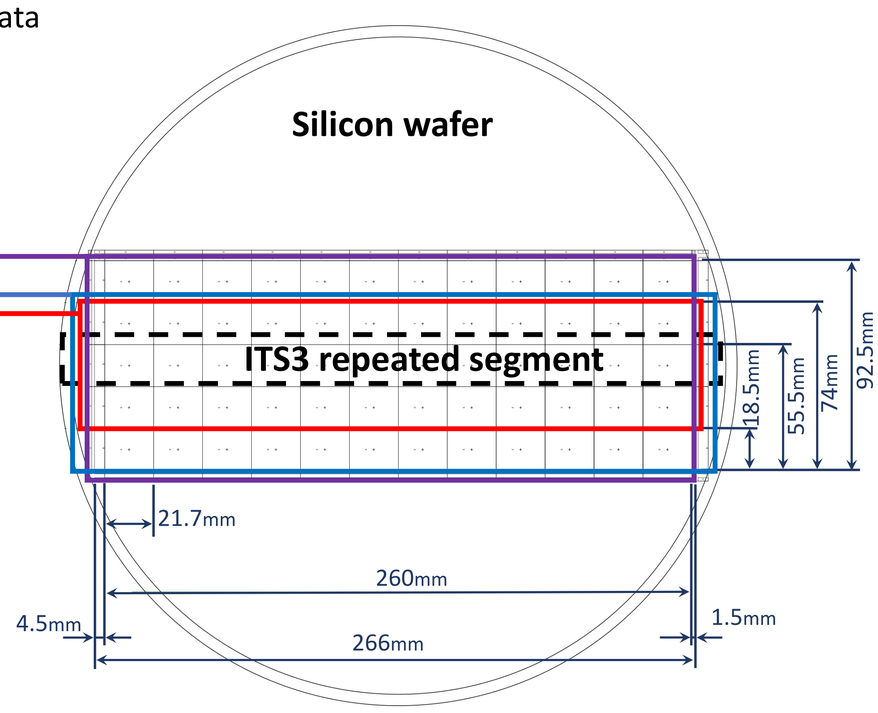
- **Objective**
  - Lower detector material (material thickness of 0.07 %X0 per layer)
  - Place the first layer at **19 mm** from the interaction point

- **Challenges**
  - The design must be **DFM** robust to increase the **yield.**
  - Power budget **<40 mW cm^{-2}**
  - Active area **93%**
  - Particle flux up to **5.75 MHz cm^{-2}** at the center of the chip.
  - Data connection only **on the left side of the chip**. All data must be transferred **on-chip** up to this point.

- **Specific tasks**
  - Elaborate a custom DFM cell library to achieve the yield.
  - Create a model that emulates the on-chip readout architecture to optimize the various design parameters.
  - Create the readout architecture at RTL level.







DFM/LOW-LEAKAGE STANDARD CELLS

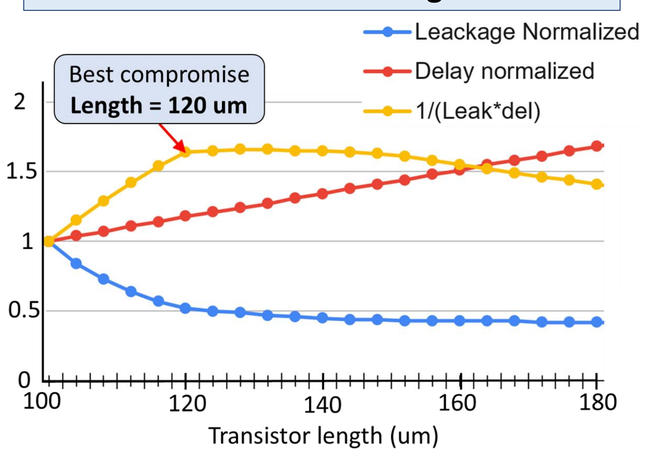
- **<u>Power consumption</u>**

  Leakage current must be reduced minimizing the impact in the cell's delay
  - **Increase gate length**

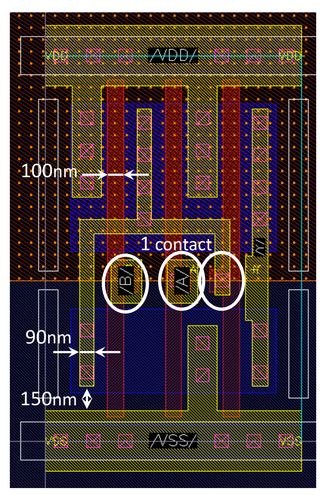
- **<u>Yield (DFM)</u>**

  Large area = Highest chances of manufacturing defects. A custom standard cells library with a robust Design For Manufacturing (DFM) was designed.
  - **Increase the number of vias**
  - **Increase metal spacing**
  - **Increase metal width**

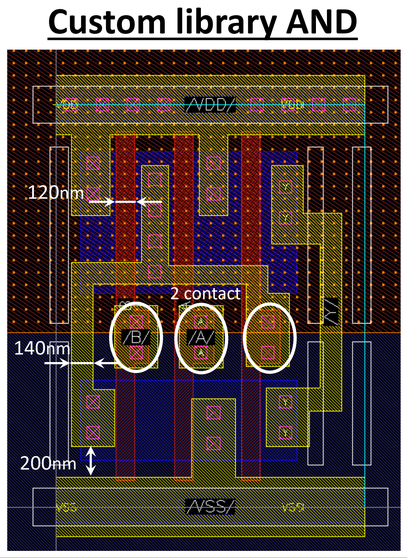
Normalized leakage current and delay over transistor length



<u>Foundry library AND</u>

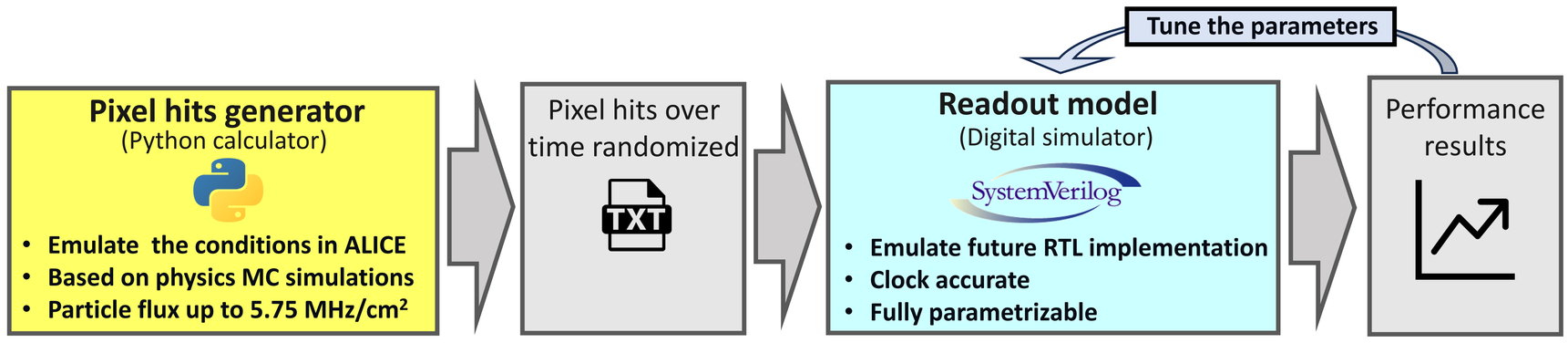


<u>Custom library AND</u>



ITS3 BEHAVIORAL MODEL

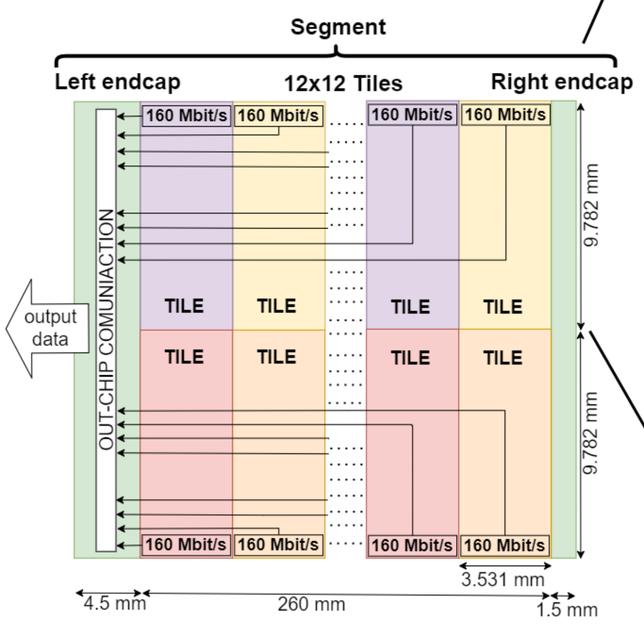
- Before the design of the ITS3, its resources and parameters **tradeoffs must be calculated:**
  - **General architecture**
  - **Number of divisions of the matrix**
  - **Number of FIFOs and depth**
  - **Number of links and speed**



ITS3 ON-CHIP READOUT ARCHITECTURE

ITS3 on-chip readout architecture:

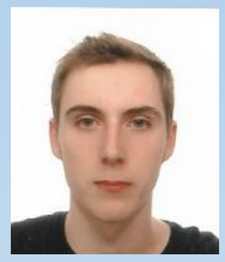
- **Chip segmentation:** Division in Tiles with independent readout links.
- **Global shutter:** The detected pixel hits are transmitted in time-stamped packets.
- **2 in-pixel registers:** Alternate the integration of the pixel hits and the readout to the FIFOs.
- **Sequential FIFO read:** FIFOs are processed in order.



REFERENCES

1) The ALICE Collaborator, "Technical Design report for the ALICE Inner Tracking System 3 - ITS3 ; A bent wafer-scale monolithic pixel detector", CERN-LHCC-2024-003 ; LHCC-I-03.

2) A. Szczepankiewicz *et al*. "Readout of the upgraded ALICE-ITS", ELSEVIER, Nucl. Meth A Volume 824, 11 July 2016, Pages 465-469.



Manuel Viqueira Rodriguez
PhD student at EP-ESE-FE
manuel.viqueira.rodriguez@cern.ch
CERN phone: 69169
Office: 14/4-22