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ALICE ITS3 WAFER-SCALE ON-CHIP READOUT ARCHITECTURE

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The ALICE collaboration is developing the new Inner Tracker System 3, a novel detector that uses the stitching technique to construct a single-die monolithic active pixel sensor. For material budget, flexible cables are minimized. This forces all the data to be transferred on-chip to the left edge, responsible for communication with the outside world. These long-distance on-chip communication links require careful optimization of throughput, area, and power consumption. Additionally, the yield must be contained.

To achieve this on-chip readout architecture, the following tasks were performed and will be presented in this contribution:
- Design of a custom DFM standard cells library to achieve the yield.
- Model of the on-chip readout architecture to optimize the various design parameters.
- Create the readout architecture at RTL level.

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