SOCRATES: a Radiation-Tolerant SoC Generator Framework

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Marco Andorno, Alessandro Caratelli, Davide Ceresa, Benoît Denkinger, Kostas Kloukinas, Anvesh Nookala, Risto Pejašinović

Introduction

As **front-end ASIC complexity** in HEP experiments grows, there is a shift towards more **modular, programmable, and cost-effective designs**. This work introduces the **SOCRATES** platform, a radiation-tolerant SoC generator toolset, centered on **SoCMake**, a hardware/software build system that **automates SoC assembly and verification**.

Utilizing existing IP blocks, SoCMake generates the interconnects and the software framework to run application code. The platform includes **radiation-tolerant IPs** and supports **fault-tolerant extensions** for redundancy and error correction in view of harsh operating conditions at HEP experiments.

A **prototype ASIC** based on the **RISC-V Ibex processor**, created using SOCRATES in a 28nm CMOS process, is going to validate the toolset through SEE and TID testing.

Programmability for future on-detector ASICs

- Allows retargeting of ASICs for different applications
- Re-program algorithms at runtime

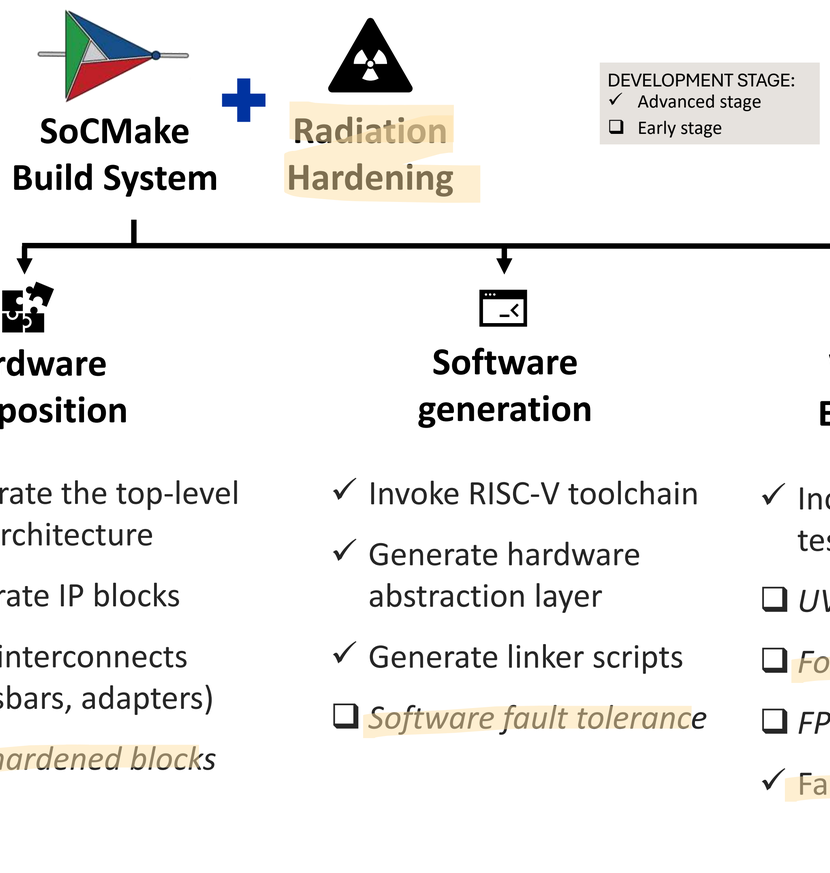
Simpler system integration and shorter design time

- Introduce modularity with self-contained blocks
- Accelerate digital design and verification
- Accelerate physical implementation

RadTol Digital IP-block library

- Encourage design re-use within the community
- All IPs are coherent with a standardized interconnect
- Pre-verified building blocks

Platform description



- ✓ Generate the top-level SoC architecture
- ✓ Integrate IP blocks
- ✓ Infer interconnects (crossbars, adapters)
- ❑ *Rad-hardened blocks*

- ✓ Invoke RISC-V toolchain
- ✓ Generate hardware abstraction layer
- ✓ Generate linker scripts
- ❑ *Software fault tolerance*

- ✓ Include functional testing environment
- ❑ *UVM environment*
- ❑ *Formal verification for TMR*
- ❑ *FPGA prototyping*
- ✓ Fault injection framework

SOC RAdiation Tolerant Eco-System

SOCRATES provides a complete toolset for the generation of radiation-tolerant System-on-Chip (SoC) designs.

The project aims to enable **design reusability and modularity** by minimizing the amount of manually-written RTL code and promoting the reuse of qualified IP blocks, thus greatly reducing design and verification turnaround time and cost.

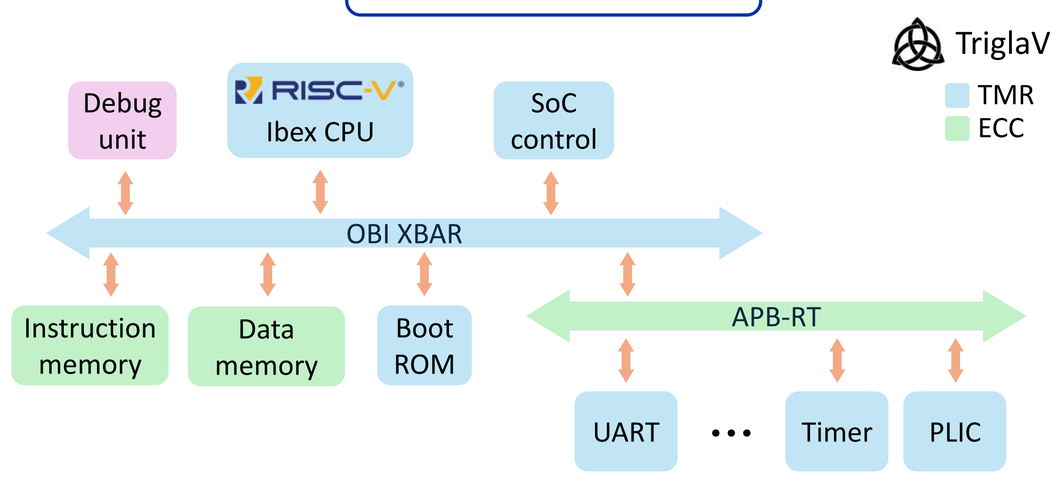
By making used of a **custom build system**, the SOCRATES platform aims at being a fully integrated environment for the generation and customization of SoC designs, from the **hardware components**, to the **software toolchains**, to **functional verification**.

Radiation tolerance is provided by **extensions** that introduce **TMR** (Triple Modular Redundancy) and **ECC** (Error-Correcting Code). Each peripheral register block is generated with embedded TMR, the peripheral interconnect bus is automatically instantiated and consists of an AMBA APB protocol extended with ECC (**APB-RT**).

Build system

At the heart of the SOCRATES platform is SoCMake, a **CMake-based build system** with custom extensions targeted at **hardware/software co-design**. Starting from a **SystemRDL description**, along with the RTL of the CPU core, memories, peripherals, and any other custom logic, SoCMake calls different tools to **generate the RTL of the whole SoC**, the **Hardware Abstraction Layer** (HAL) for the peripherals, the **linker script** for application mapping and the **documentation**.

Demonstrator ASIC



To **validate this toolset** and **test the radiation performance** of the resulting design, a **demonstrator chip** is being developed in a commercial 28nm bulk CMOS technology. This SoC is generated using the SOCRATES platform and it's based around Ibex, an open-source RISC-V processor core. A minimum set of peripherals is included, while maintaining a focus on introducing **observability and testability features** to evaluate the radiation tolerance of the design under irradiation testing.

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