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MiniMALTA3 DMAPS

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MALTA3 DMAPS, last prototype of MALTA family, will be designed in the standard TOWER 180 nm technology with numerous process modifications, as well as front-end changes in order to boost the charge collection efficiency after the targeted fluence of 1 × 10E15 1 MeV neq/cm 2.
The effectiveness of these changes have been demonstrated with recent measurements of the full size MALTA2 chip. With the original MALTA concept being fully asynchronous, a small-scale MiniMALTA demonstrator chip has been developed with the intention of bridging the gap between the asynchronous pixel matrix, and the synchronous DAQ. This readout architecture will serve as a baseline for MALTA3, with focus on improved timing performance. The synchronization memory has been upgraded to allow clock speeds of up to 1.28 GHz, generated by a PLL pushing the technology to its limit, with the goal of achieving a sub-nanosecond on-chip timing resolution.
The data output protocol will be upgrated with analysed data serialization discussed in the context of the overall sensor architecture.

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