# Radiation Hardness of Silicon Detectors

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# Plan for the lectures

- Brief introduction
- Displacement damage
- Surface damage

The material used to prepare the lectures is referenced to in the slides.

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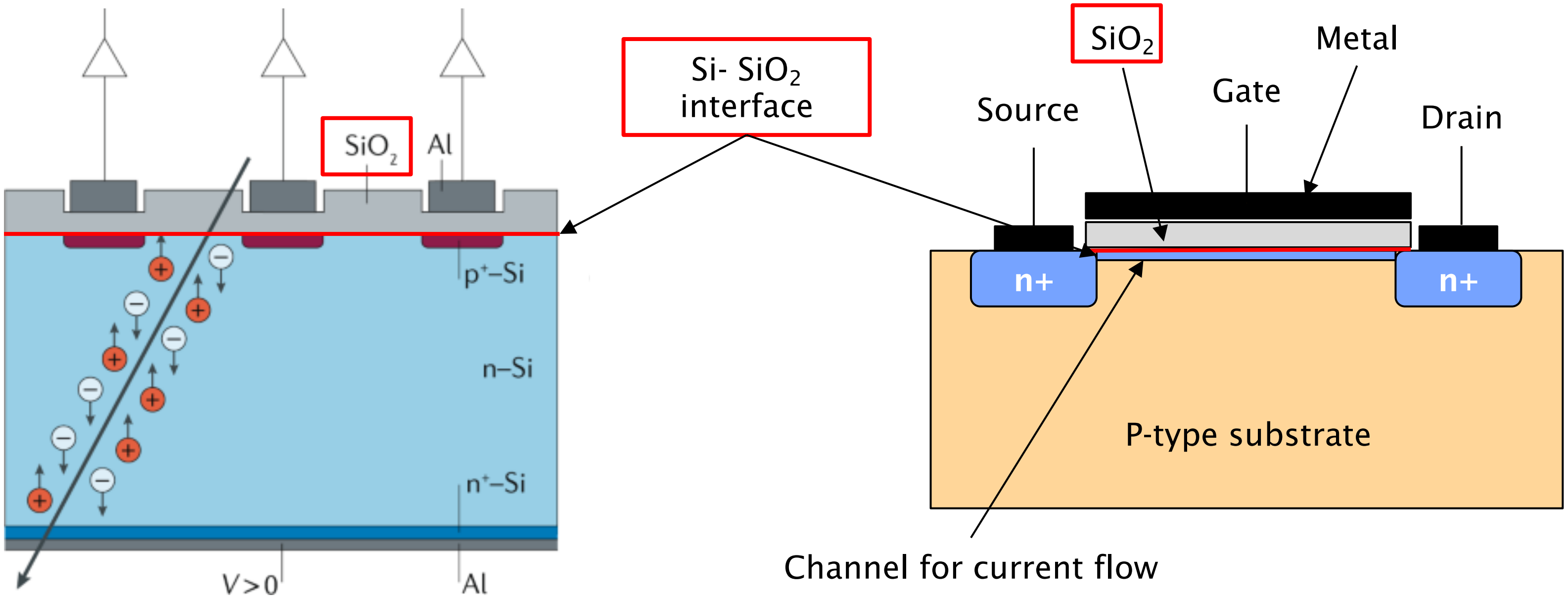
# Plan for the lectures

- Brief introduction
- Displacement damage
- **Surface damage**

# Surface damage

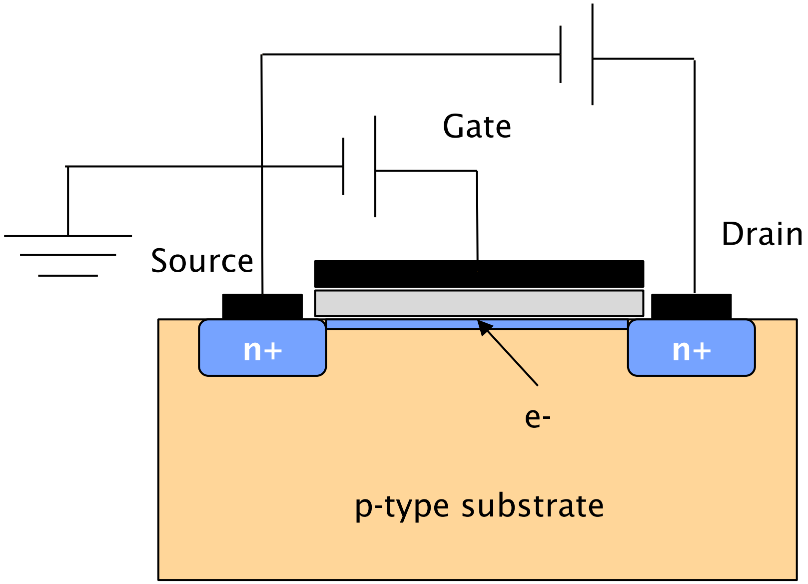
- Damage to the surface of silicon sensors and electronics, especially in the $SiO_2$ layer and at the $Si$-$SiO_2$ interface.
- $SiO_2$ is used as:
  - Passivation layer on silicon sensor.
  - Gate Oxide in MOSFET transistors.
  - Shallow Trench Isolation (STI) between transistors.
- Surface damage affects mostly electronics.



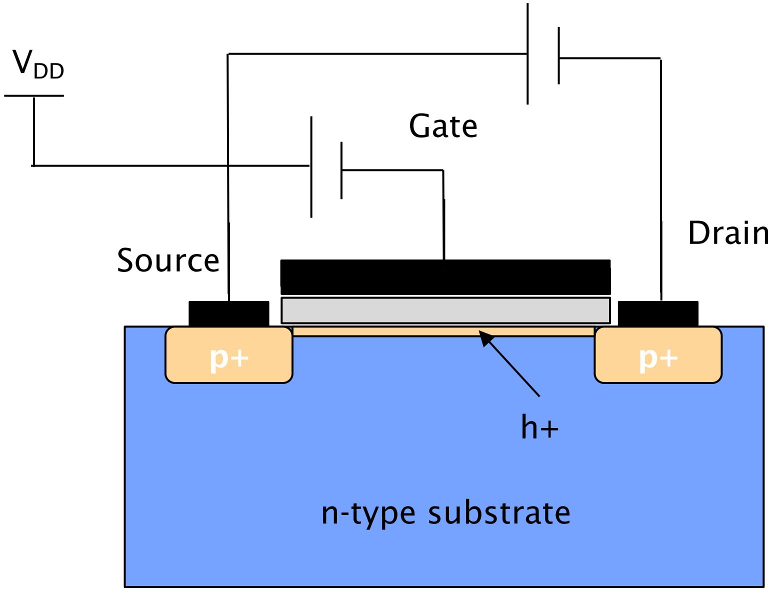
# MOSFET transistors basics

1. A voltage is applied to the gate to induce a channel of free charge carriers below the Si-SiO2 interface.
2. By applying a voltage on the drain, carriers can move → current.

- NMOS transistor:
  - $V_{GS} > 0$.
  - Electrons in the conduction channel.

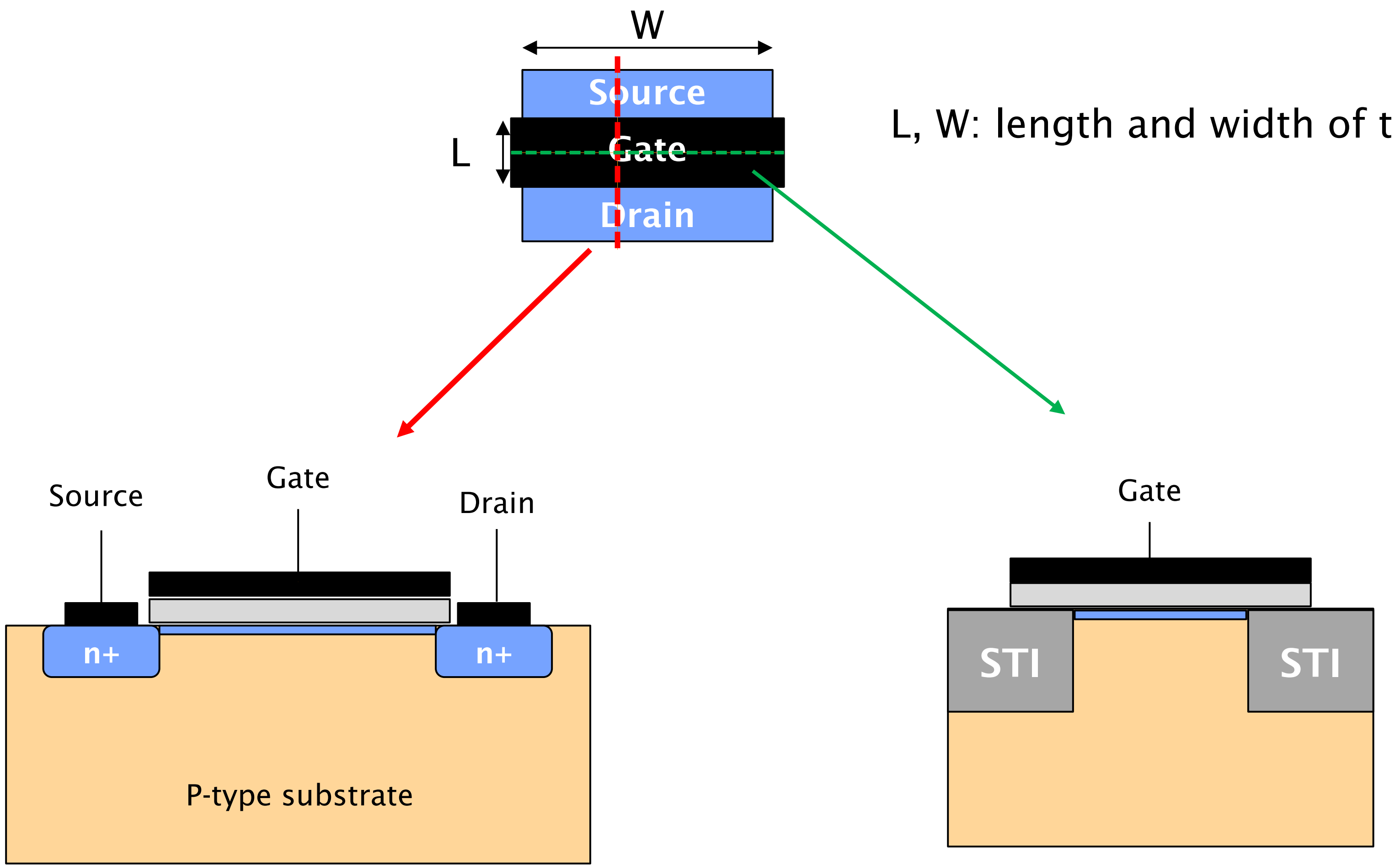


- PMOS transistor:
  - $V_{GS} < 0$.
  - Holes in the conduction channel.



# Other transistor views

View from the top



L, W: length and width of the channel

Shallow Trench Isolation (STI)

# Damage to $SiO_2$

- Radiation causes ionisation and/or dislocation of lattice atoms in $SiO_2$.

- Damage impact from ionisation is more severe in $SiO_2$ → it creates charged defect states in the oxide and at the interface with the silicon that impact transistor's operational parameters.
  - High electric fields can exist in the oxide of MOS transistors.
  - Charge carriers generated by ionisation are separated.
  - Holes have a mobility $10^6$ times lower than electron mobility in $SiO_2$ (large hole capture cross section by shallow levels in the silicon oxide).

- NIEL damage does not get electrically active in the $SiO_2$.
  - Also, the substrate of integrated circuits is highly doped (i.e. low resistivity) which reduces the sensitivity to displacement damage.

# Defects in $SiO_2$ and Si-$SiO_2$ interface

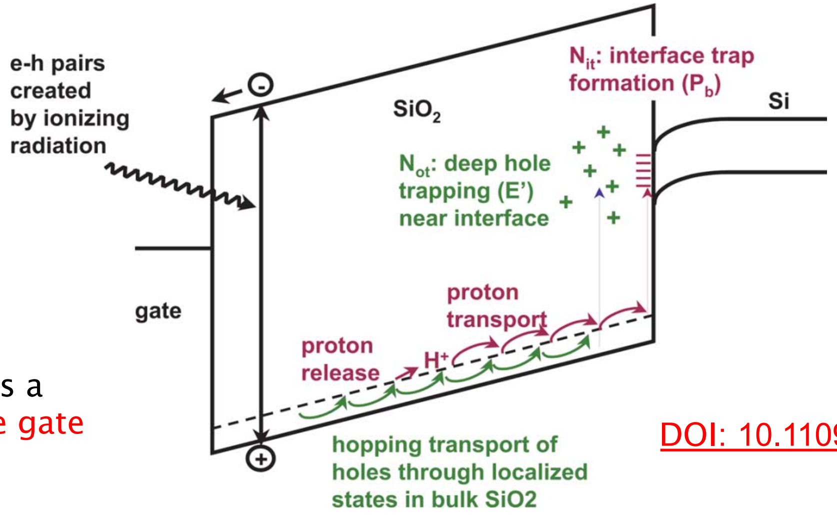
- Defects are present in the $SiO_2$ and at the Si-$SiO_2$ interface that introduce localised energy states in the bandgap of the material and act as traps for charge carriers.

- In the $SiO_2$ defects are due to a precursor that is not active in its normal condition but is activated by radiation and becomes a trap for positive charges.
  - This precursor is the physical origin of oxide traps.
  - Oxide traps are donor like, i.e. positive.

- At the Si-$SiO_2$ interface defects are due to the abrupt transition between a crystalline material (Si) and an amorphous one ($SiO_2$) that interrupts the crystalline structure of silicon.
  - Interface states are located at the interface or a few angstrom from it.
  - Responsible for interface traps.
  - Interface traps can be both donor or acceptor like, i.e. their net charge will positive or negative according their position wrt. the Fermi level.

# Oxide charges

- The incoming radiation generates e-/h+ pairs.
- After a few ps a fraction of the e-/h+ pair has recombined, the other pairs are separated by the E-field and start to drift in opposite directions.
  - The fraction of non-recombined pairs depends on the type of incident radiation, material, and applied electric field.
- Assuming a positive voltage on the gate.
  - The e- drift to the gate and exit the oxide in a few ps (higher mobility).
  - The h+ will drift (slowly) towards the Si-$SiO_2$ interface.

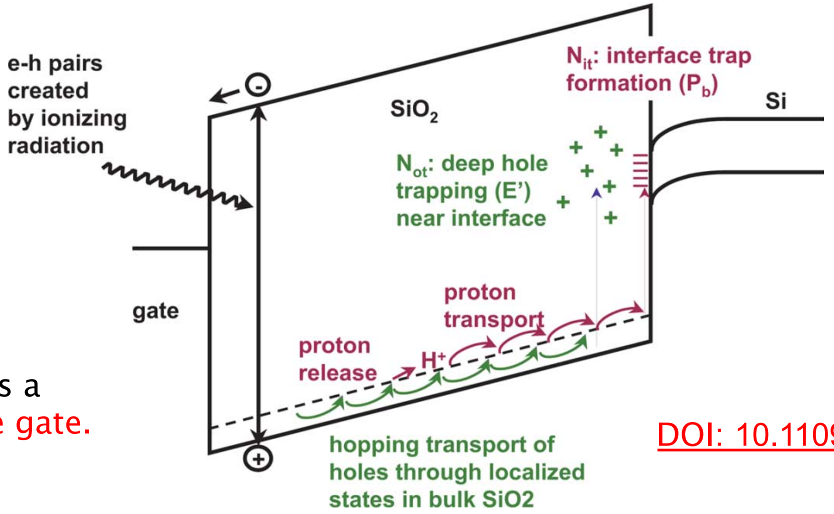


This figure assumes a positive bias on the gate (worse condition).

DOI: 10.1109/TNS.2008.2001040

# Oxide charges

- The h+ move with a dispersive transport phenomena called “polaron hopping”.
  - Being slow h+ are self-trapped, i.e. they are localised in the lattice distortion that they generate → polaron.
  - The polaron moves by hopping from one lattice location to the next → increased holes effective mass, lower mobility.
  - Higher T and E field = faster transport.
  - Dependent on oxide thickness.
  - Long time scales compared to the charge injection.



This figure assumes a positive bias on the gate.

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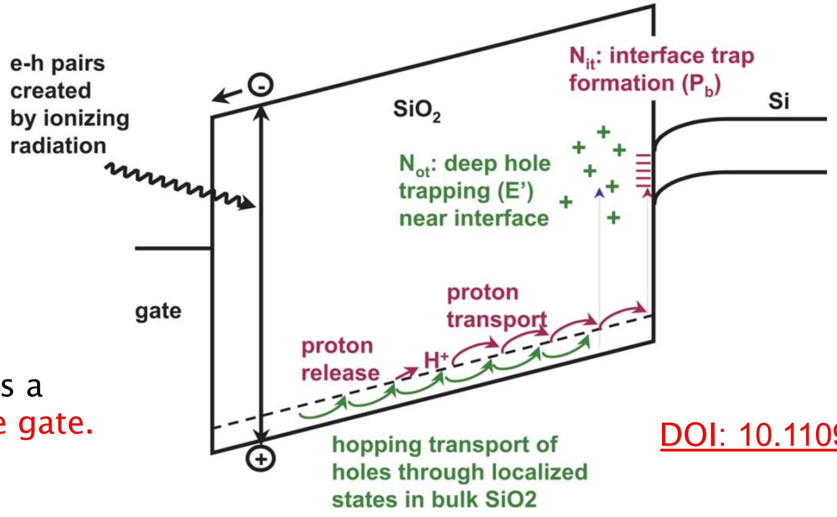
# Oxide charges

- The h+ can be trapped in defects presents in the $SiO_2$ and in oxygen vacancies close to the interface (deep hole trapping) giving origin to a fixed positive charge.
  - The fraction of trapped holes depends on the mean trap density, their hole capture cross-section, and the width of their distribution.



This figure assumes a positive bias on the gate.

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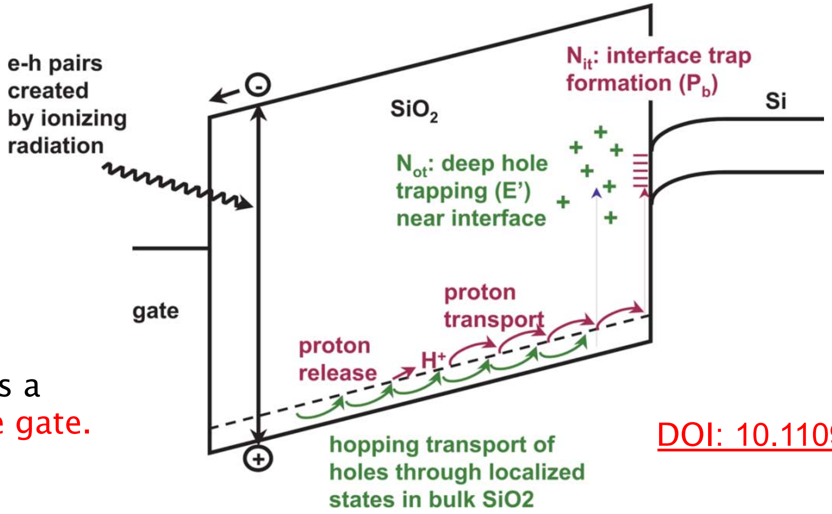
# Interface states

- Because of irradiation, the density of interface traps increases by orders of magnitude.
- Impurity hydrogen ions are released from the lattice by hole hopping.
- These ions move toward the Si-$SiO_2$ interface where they give origin to new interface states that serve as traps.
- Creation of interface states is a slower process than oxide charge formation due to the lower mobility of the hydrogen ions.



This figure assumes a positive bias on the gate.

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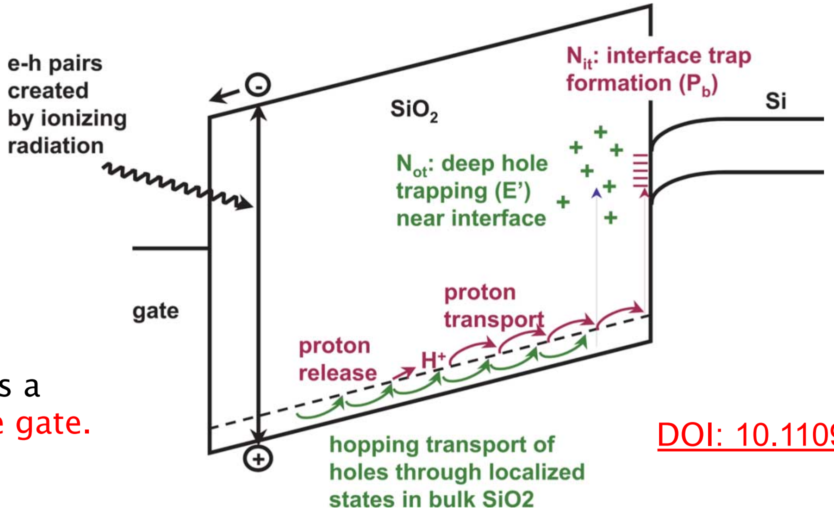
# Interface states

- The radiation-induced traps have energy levels in the bandgap.
  - Traps above midgap = acceptors.
  - Traps below midgap = donors.

- For NMOS under positive bias, interface traps are negatively charged.
- For PMOS under negative bias, interface traps are positively charged.



This figure assumes a positive bias on the gate.

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# Annealing

- Annealing happens through two mechanisms whereby electrons recombine with the trapped holes.

- Electron tunnelling from the silicon to the oxide traps.
  - Strongly dependent on the E-field in the oxide and on the spatial distribution of traps, which in turn depends on the fabrication process.

- Thermal emission of electrons from the oxide valence band into the trap levels.
  - Strong dependence on temperature.
  - Traps need to be close to the valence band.

- Annealing can start already during irradiation depending on dose rate, temperature during irradiation, and the electric field in the oxide, but it is a slow process.
  - Complete annealing can take many months.

# TID technology dependence

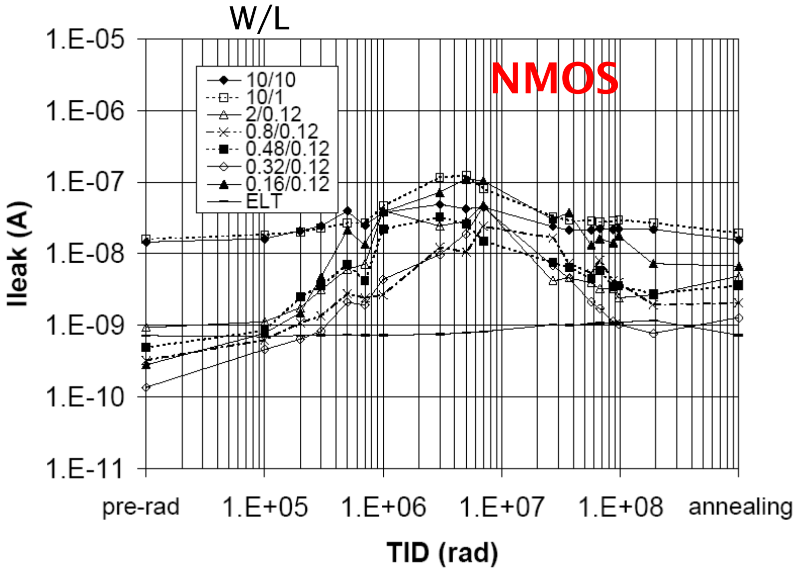
- The scaling of CMOS technologies and reduction of MOSFET gate oxide thickness has greatly improved the radiation hardness of integrated circuits for use at high luminosity experiments.
  - Thick oxides however still exists, e.g shallow trench isolation oxides, field oxides.

- TID damage is greatly influenced by the oxide growth process and the level of initial impurities.
  - Some technologies are more affected than others, even within the same node, i.e. same gate oxide thickness.
  - Even the technology from a specific foundry can have different radiation performance depending on the production sites.

- In the following slides I will discuss TID effects on the 130 nm CMOS technology used for various ATLAS and CMS upgrades.

# Leakage current

- Leakage current in MOSFET transistors is defined as the current that flows through the device for $V_{GS} = 0$.
- A change in leakage current is observed for NMOS transistors.
  - Increase in current up to a TID of a few Mrad, followed by a decrease towards the pre-irradiation value.
  - Peak at a few Mrad.
- No change is observed in PMOS transistors.



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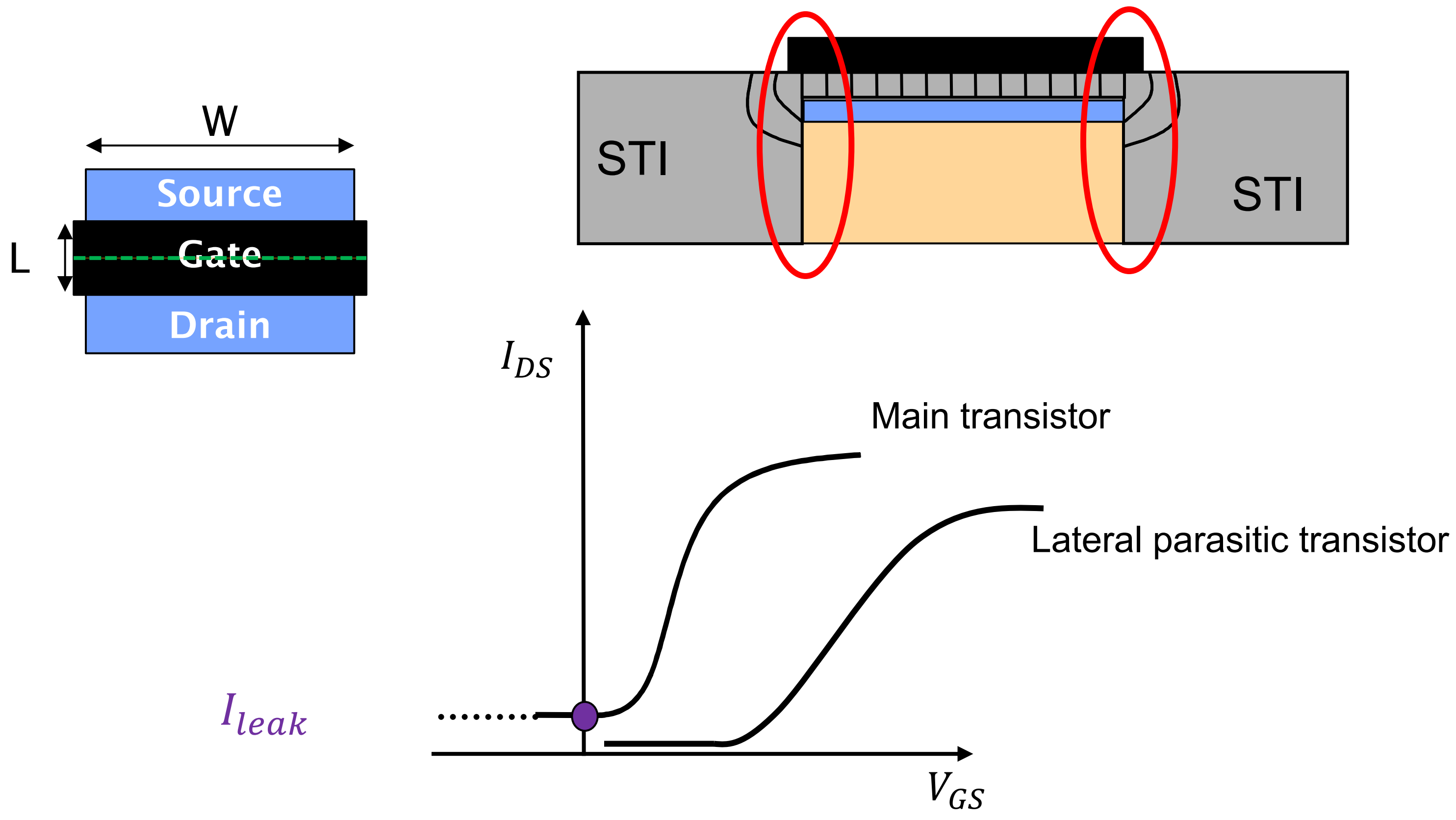
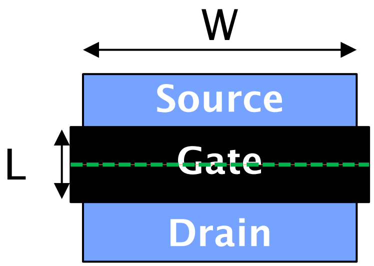
# Edge effects: NMOS

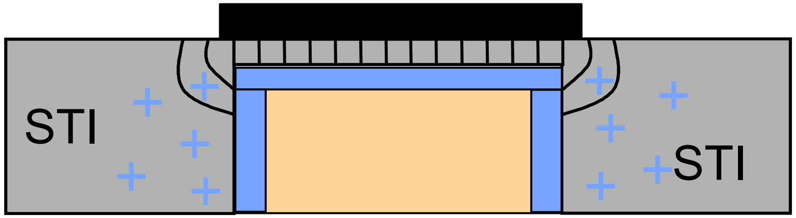
- Parasitic transistors exist at the edges of the transistor.
- Their gate oxide is the STI.

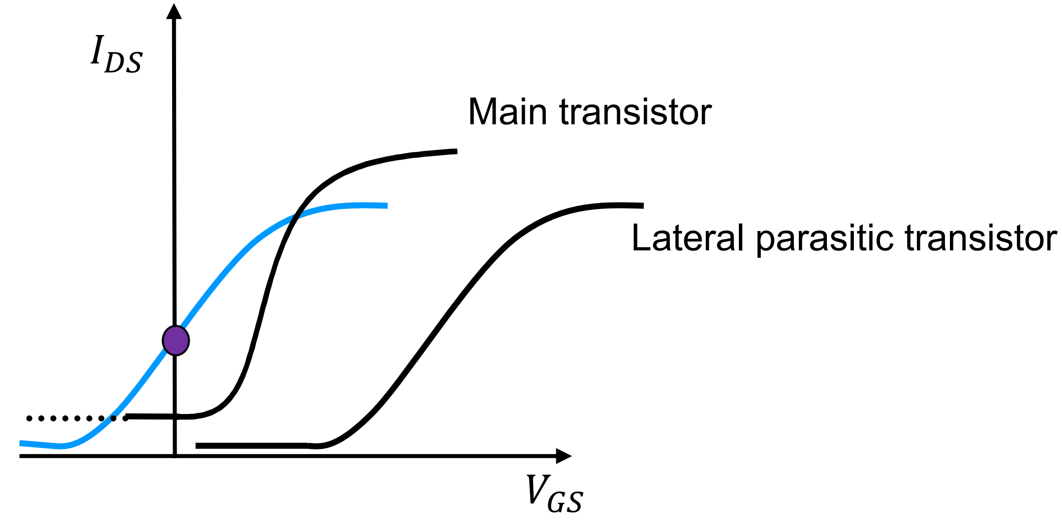


# Edge effects: NMOS

- Positive trapped charges quickly build up in the STI at the edge of the transistor.
- These open a conductive channel through which current can flow between drain and source → parasitic lateral transistor switches on.
- The leakage current increases.

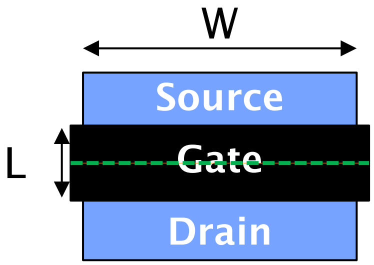


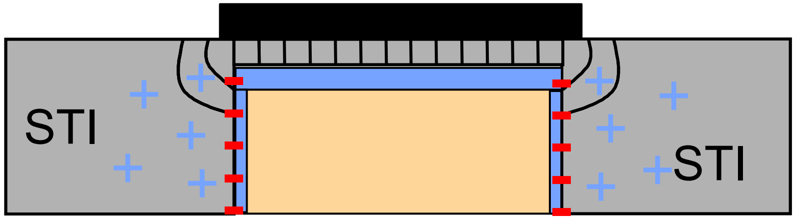


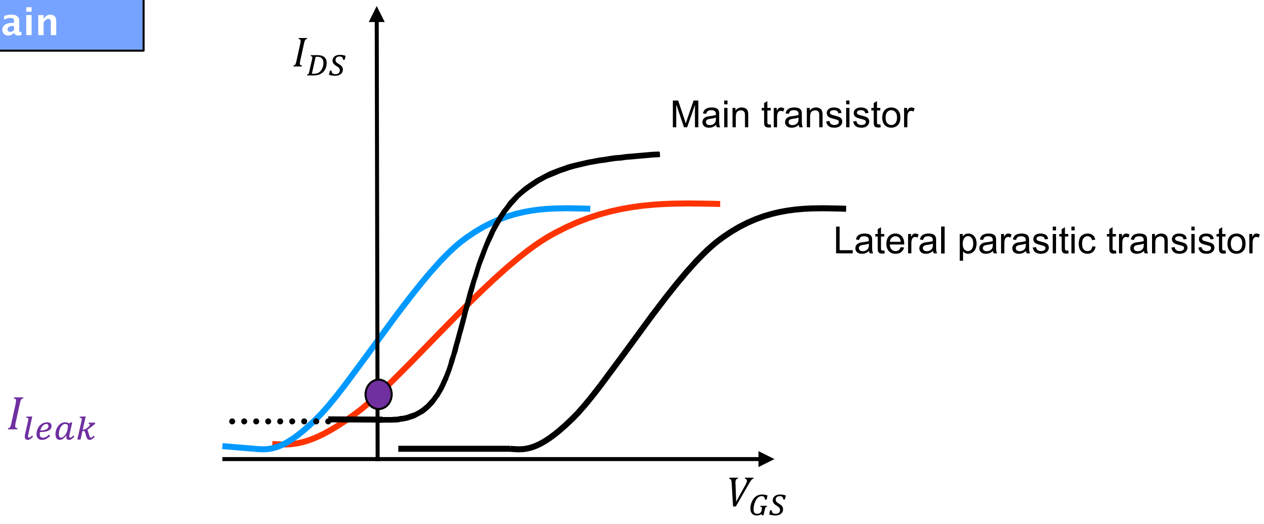


# Edge effects: NMOS

- At higher TID, due to the slower formation process, interface states start to build up.
- These are negatively charged for NMOS transistor and counteract the effect of positive charges trapped in the STI.
- The leakage current decreases.

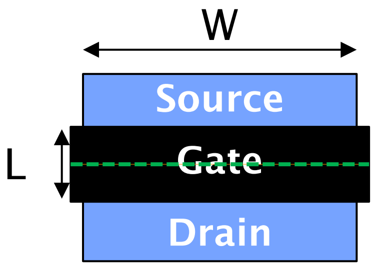


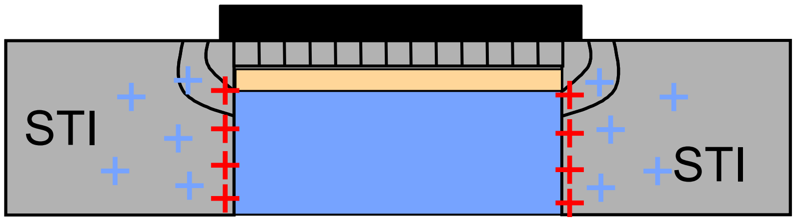


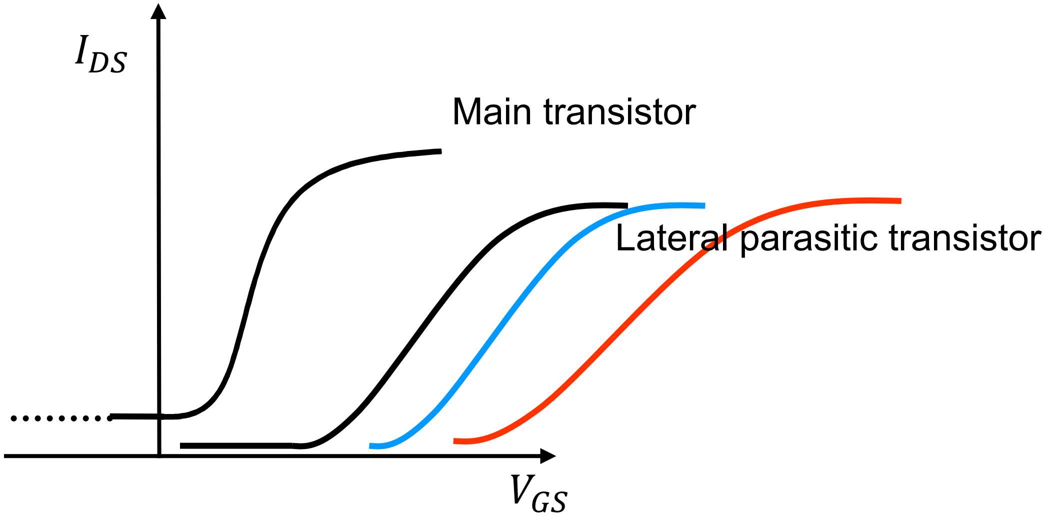


# Edge effects: PMOS

- In PMOS transistors, both oxide charges and interface states are positively charged.
- They repel further the holes from the side of the transistor → the parasitic transistors do not switch on.
- The leakage current does not change.



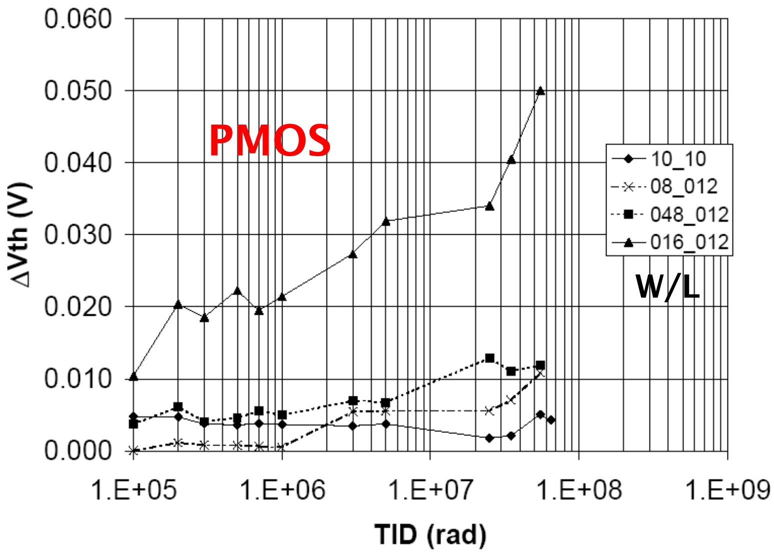


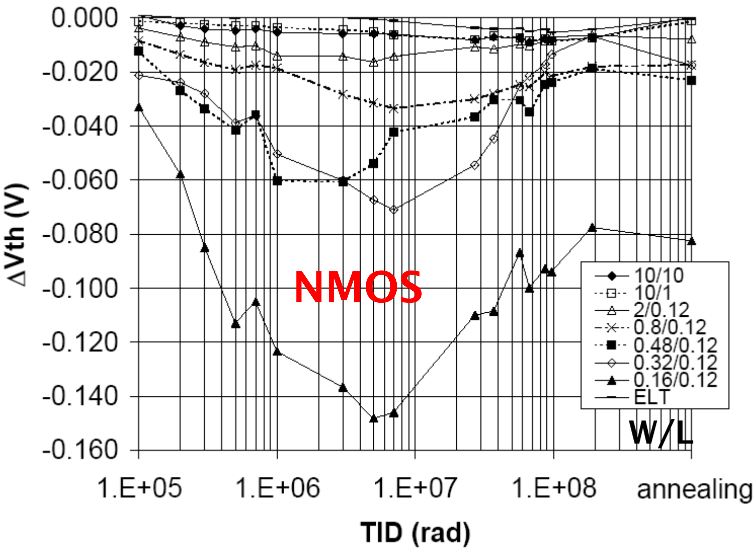


# Threshold voltage shift

- A threshold shift is observed for narrow transistors both NMOS and PMOS.

- For narrow transistors, i.e. small W, the net charge at the transistor edges influences the electric field in the main device → narrow channel effect.
  - Observed in deep-submicron CMOS technologies as a decrease of $V_{th}$ with transistor width.





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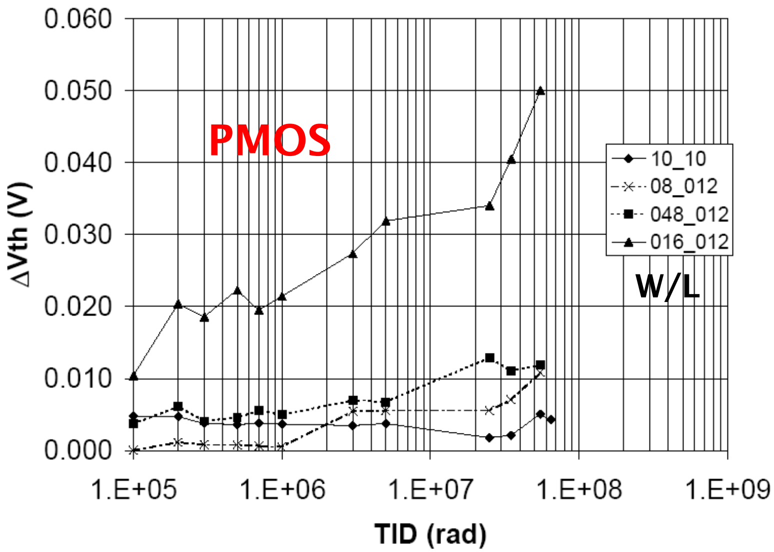
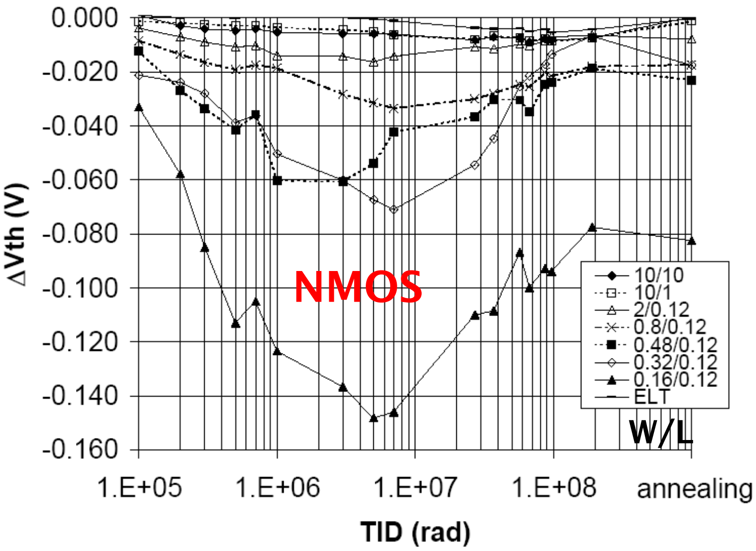
# RINCE

- Due to the positive oxide charge trapped in the STI oxide, the narrow channel effect decreases/increases the $V_{th}$ of NMOS/PMOS transistors.
- For NMOS, the negatively charged interface states counteract the effect of the positive oxide charge → rebound with peak at a few Mrad.
- For PMOS, the positively charged interface states add to the effect of the positive oxide charge → increase of the $V_{th}$ slope.

Radiation Induced Narrow Channel Effect (RINCE)

10.1109/TNS.2005.860698





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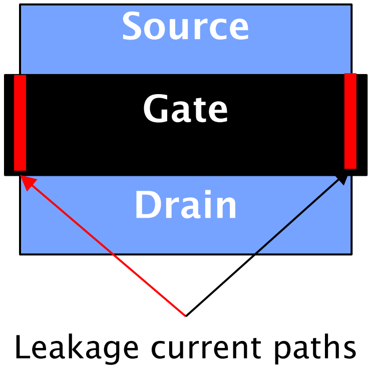
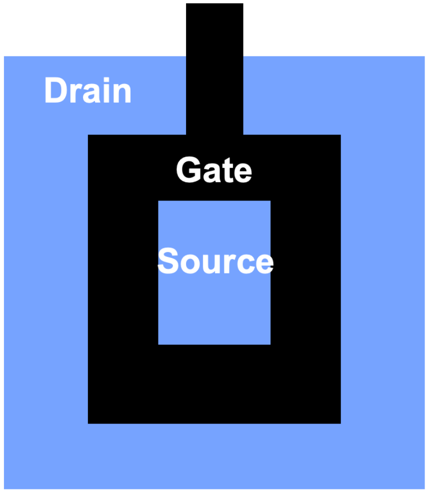
# Hardening by layout techniques

- Enclosed layout transistor can be used to cut leakage current paths at the edge of the transistors.
  - For the same W/L, ELT use more space → Loss of logic density.
  - Only really feasible for the analogue part of the circuit.
  - Lack of a commercial digital library for digital design

Linear transistor layout



Enclosed transistor layout (ELT)

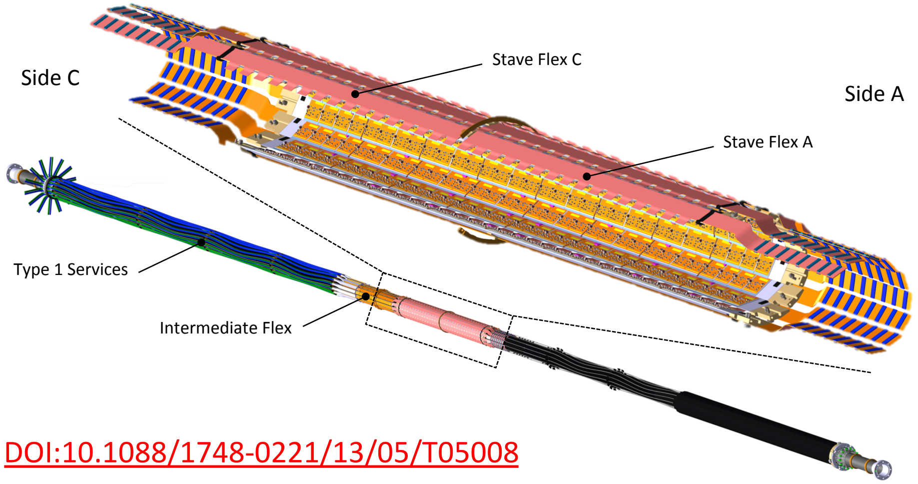


# TID effects on ATLAS IBL operation

- The ATLAS Insertable B-Layer is the innermost layer of the ATLAS tracking system at the LHC.
  - New layer inserted in the ATLAS Inner Detector during the LHS LS1 (2013-14).
  - Closest layer to IP, radius = 33.5 mm (beam pipe r = 23.5 mm).

- The IBL sensors and front-end electronics must cope with radiation doses of $5 \times 10^{15}$ $n_{eq}/cm^2$ NIEL and 250 MRad TID during the LHC Phase-I.

- New front-end chip in 130 nm CMOS technology → FE-I4.



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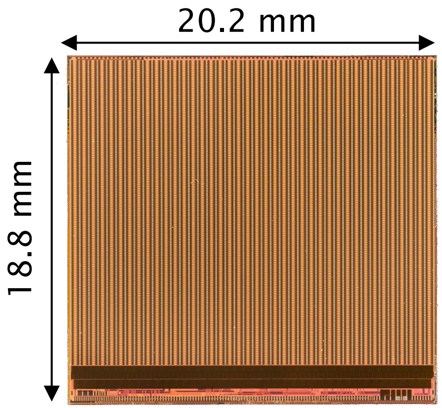
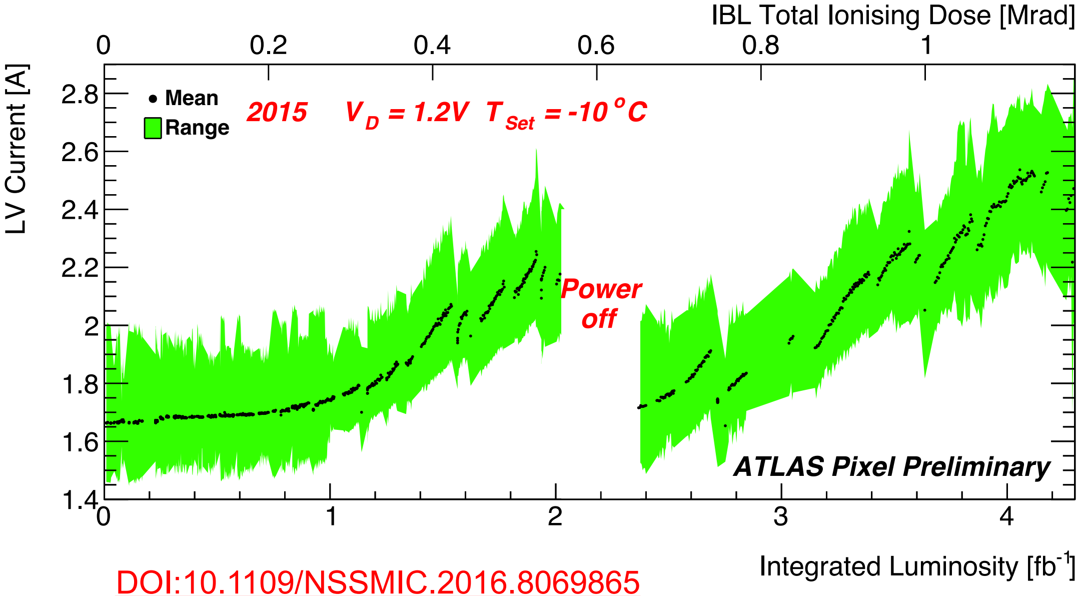


# TID effects on ATLAS IBL operation

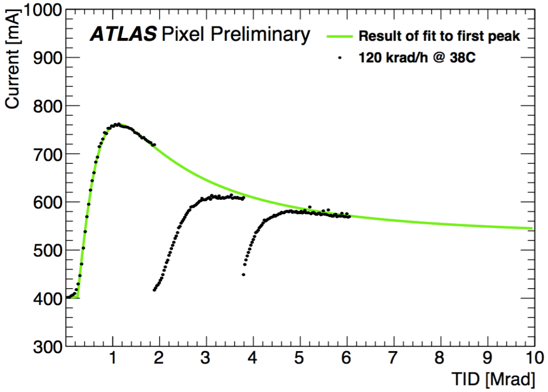
- The current of the FE-I4 chip (LV current) was stable at a value of 1.6–1.7A (for a four-chip unit) until the middle of September 2015.
- The current then started to rise up significantly → consequence of $I_{leak}$ increase in transistors.
  - Between September to November 2015 the current increase was more than 0.2 A even within a single LHC fill, depending on the luminosity and the duration of the fill.
- This led to a temperature increase of the modules.
  - Increased IBL distortion.
  - Drifting module calibration.



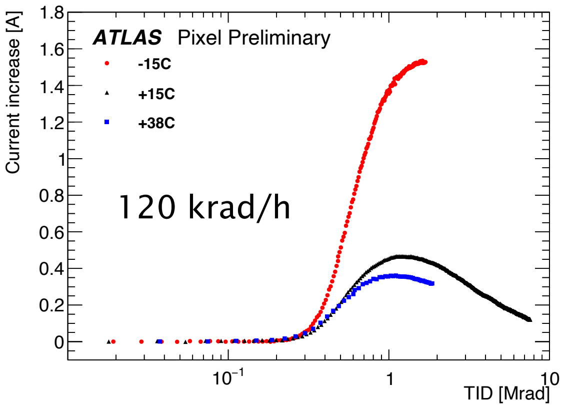
DOI:10.1109/NSSMIC.2016.8069865

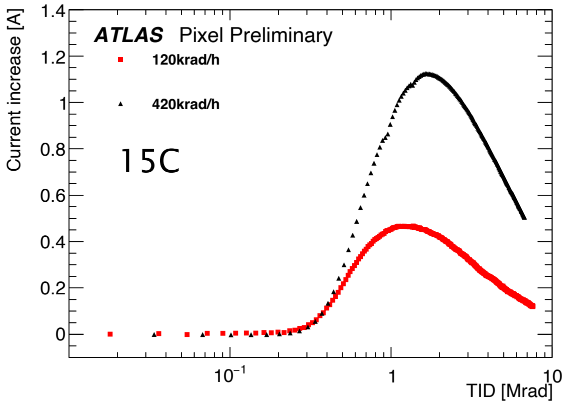
# Studies of IBL current increase

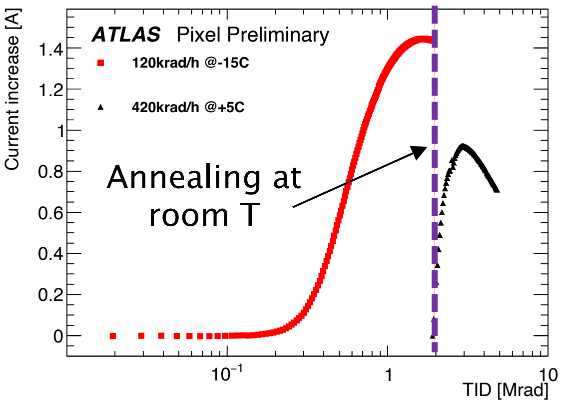
- X-rays irradiation were performed on IBL modules in the lab at different dose rates and temperatures.



- Important findings:
  - At a given temperature and dose rate, the current always approaches a boundary after annealing periods and re-irradiation.
  - At a given dose rate, the LV current increase is stronger at lower temperatures.
  - At a given temperature, the LV current increase is stronger at higher dose rates.
  - By increasing the operational temperature of the chip during irradiation the increase of the LV current can be kept below the boundary.







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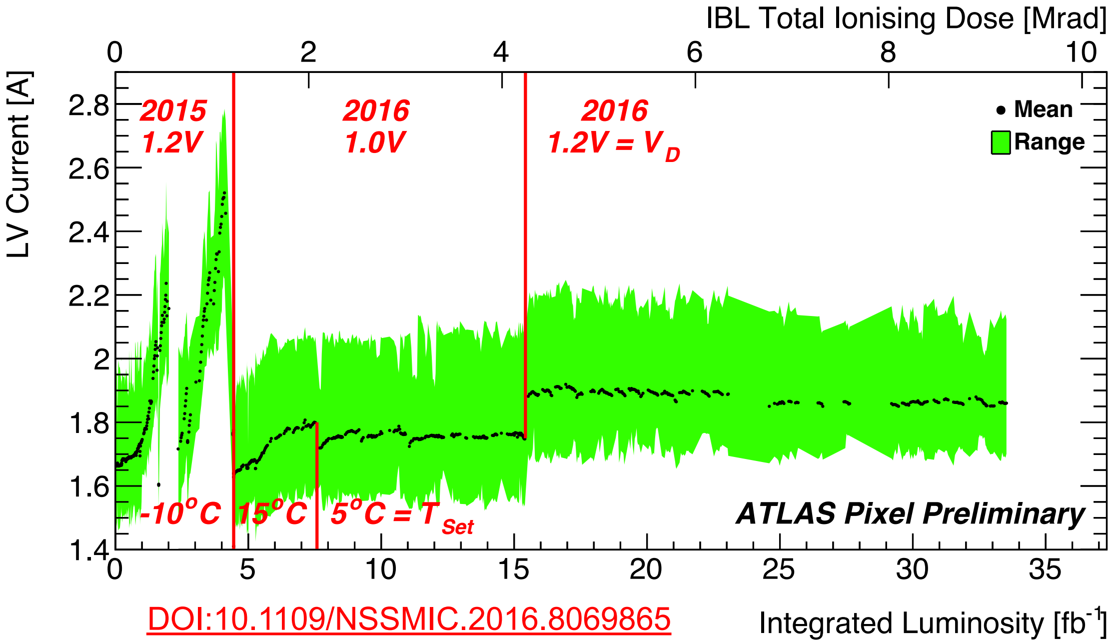
# IBL mitigation strategy

- Based on experience in 2015 and lab measurements, the IBL was run at higher temperatures and lower digital voltage for part of 2016.
- The digital voltage was increased back to 1.2V after 5 Mrad, well beyond the peak of current increase.



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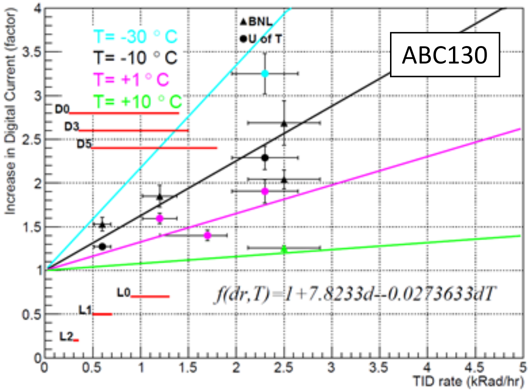
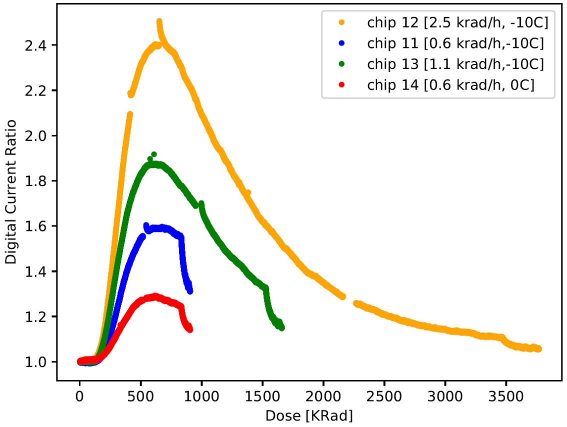
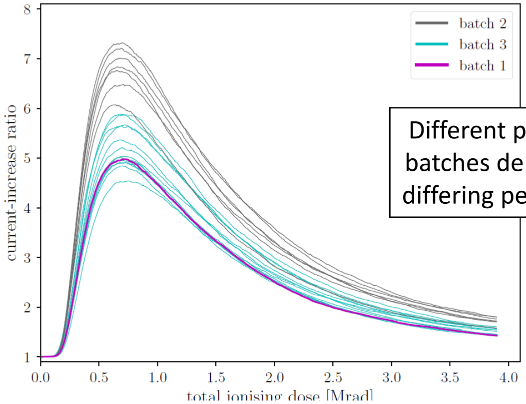
# TID mitigation measures for the ATLAS ITk

- The ITk is the new ATLAS Inner Tracker system for the HL-LHC.
  - All-silicon detector made of pixels and strips layers.

- The readout chip for the strips detector, the ABCStar, is designed in the same 130 nm CMOS process as the FE-I4.
  - Max TID at ITk for the ABCStar = 60-70 Mrad.
  - Enclosed layout transistors are used in the analogue part of the chip.
  - Extensive irradiation campaigns to study current increase versus temperature and dose rate.
    - Slow dose rate to estimate current increase during operation, high dose rate studies to gather information on larger samples of chips.



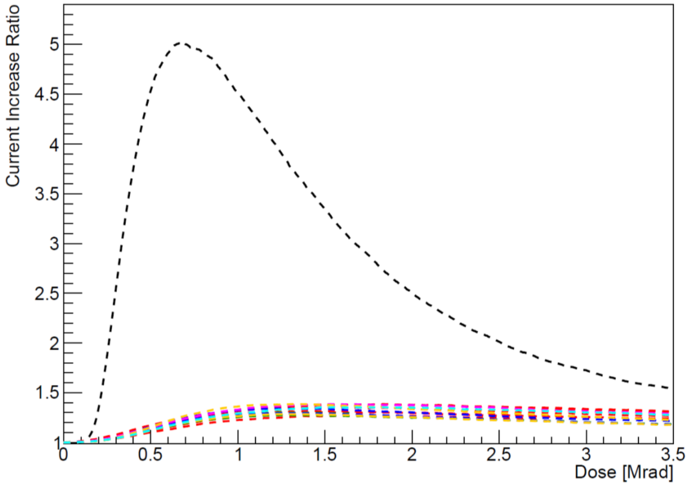


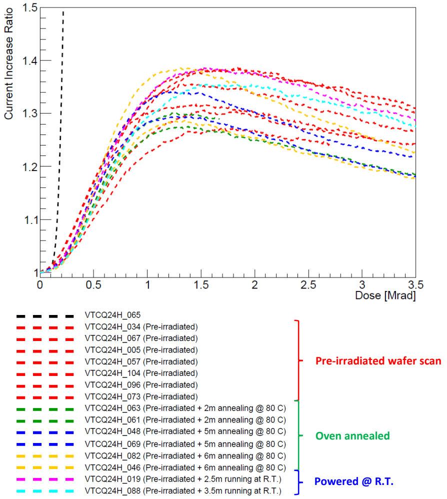


Different production batches demonstrate differing peak heights

# ATLAS ITk TID consequences and mitigations

- Consequences of higher current for the operation:
    - Cable plant and cooling system requirements need to be adapted.
    - Implications on system stability/alignment during runs.
    - Voltage regulators cannot support more Vdrop on cables.
    - Higher transients from module switch off.
    - Un-predictable wafer-by-wafer and batch-by-batch variations.
    - Thermo-electric models based on very low statistics.
- Mitigation: pre-irradiation of all ABCStar chips to be used in the experiment.
    - After pre-irradiation and annealing, current peak is lower.





# TID effects in CMOS 65 nm and 28 nm

- TID effects become more complex in smaller technology nodes.
- Thinner gate oxide is beneficial however…
  - Thick oxides still presents.
  - Effect from other structures, such as gate spacers (nitride).
  - Radiation Induced Short Channel Effect (RISCE).

- Suggestions for reading:
  - F. Faccio et at., Influence of LDD Spacers and H++ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses, DOI: 10.1109/TNS.2017.2760629
  - G. Borghello, Ultra-high-dose effects on 28nm CMOS technology, https://indico.cern.ch/event/863071/contributions/3738765/attachments/2044482/3424763/ACES_2020.pdf

# Summary and final considerations

- Radiation hardness is one of the most important requirements for operation of silicon tracking systems at high luminosity collider experiments.

- Development of radiation hard sensors and electronics is carried out by large experimental collaborations and takes many years of development.

- Work on the silicon technologies is supported by modelling and simulations (see work by the RD50 collaboration).

- Silicon detectors exist that will be able to cope with the HL-LHC environment, i.e. up to $2 \times 10^{16}\ n_{eq}/cm^2$ and 1 Grad.

- For future hadron colliders (e.g. FCC hh), radiation levels will increase to $6 \times 10^{17}\ n_{eq}/cm^2$ and 40 Grad → Completely new challenge; Will silicon still work? Will we need new materials? Which ones? …