Device Fabrication

(or how the detectors for your experiment get made)

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UK Instrumentation Lectures

Outline of Lectures

Lecture 1 (today)

- Brief look at why Silicon detectors* are used
- Outline of the steps used to fabricate a microstrip detector
  - PhotoLithography
  - E-beam Lithography
  - Resists
  - Applications of E-beam lithography
  - Additive/Subtractive Processes
    - Lift Off
  - Etching
    - Wet
    - Dry (Plasma & ICP)
    - FIB
  - Doping
- Cleanrooms and Specifications
- New Detector geometries (3D, edgeless, TSV)

** Other semiconductors are available*

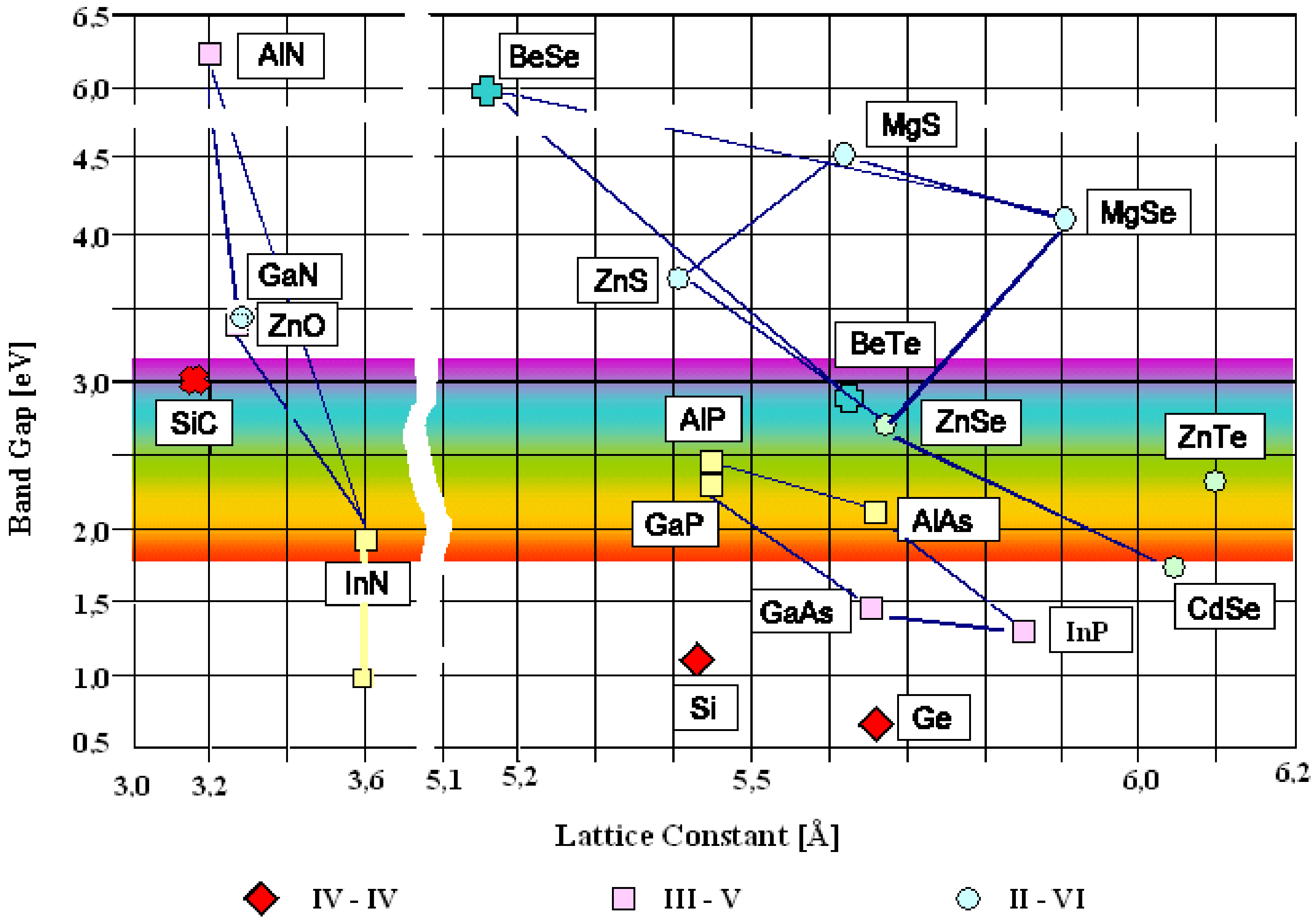
Semiconductor Materials

	Material	Bandgap (eV)	Uses
Si	Silicon	1.11	Particle, X-ray
CdZnTe	Cadmium Zinc Telluride	1.4-2.2	X-Ray
GaAs	Gallium Arsenide	1.43	Particle, X-ray
SiC	Silicon Carbide	2.86	UV/Rad Hard
GaN	Gallium Nitride	3.4	UV/Rad Hard
C	Diamond	5.5	UV/Rad Hard

Issues

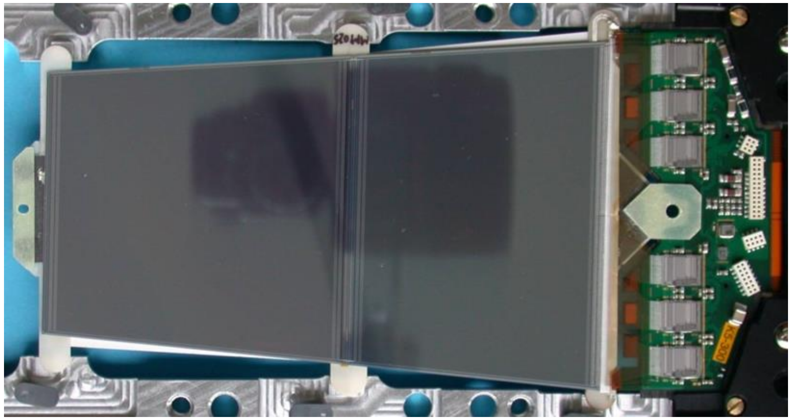
- Growth – How easy to make?
- Defects – How many?
- Material science – contact formation, pasivation etc

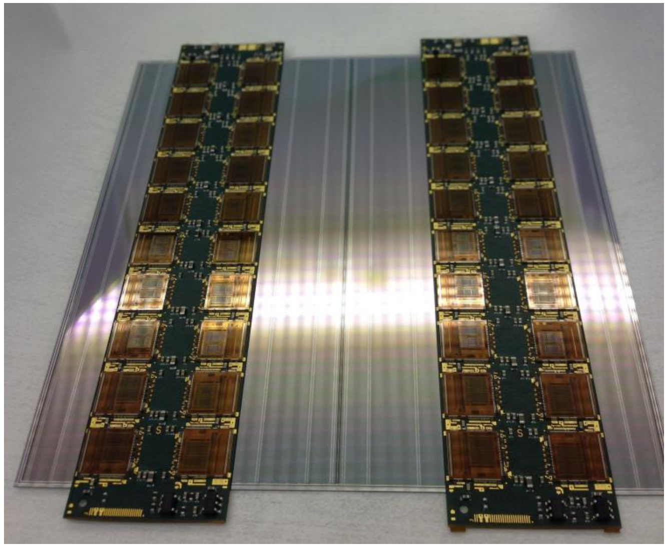
Semiconductor Materials



http://www.tf.uni-kiel.de/matwis/amat/semitech_en/kap_2/illustr/materials.gif

Why Silicon?





Material is well known

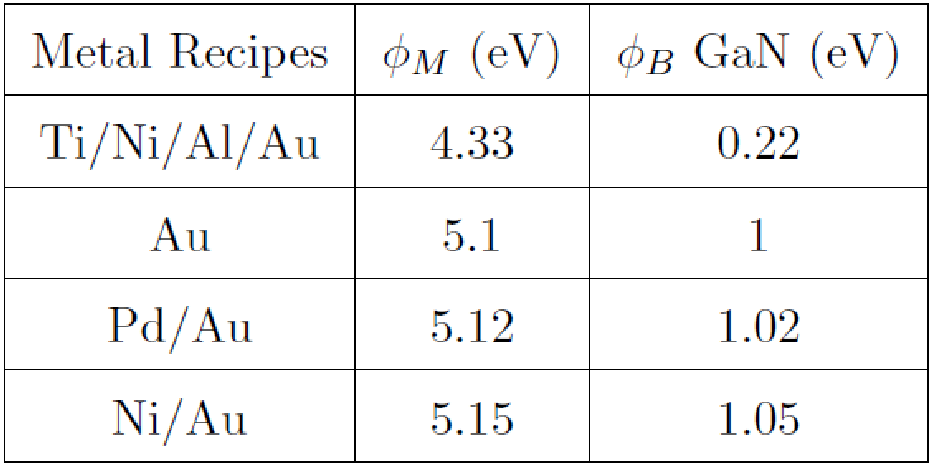
- Very high purity material is commonly available
- Higher purity material reduces leakage current and noise

Fabrication processes are very well developed

- Technology doesn't have to be developed. It already exists, reducing the production time by several years

Contact formations

- Non Si based Semiconductors can have ‘non trivial’ Metal contact schemes
- Example: Gallium Nitride (GaN)



Metal Recipes	ϕ_M (eV)	ϕ_B GaN (eV)
Ti/Ni/Al/Au	4.33	0.22
Au	5.1	1
Pd/Au	5.12	1.02
Ni/Au	5.15	1.05

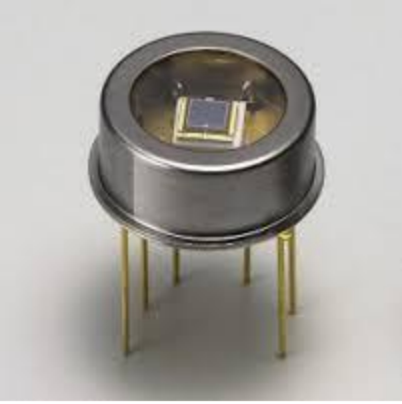
Work Functions and associated Schottky barrier heights for various metal contact schemes on GaN

Semiconductor Detectors

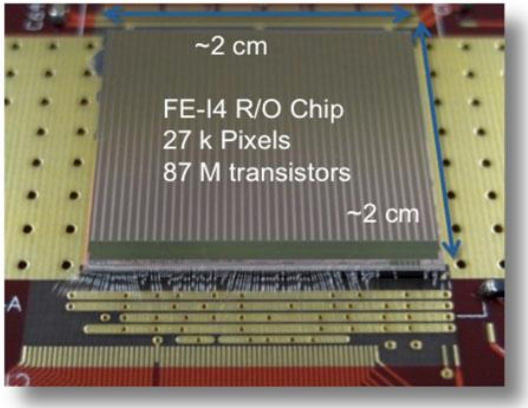
- The main semiconductor detectors used in physics are
  - Single Segment
    - Large or small ‘1D’ detectors (energy and timing Information)
    - Eg Si Photo Diodes
  - Multi Segmented
    - 2D detectors (Position, energy and timing information)

  - You can use lots of single segmented detectors in array to get position information
  - Or can you can use fabrication techniques to create ‘sub cell’ information
    - Pixel Detectors
    - Strip Detectors

- So how do we decide on what to make?
  - Physics needs, cost, complexity, yield…

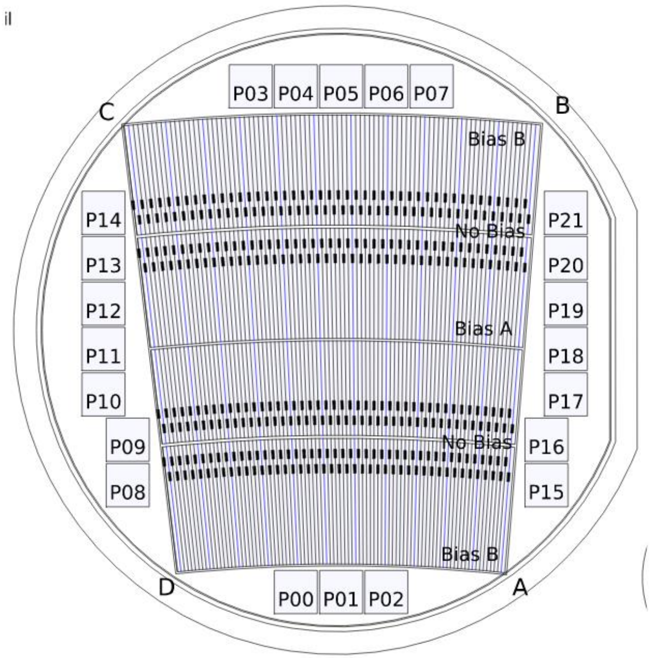


‘Single Segment’ Photodiode



‘Multi Segmented ’ Pixel Detector

Semiconductor Detectors: Wafer Scale



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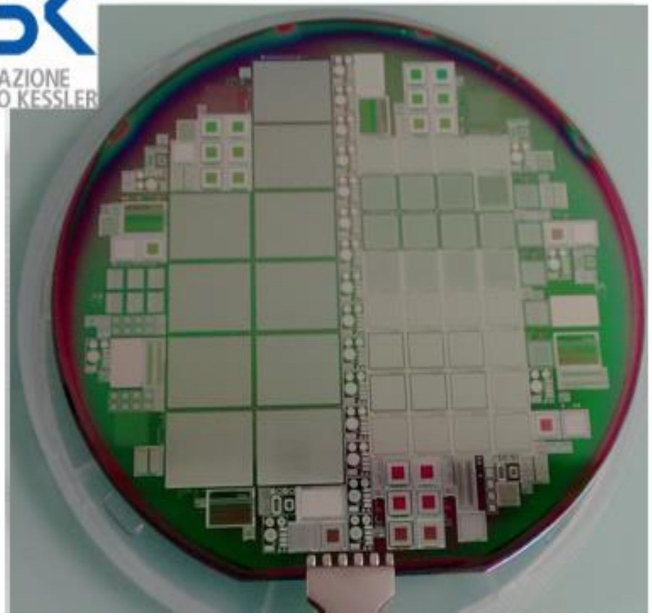
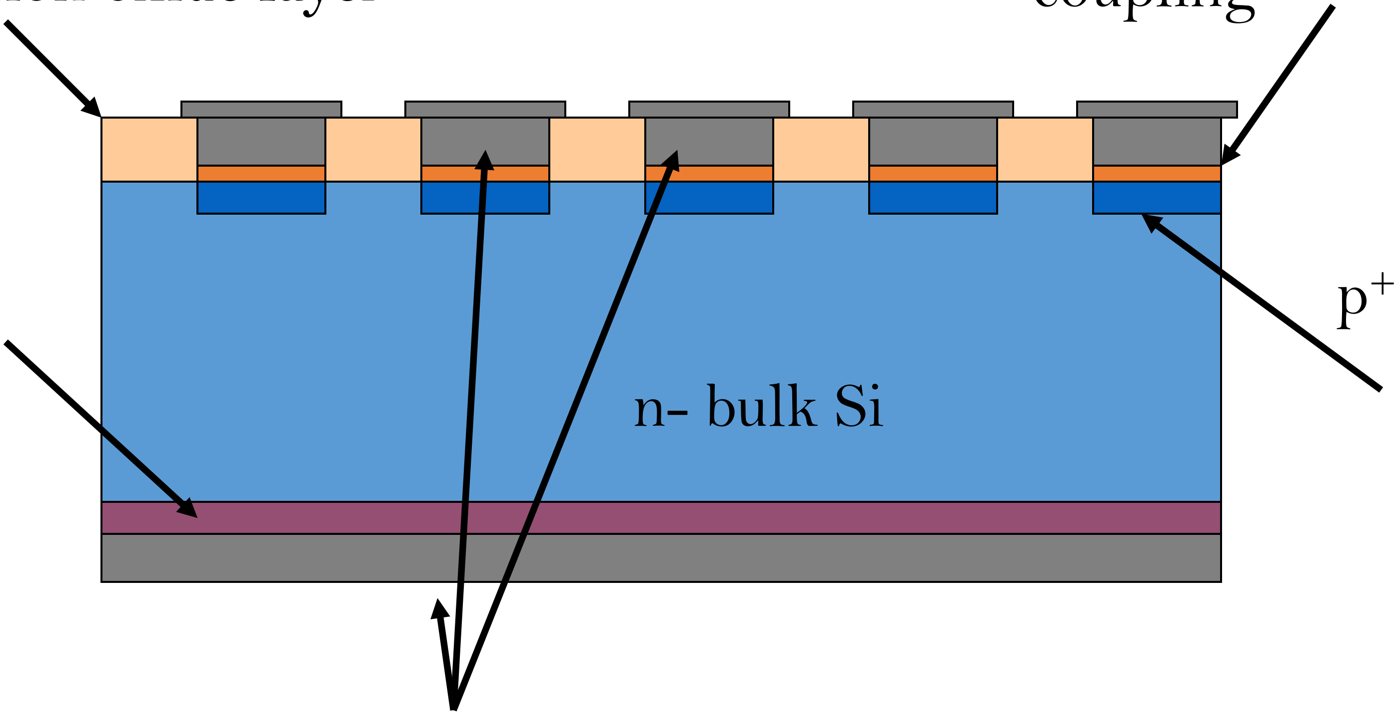
BRUNO KESSLER



Wafer Size (inches)	Wafer Size (mm)	Thickness (um)
2	51	275
3	76	375
4	100	525
5	76	625
6 (5.9)	100	675
8 (7.9)	200	775

Stages in Creating A Si Microstrip Detector



passivation oxide layer

oxide for capacitive coupling

n^+ doped

p^+ doped

n- bulk Si

aluminium contacts

Starting Material

High purity, high resistivity Si n_{eff} ~10^{13} cm^{-3}

- Used because it reduces:
  - Depletion voltage
  - Leakage current
  - Defect concentrations
- Together these mean lower noise and more efficient operation

So..

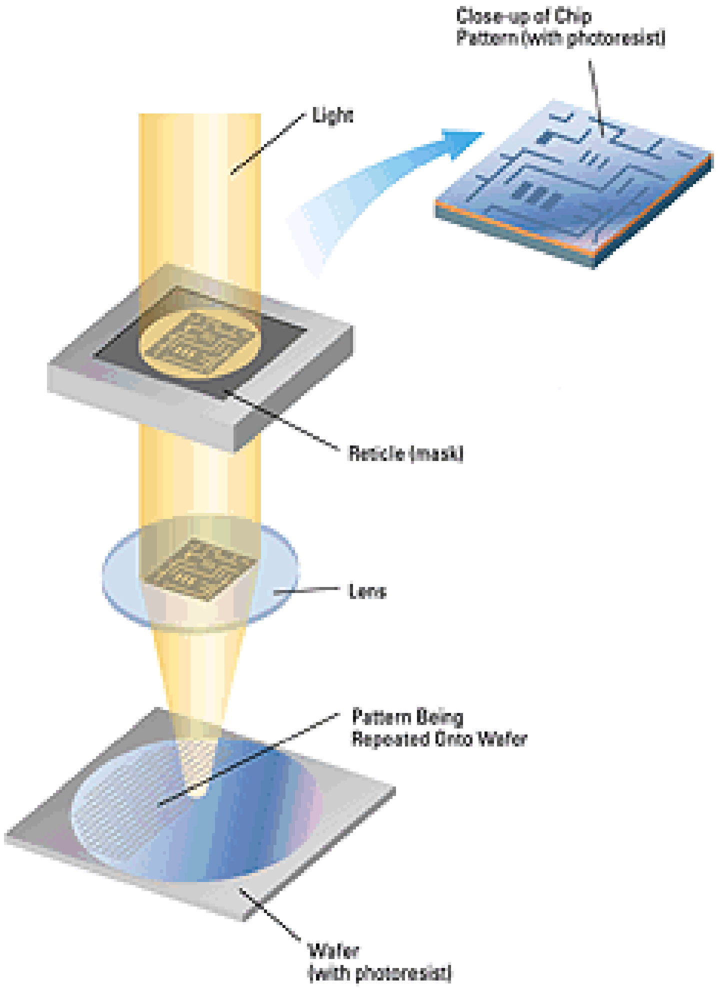
How do we start to “build” our layers of design on to the bulk material?

Lithography

Lithography:

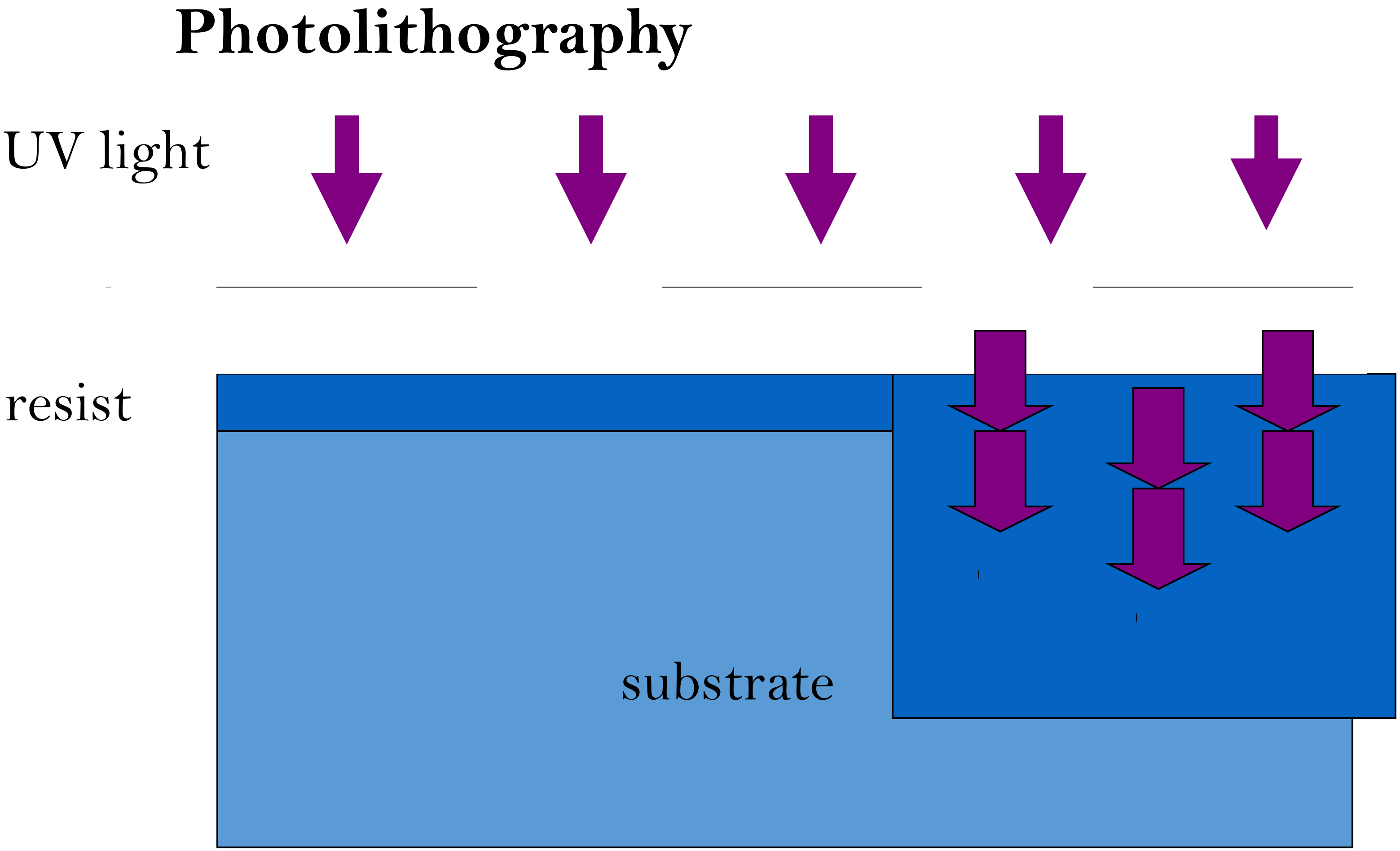
- The process of transferring a pattern to a material using an intermediate medium
- Two common types
  - Electron beam lithography
  - Photolithography
- This is the process which allows the others to be carried out.

Photolithography



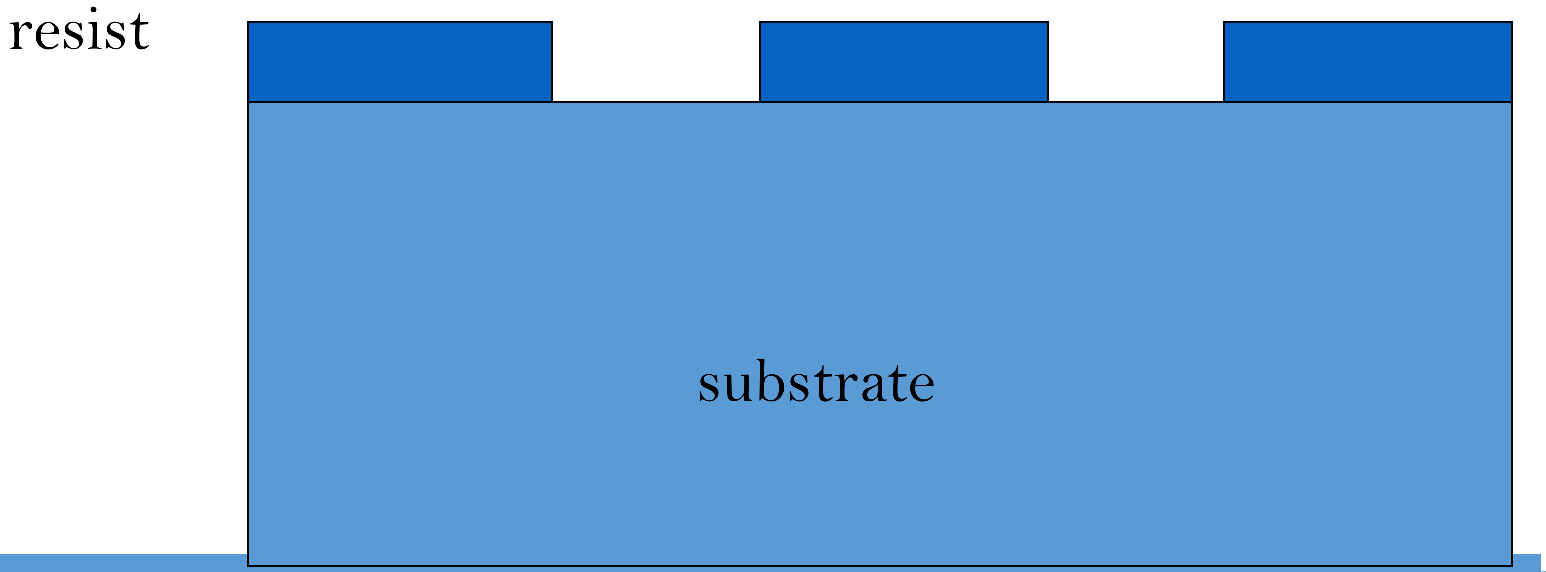
- Transfers the pattern using UV light via photoresist
- Areas exposed to light will wash away in solvent due to chain scission
- Masks used are written using e-beam
- Chlorobenzene can be used to enhance metal lift-off

Lithography



Lithography

Photolithography



Photolithographic Mask

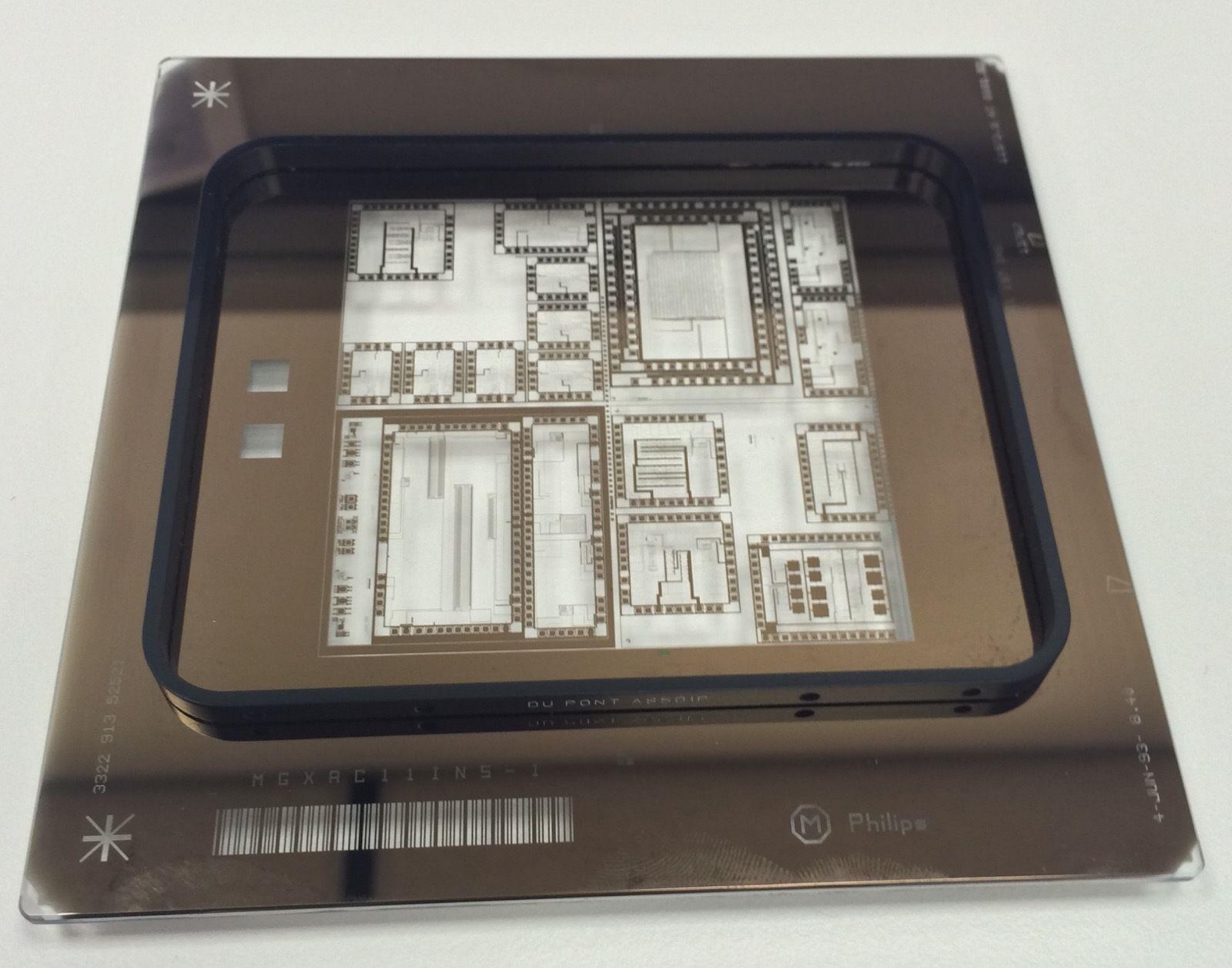


Photo Resists

- Resist chosen depends on
  1. Selectivity - Amount of light needed to create chemical change in the resist
  2. Resolution – Determines the minimum feature size that can be transferred onto the resist
  3. Thickness – Amount of resist that can be used as an etch mask

- There are 8 photoresists used in the Glasgow Engineering Dept, all with a range of alignment, development times

- However, these times will also change depending on the feature size of the pattern

Lithography

Photolithography: The good

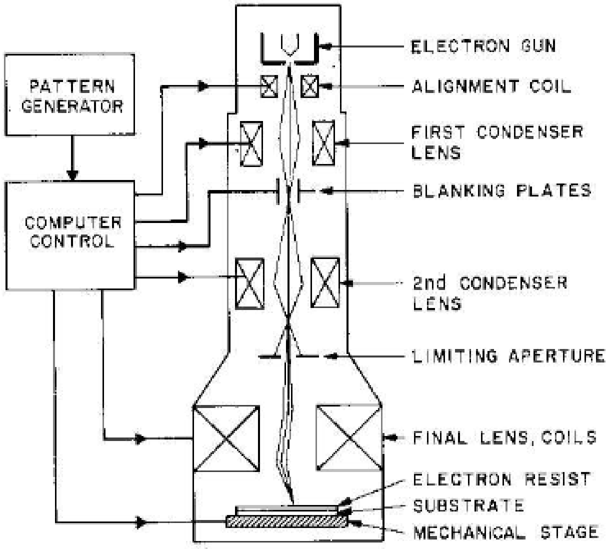
- Quick relatively simple process
  - Printing process entire wafer exposed at once
- The resist compounds are very robust
  - Patterns produced are suitable for a large number of subsequent processes

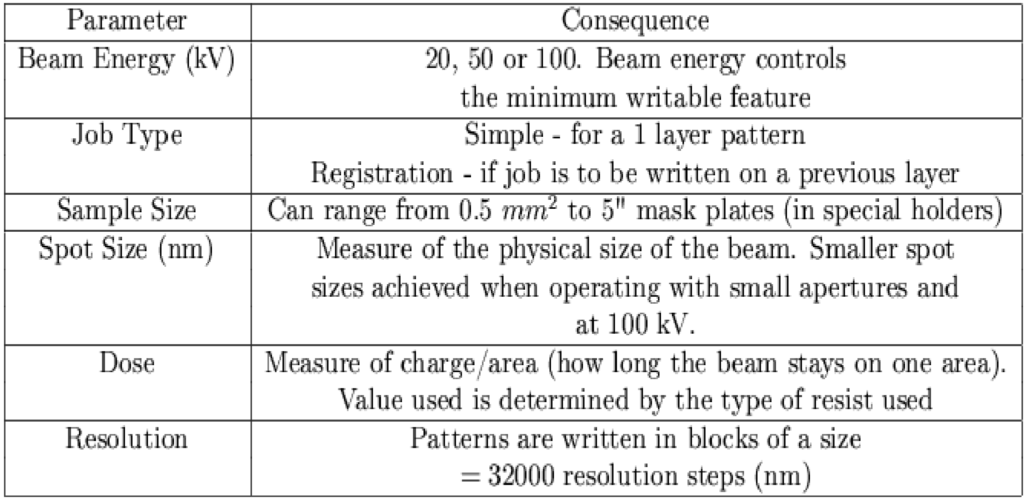
Lithography

Photolithography: The bad

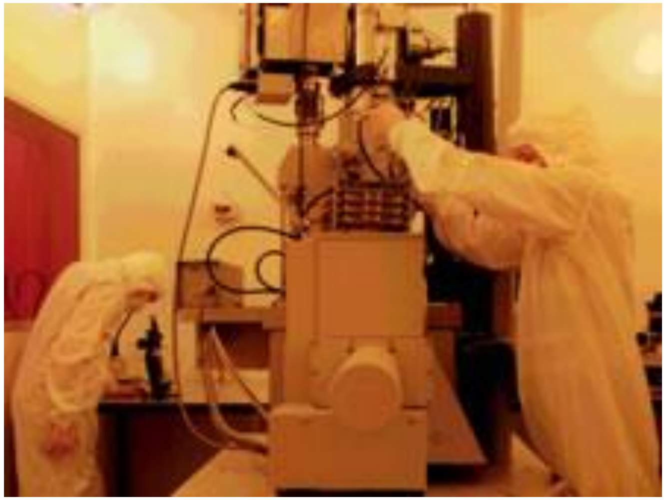
- Resolution limited
  - Minimum feature size ~1 mm for manual photolithography
  - Industrial best ~ 0.15 mm, Pentium chips
- Possible contamination
  - The use of a physical mask can introduce contaminants

Electron Beam Lithography



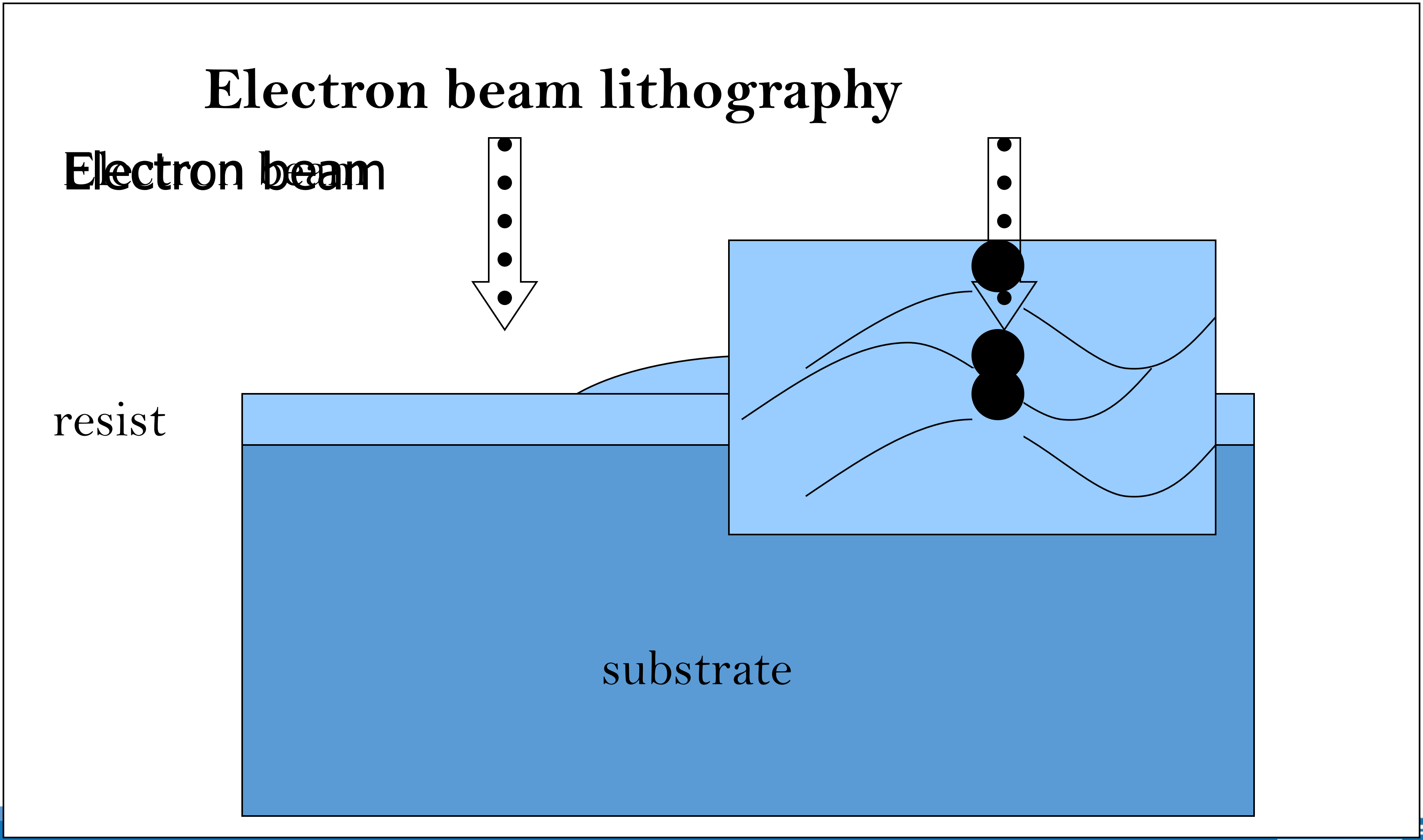


Parameter	Consequence
Beam Energy (kV)	20, 50 or 100. Beam energy controls the minimum writable feature
Job Type	Simple - for a 1 layer pattern Registration - if job is to be written on a previous layer
Sample Size	Can range from 0.5 mm^2 to 5" mask plates (in special holders)
Spot Size (nm)	Measure of the physical size of the beam. Smaller spot sizes achieved when operating with small apertures and at 100 kV.
Dose	Measure of charge/area (how long the beam stays on one area). Value used is determined by the type of resist used
Resolution	Patterns are written in blocks of a size = 32000 resolution steps (nm)



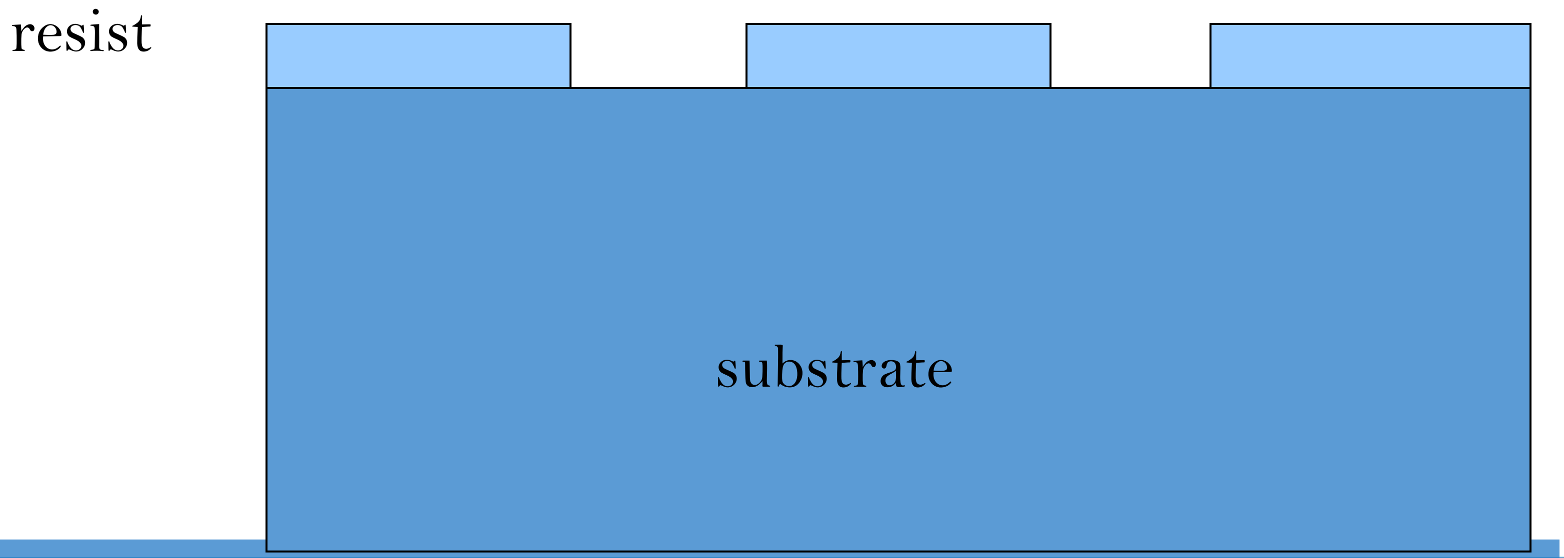
- Electrons are generated by an electron gun
- Condenser lens focus the beam to a set diameter
- Banking plates switch the beam on/off
- Aperture controls the current density of the beam

Lithography


Electron beam lithography

Lithography

Electron beam lithography



E-Beam Mask?

- There isn't one

- Pattern is made by as CAD file (gds)
    - Translated into movements of the electron beam

Lithography

Electron beam lithography: For

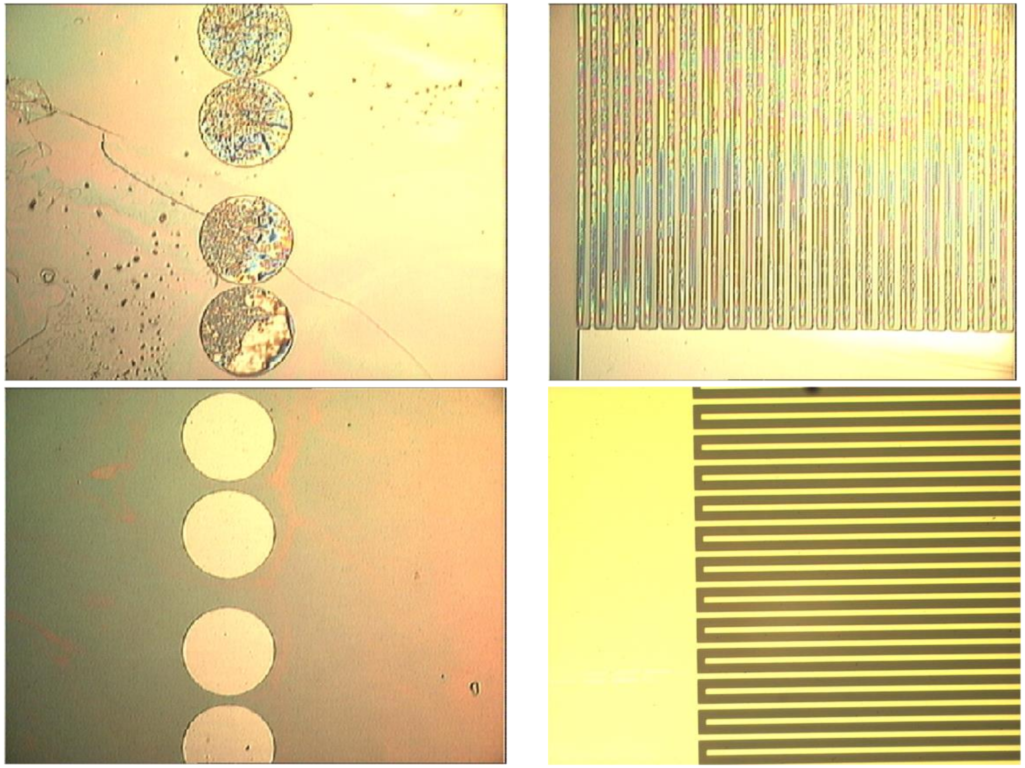
- Resist much thinner
  - ~100 nm thicknesses available
- Resolution down to ~10 nm
  - Limited by Gaussian spread of the electron beam
- Less contamination
  - No mask, direct write

Lithography

Electron beam lithography: Against

- Slow and expensive
  - Vector scan technique writes the pattern sequentially
- Resist compounds not as robust
  - Limits possible processes for patterned substrates

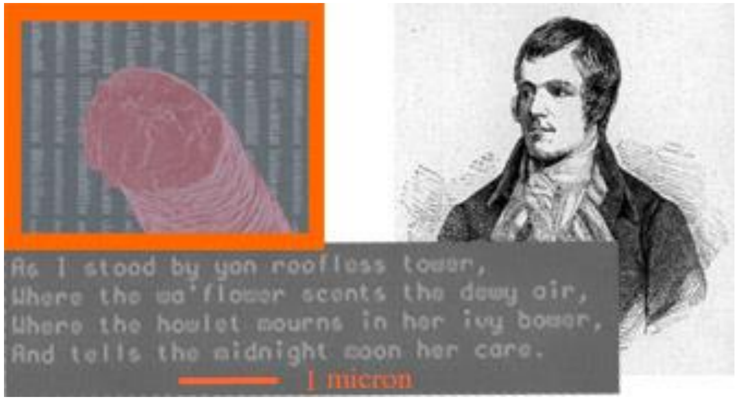
E-beam – Good + Bad



Dose tests : (Top left) under exposure

(Top right) over exposure

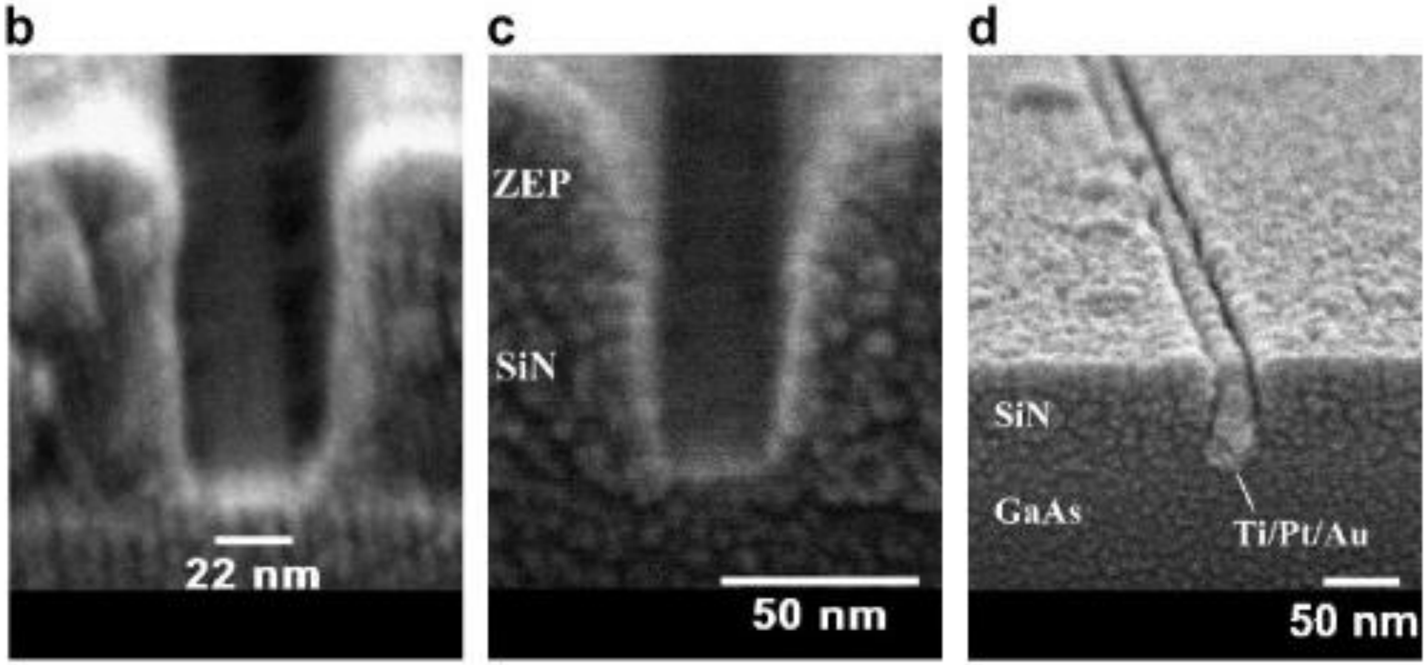
(Bottom) – Correct exposure

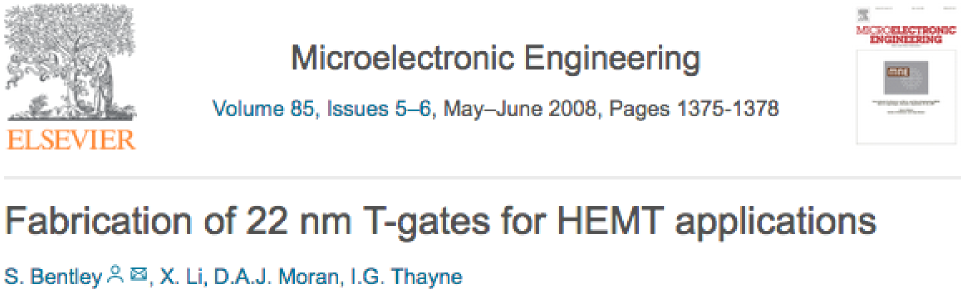


As I stood by yon roofless tower,
Where the wa'flower scents the dewy air,
Where the howlet mourns in her ivy bower,
And tells the midnight moon her care.

A book of the Complete Works of Robert Burns, Scotland's National Bard, has approximately 480 pages. To publicise the capability of the new Vistec VB6 UHR EWF electron beam lithography tool at the JWNC, we used it to write the Complete Works of Robert Burns on a small piece of silicon. Ten copies would fit on the head of a pin and this is likely to be the world's smallest copy of the works of Burns. The image shows pages of text alongside a human hair plus detailed text from the song "As I stood by yon roofless tower". Each character is approximately 150 nm

E-Beam: 22nm Gates





Microelectronic Engineering

Volume 85, Issues 5–6, May–June 2008, Pages 1375-1378

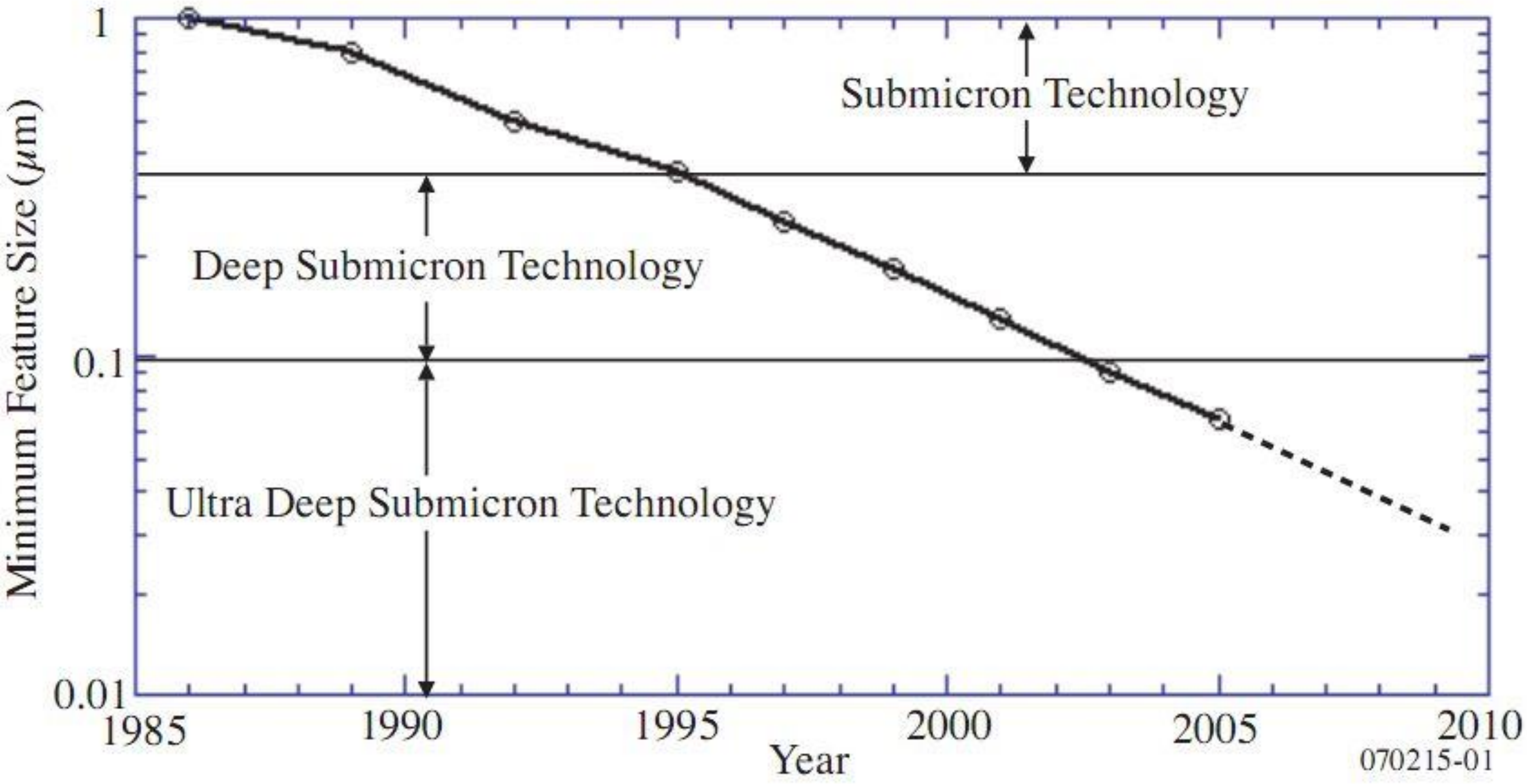
Fabrication of 22 nm T-gates for HEMT applications

S. Bentley, X. Li, D.A.J. Moran, I.G. Thayne

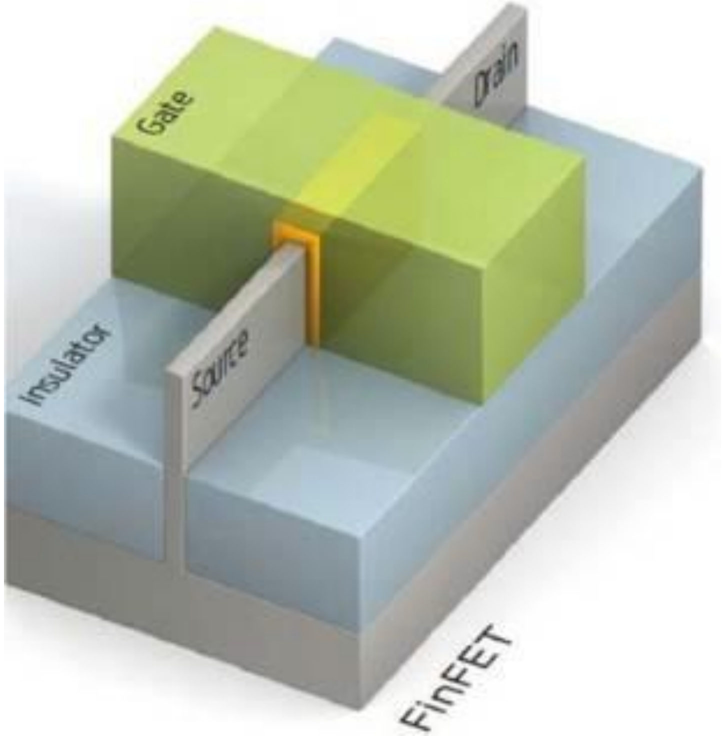
CMOS

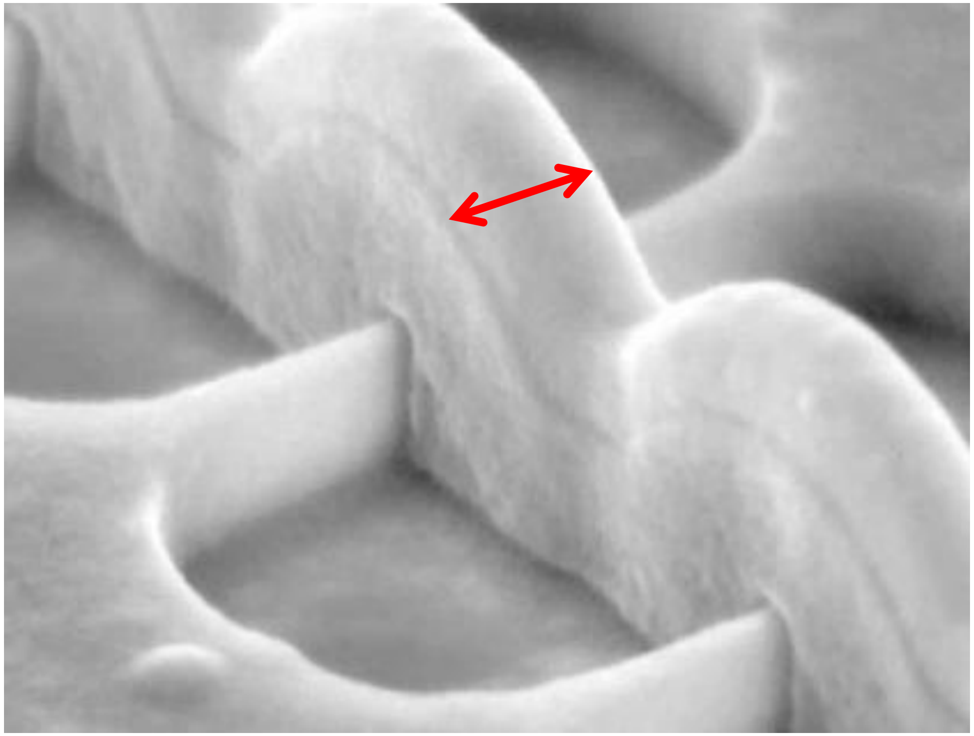
- As well as for fabrication of semiconductor detectors, lithography (e-beam) is essential for the production of CMOS devices
- Used mostly in particle physics for readout
  - Can be used for data processing, multiplexing etc
- Advantages to going to smaller technology
  - Cost, power, integration of Digital and Analog, chip size…

CMOS technology



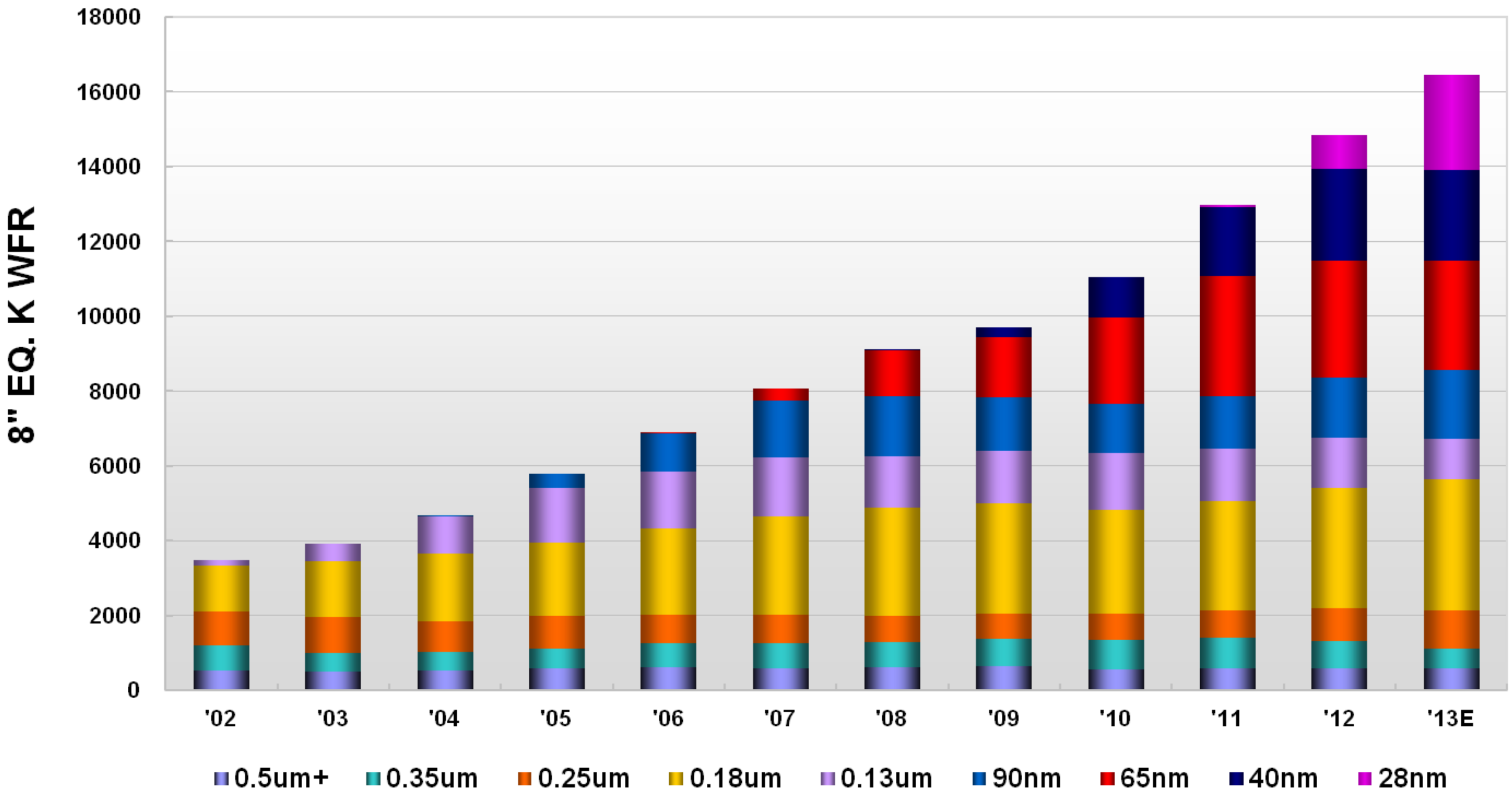
State of the art 2013: 16 nm FINFET





Source: TSMC

Installed Capacity by Technology



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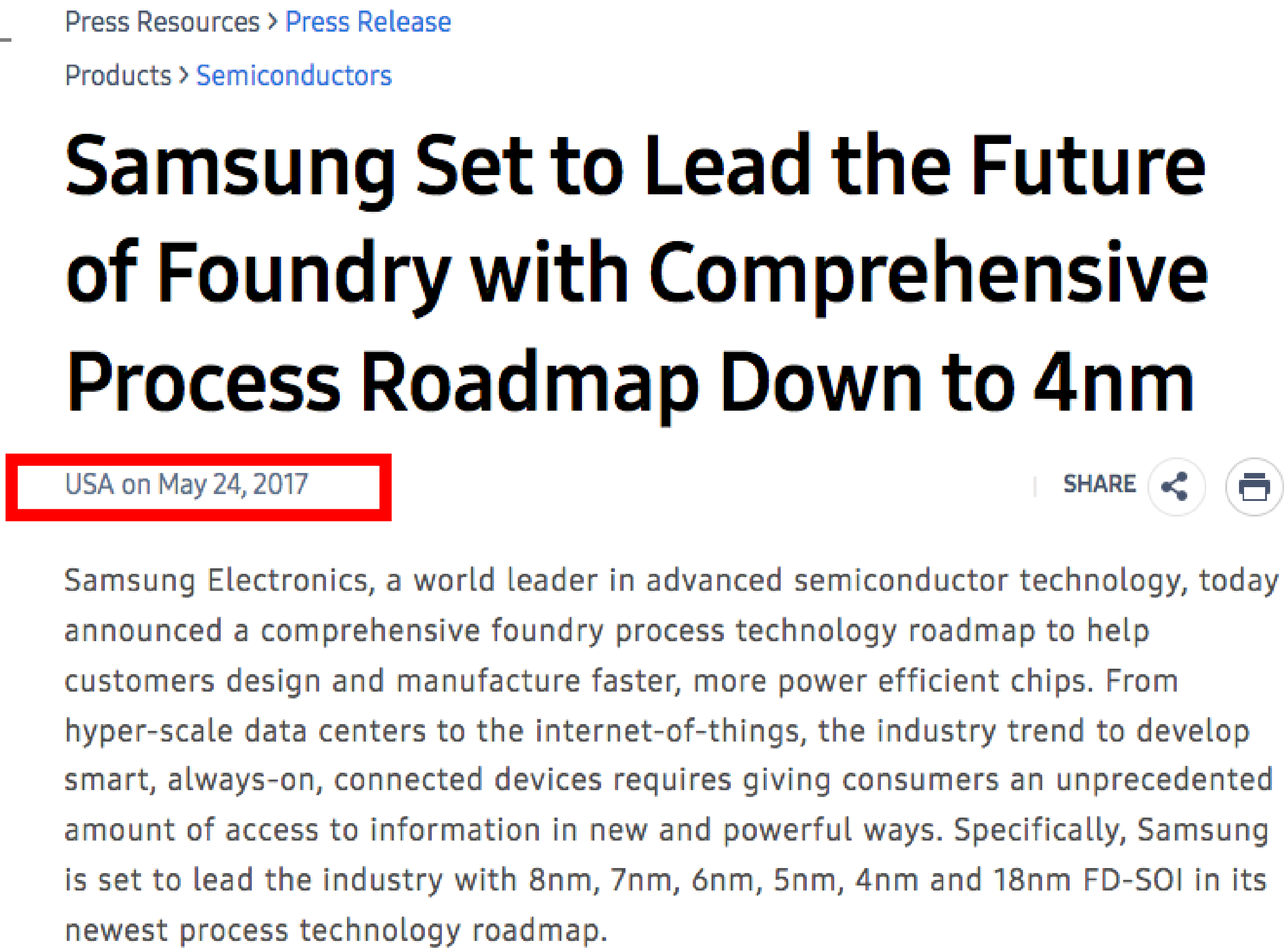


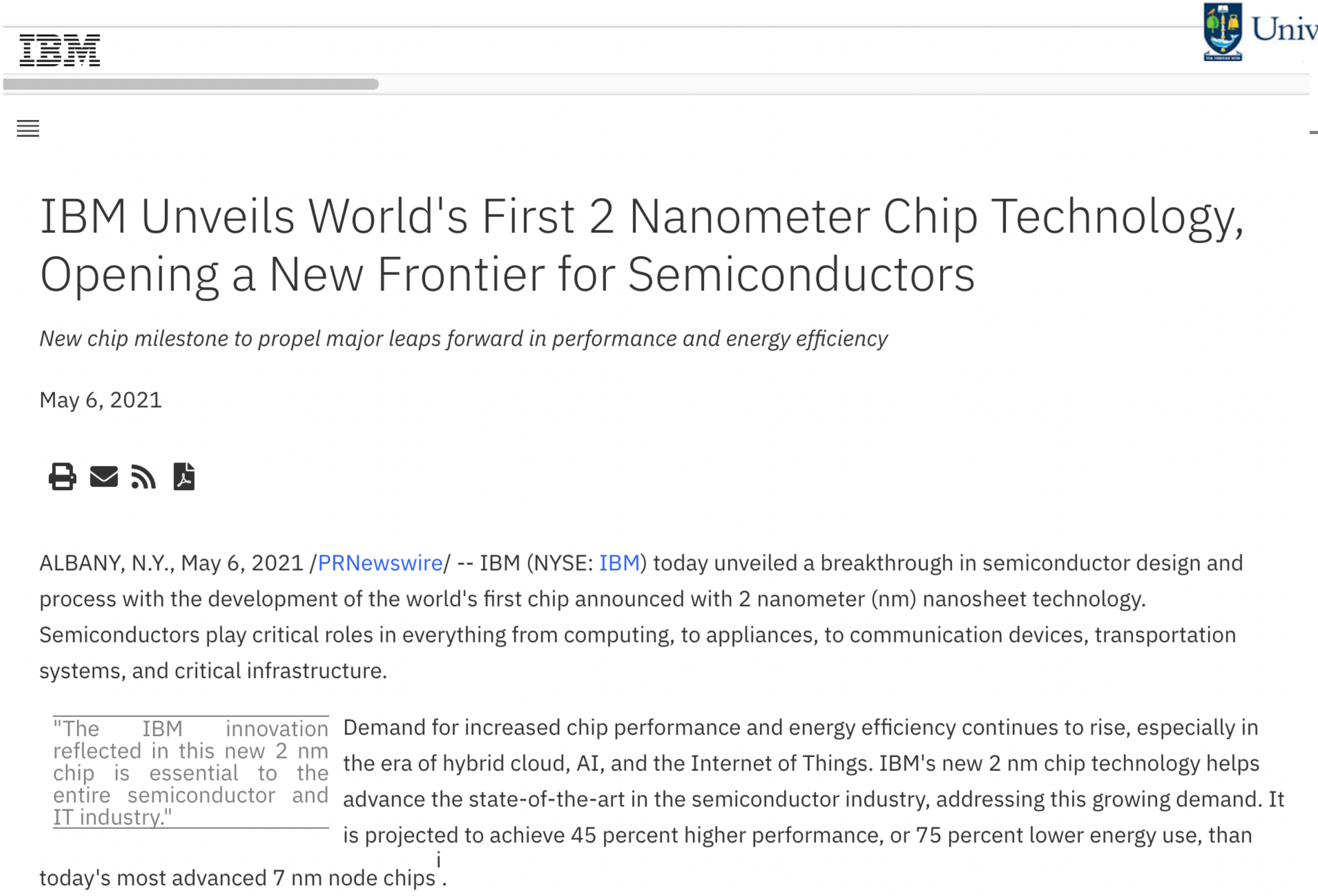
Press Resources > Press Release

Products > Semiconductors

Samsung Set to Lead the Future of Foundry with Comprehensive Process Roadmap Down to 4nm

USA on May 24, 2017

Samsung Electronics, a world leader in advanced semiconductor technology, today announced a comprehensive foundry process technology roadmap to help customers design and manufacture faster, more power efficient chips. From hyper-scale data centers to the internet-of-things, the industry trend to develop smart, always-on, connected devices requires giving consumers an unprecedented amount of access to information in new and powerful ways. Specifically, Samsung is set to lead the industry with 8nm, 7nm, 6nm, 5nm, 4nm and 18nm FD-SOI in its newest process technology roadmap.



IBM Unveils World's First 2 Nanometer Chip Technology, Opening a New Frontier for Semiconductors

New chip milestone to propel major leaps forward in performance and energy efficiency

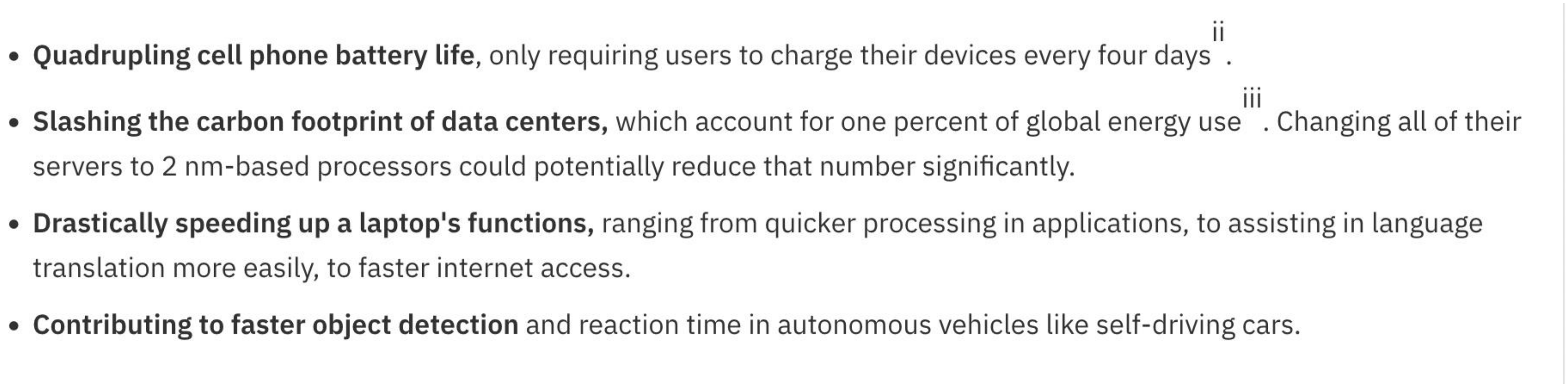
May 6, 2021

ALBANY, N.Y., May 6, 2021 /PRNewswire/ -- IBM (NYSE: IBM) today unveiled a breakthrough in semiconductor design and process with the development of the world's first chip announced with 2 nanometer (nm) nanosheet technology. Semiconductors play critical roles in everything from computing, to appliances, to communication devices, transportation systems, and critical infrastructure.

"The IBM innovation reflected in this new 2 nm chip is essential to the entire semiconductor and IT industry."

Demand for increased chip performance and energy efficiency continues to rise, especially in the era of hybrid cloud, AI, and the Internet of Things. IBM's new 2 nm chip technology helps advance the state-of-the-art in the semiconductor industry, addressing this growing demand. It is projected to achieve 45 percent higher performance, or 75 percent lower energy use, than today's most advanced 7 nm node chips[i].

https://newsroom.ibm.com/2021-05-06-IBM-Unveils-Worlds-First-2-Nanometer-Chip-Technology,-Opening-a-New-Frontier-for-Semiconductors

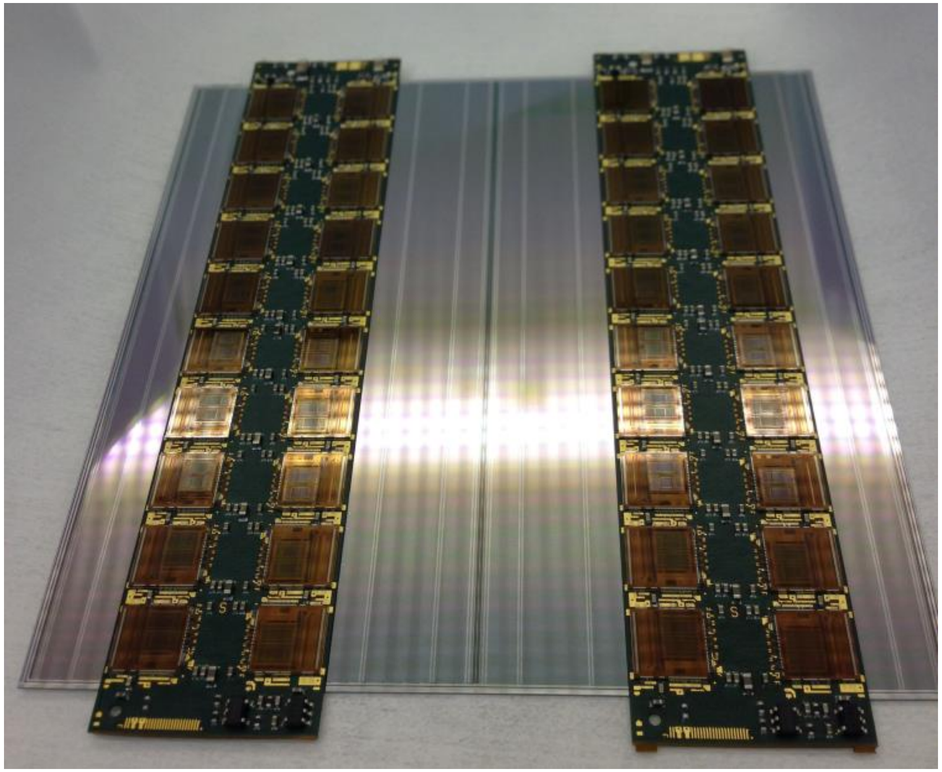


- **Quadrupling cell phone battery life**, only requiring users to charge their devices every four days[ii].
- **Slashing the carbon footprint of data centers,** which account for one percent of global energy use[iii]. Changing all of their servers to 2 nm-based processors could potentially reduce that number significantly.
- **Drastically speeding up a laptop's functions,** ranging from quicker processing in applications, to assisting in language translation more easily, to faster internet access.
- **Contributing to faster object detection** and reaction time in autonomous vehicles like self-driving cars.

https://newsroom.ibm.com/2021-05-06-IBM-Unveils-Worlds-First-2-Nanometer-Chip-Technology,-Opening-a-New-Frontier-for-Semiconductors

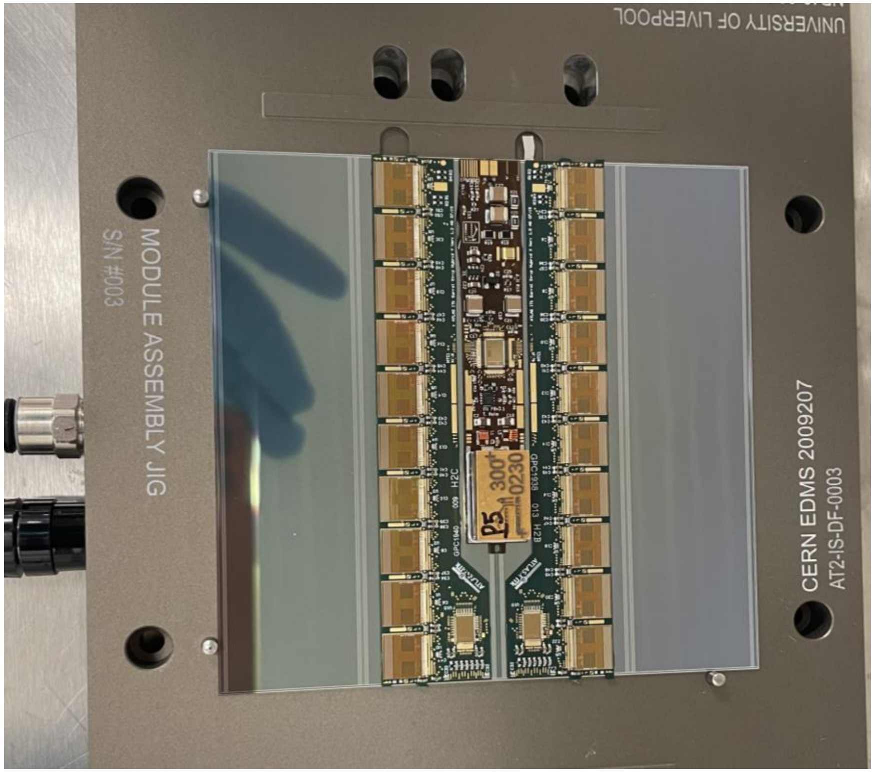
CMOS Improvements – Closer to Home

ATLAS ITk Strip Module - 250nm Chip set



2013

ATLAS ITk Strip Module – 130nm Chip set



2023

Summary

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