Circuits and layouts II

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Overview

- **Introduction, definitions**
- **Hybrid and Monolithic Sensors**
- **Common isolation techniques**
- **Example of ItK Strips HV biasing**

Introduction

- IC (integrated circuit) single silicon chip that includes active and passive interconnected devices to implement complex operations (analogue, digital)

- Planar technology: the processing steps are implemented in a thin layer of the surface of the chip

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

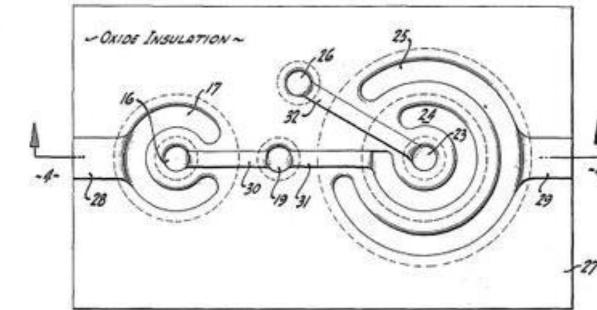

FIG-3

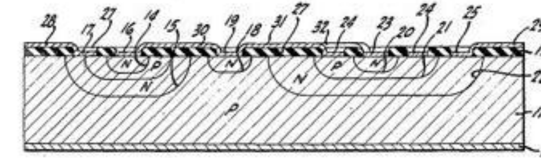

FIG-4

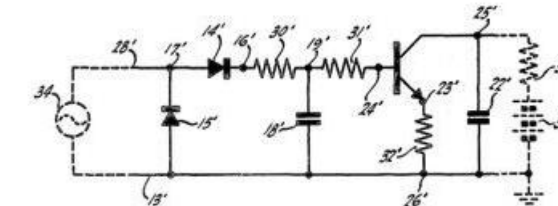

FIG-5

INVENTOR.
ROBERT N. NOYCE
BY Lippincott & Ralls
ATTORNEYS

Semiconductor device-and-lead structure
US2981877A
First planar IC patent, 1961

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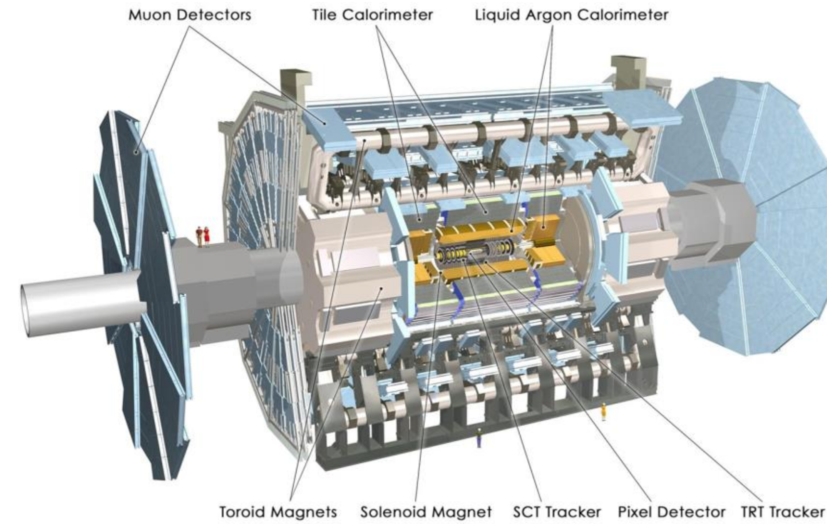
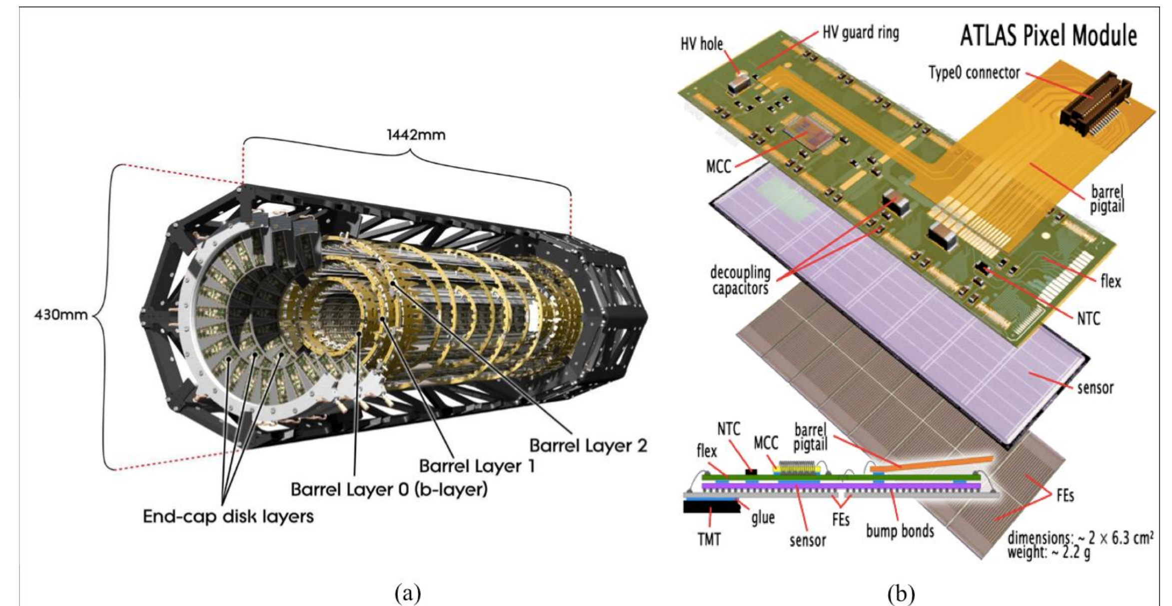
Introduction

- Planar technology used also for HEP detector technology

- Remarkable evolution in planar technologies impacted on detector technology as well

- HEP traditionally used the '**hybrid**' approach





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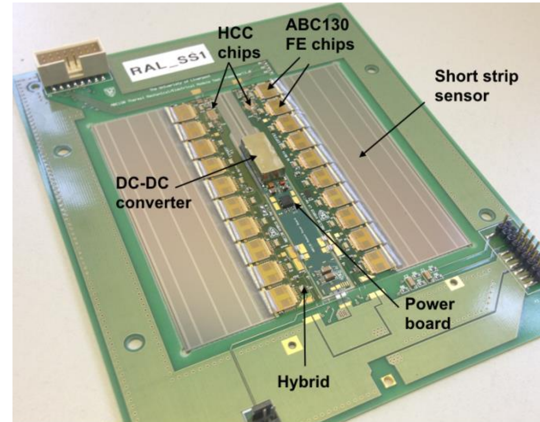
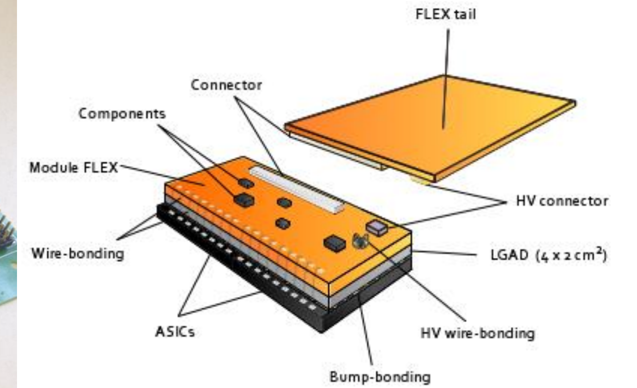
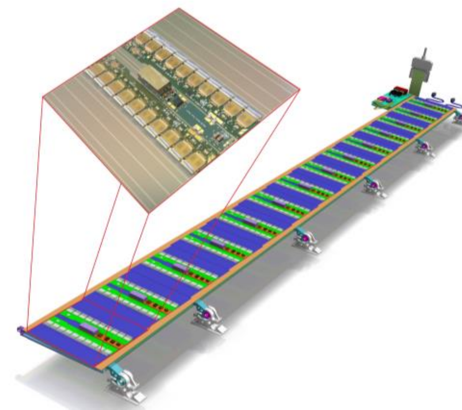
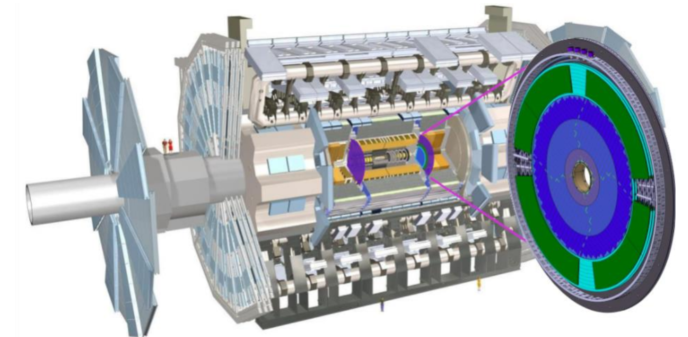
Hybrid solution

- **Hybrid**: different operations are implemented on different silicon chips (like sensing and read out on separate carriers)
    - High quality substrate for the **sensor** to optimize the charge collection efficiency and speed
    - It requires interconnect to the readout, i.e. complex bonding, affecting reliability, costs
    - Extra material due to the various layers







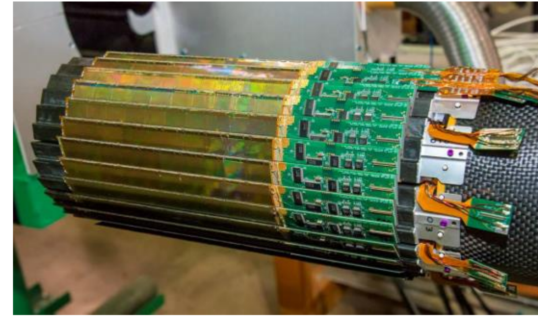


ATLAS Inner Tracker Upgrade (ITk) silicon strip module on barrel stave

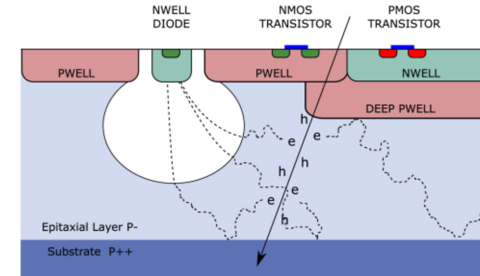
Hybrid module for the High Granularity Timing Detector (HGTD) for the upgraded ATLAS detector

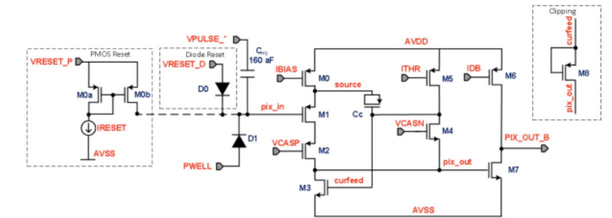
Monolithic solution

- **Monolithic**: sensor and readout are implemented on the same silicon chip
    - In-pixel processing possible: amplification and digitization integrated in the same chip
    - Small pixels (‘10’s x 10’s um)
    - Low noise, due to small pixel, low leakage, low capacitance
    - Good S/N
    - Sensitive region 10’us um, thinning of the sensor is possible, to reduce the overall mass

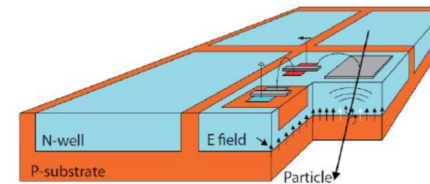


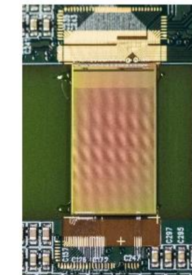
The vertex detector of the STAR experiment, the first to use CMOS MAPS





MAPS used for ALICE ITS upgrade, with in-pixel FE circuitry





HV MAPS used for Mu3e

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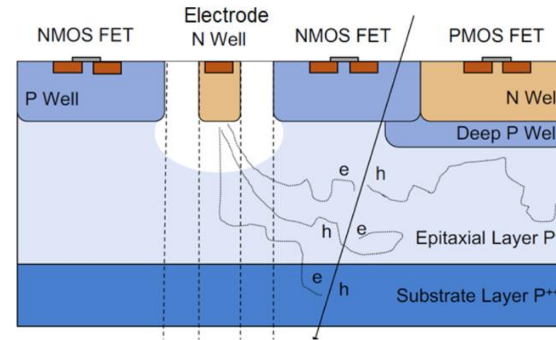
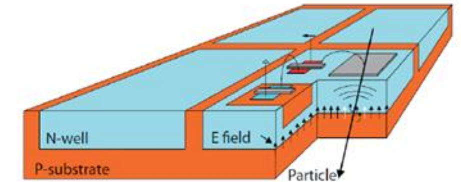
Monolithic solution



Deep P Well



Deep N Well

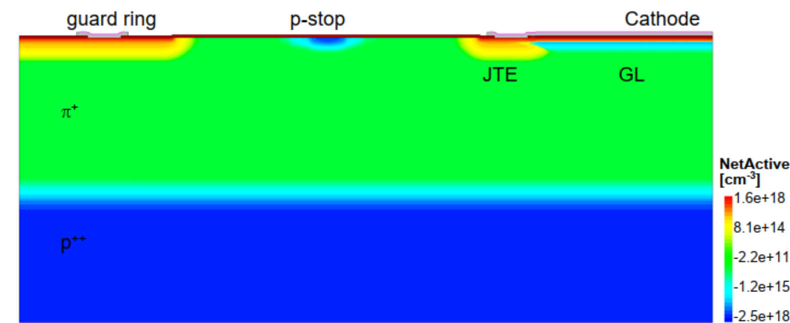
- **Monolithic**: sensing and read out are implemented on the same silicon chip
  - Mostly use commercial CMOS process
    - Redundancies of foundries
    - Potentially low cost, large area cover possible
    - High yield
  - Reliability, no need for wire/bump bonding

Monolithic approach is an interesting option for most HEP experiments

LHC Tracker Upgrades	Area
ALICE ITS	12 m^2
ATLAS Pixel	8.2 m^2
ATLAS Strips	193 m^2
CMS Pixel	4.6 m^2
CMS Strips	218 m^2
LHCb VELO	0.15 m^2
LHCb UT	5 m^2
HGTD	6.4 m^2

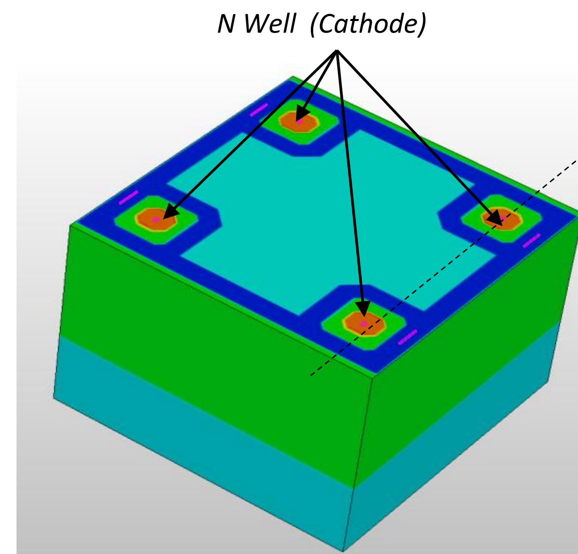
Layout of Hybrid and Monolithic

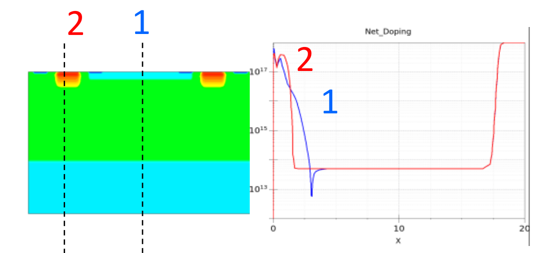
- **Hybrid and Monolithic** approach: the sensors share conceptually similar 'layouts issues':
  - Guard rings, channel stops to avoid surface currents and improve breakdown
  - Usually high voltage (100's V) are needed for biasing of sensors in hybrid approach, much less for monolithic sensors: HV biasing technique present additional challenges



*An example of Low Gain Avalanche Detector (LGAD) x-section, with **p-stop** for isolation and Junction Termination Extension (**JTE**) to increase the breakdown*

N Well (Cathode)





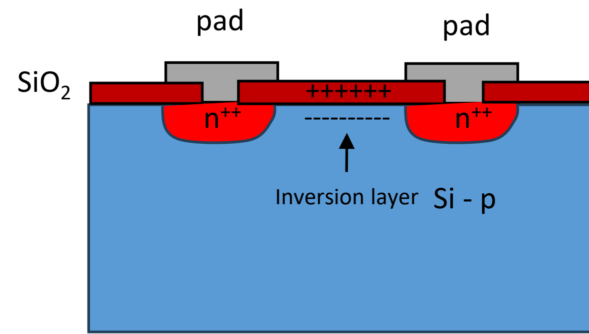
An example of a CMOS sensor on High Resistivity epitaxial x-section, with only p-stop for inter pad isolation

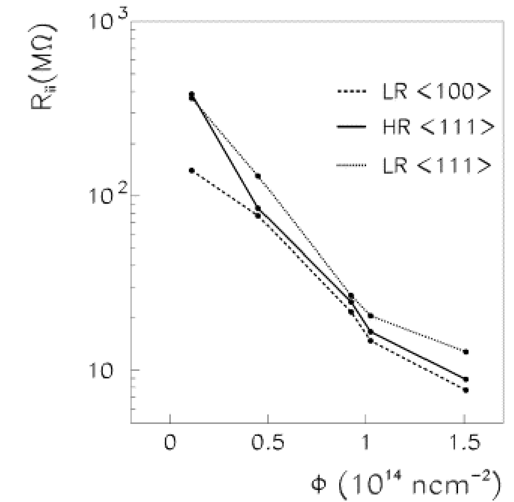
Isolation techniques

- In non-irradiated sensors (depending on the process) the dangling bonds at SiO_2-Si interface usually result in a fixed positive charge around 1e10 (Si <100>) - 1e11 (Si <111>) cm^{-2}

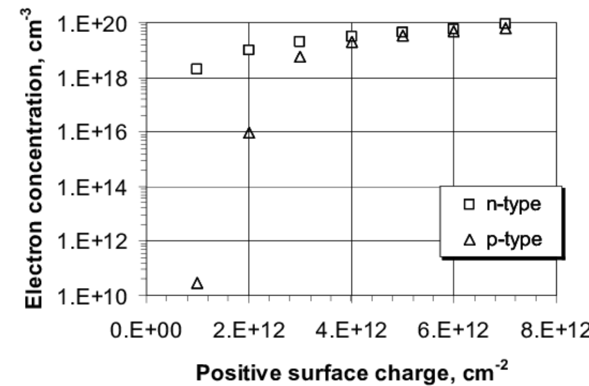
- This positive charge creates an accumulation layer of electrons in the substrate between two adjacent pads, decreasing the **interstrip resistance**

- Values up to > 1e12 cm^{-2} following ionizing irradiation further decrease the interstrip resistance





*Interstrip resistance vs non-ionising fluence**



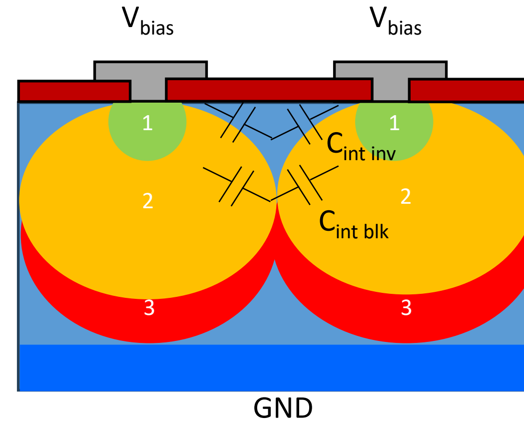
Carrier concentration vs. Oxide surface charge

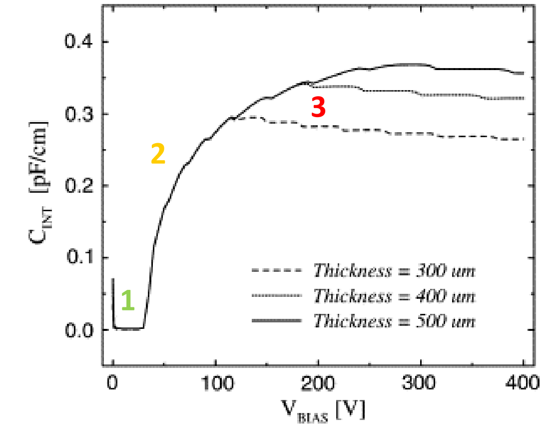
*G. Calefato, et al, s ., Comparison on radiation tolerance of 〈100〉 and 〈111〉 silicon substrates of microstrip detector,https://doi.org/10.1016/S0168-9002(01)01667-9.

Isolation techniques

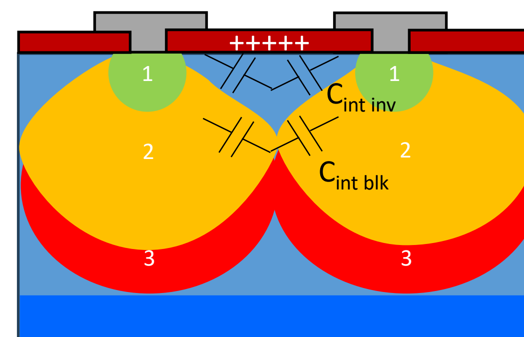
- The inversion layer also affect the **interstrip capacitance**, which affects the noise performances of the detector

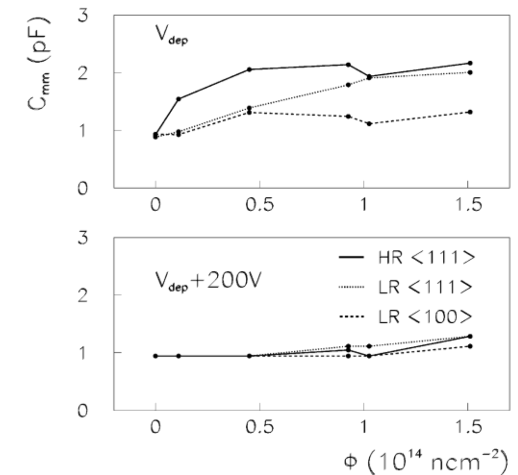
- An increased in Total Ionising Dose (TID) increases the positive charge at Si-SiO2 interface
- This might reduce the depletion of the inversion layer and increase the interstrip capacitance





D Passeri, et al. Parasitic capacitances in thick-substrate silicon microstrip detectors, https://doi.org/10.1016/S0168-9002(01)01669-2.

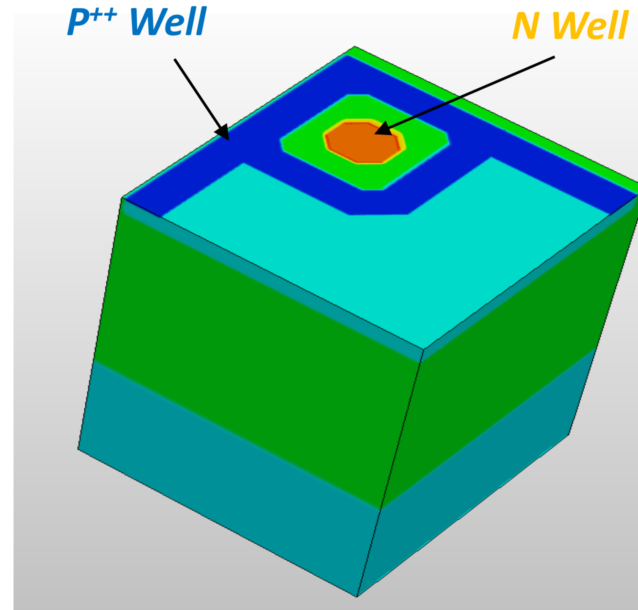


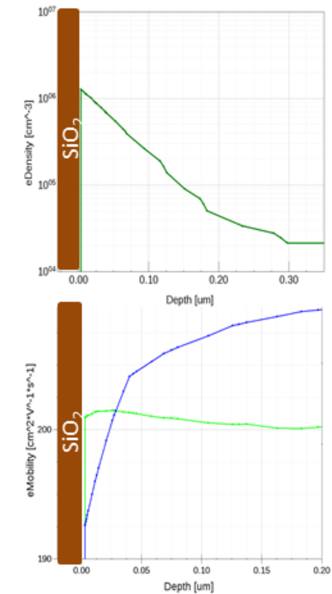


G. Calefato, et al, s ., Comparison on radiation tolerance of 〈100〉 and 〈111〉 silicon substrates of microstrip detector,https://doi.org/10.1016/S0168-9002(01)01667-9.

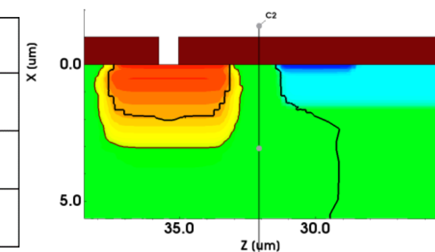
Isolation techniques

- The inversion channel might become even more important in low doped p-substrate, because of the segregation coefficient of B in SiO2 is < 1 (it is the opposite in case of n doping, like with P)





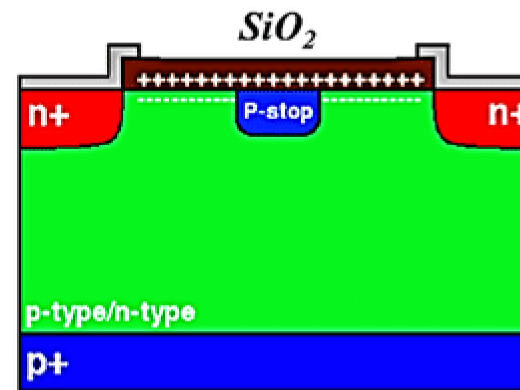
Interface Defect	Level	Concentration	σ
Acceptor	E_C-0.4 eV	40% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Acceptor	E_C-0.6 eV	60% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Donor	E_V+0.7 eV	100% of donor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV



* ***Effects of Interface Donor Trap States on Isolation Properties of Detectors Operating at High-Luminosity LHC**, DOI:* 10.1109/TNS.2017.2709815

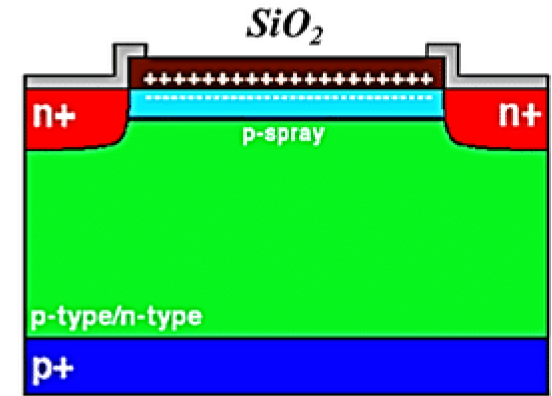
Isolation techniques

- **P-stop** and **p-spray** isolation techniques
- Breaking the inversion channel improves the isolation among cells
- The **p-stop** technique places a p^+ implant between adjacent wells
- The **p-spray** technique implements an uniform p layer between adjacent wells



*The **floating** p^+ **stop** method consists of placing a p^+ implant in between two adjacent n^+ strips*

It requires an additional mask
It might decrease the BV



*The **p-spray** method consists of having uniform p+ layer beneath the Si/SiO2 interface.*

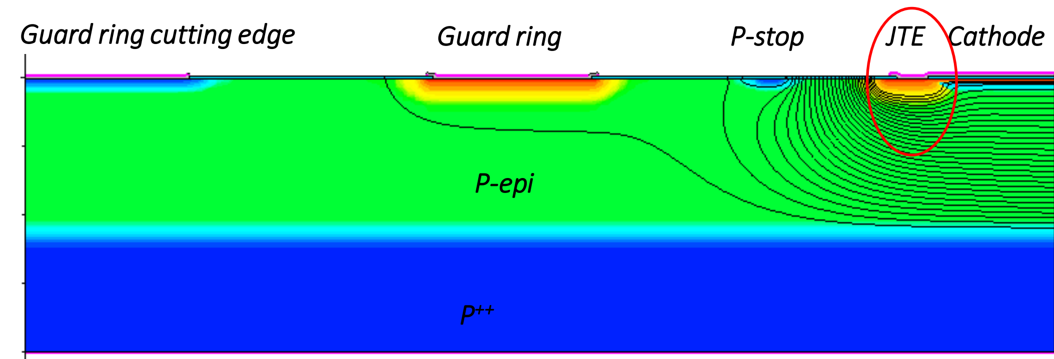
No additional mask required
It requires careful dose of doping (too low does increase BV but does not isolate, too high isolate but decreases BV)

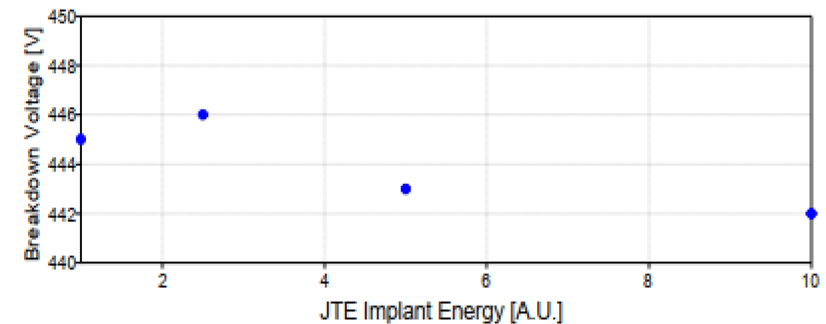
Isolation techniques

- The biasing of sensors with high voltage is required to guarantee good charge collection efficiency and short collection time

- The bias voltage is usually increased following sensors irradiation, due to loss of charge collection efficiency (reduced depletion, charge trapping – see Rad. Damage Lectures)

- Various techniques are used to reduce the likelihood of breakdown due to the high voltage operation

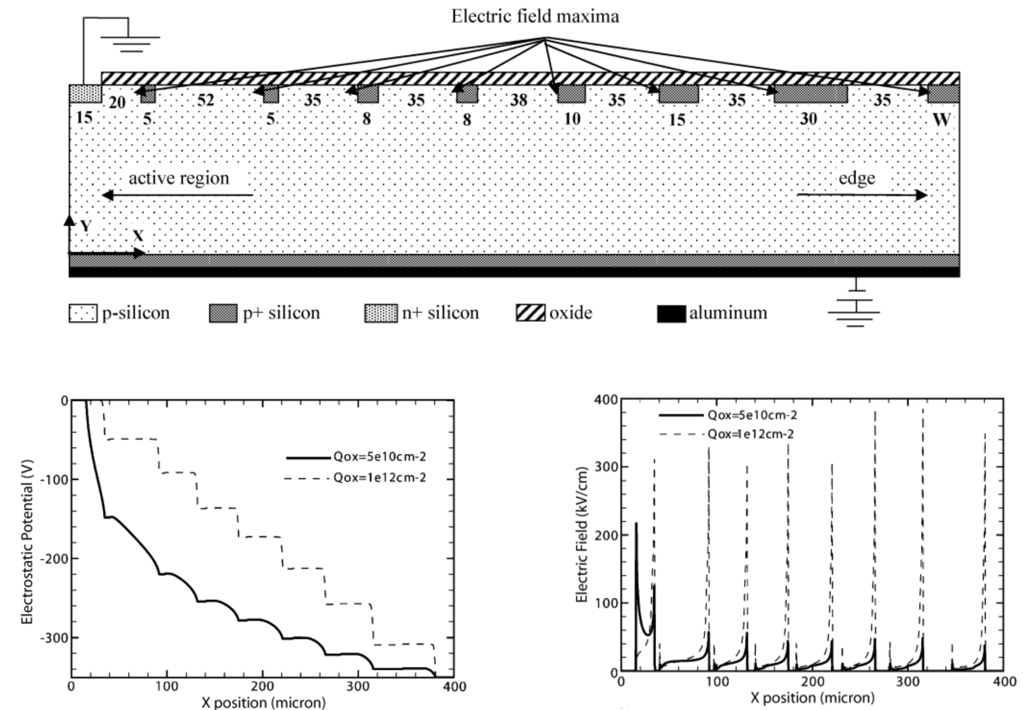




*The use of **junction termination extension** (JTE) reduces gradually the potential from the edge of the sensor, decreasing the field and increasing the breakdown*

Isolation techniques

- Guard rings are used to ensure a smooth transition from HV to ground towards the edge
- Their design need to include surface charge effects resulting from irradiation
- Multi guard rings are often employed to allow for high voltage operation
- Their use increases the design complexity and the required area



Multi guard rings *improve the high voltage operation, by decreasing the electric field at the sensor edge*

O. Koybasi, et al. "Guard Ring Simulations for n-on-p Silicon Particle Detectors," in IEEE Transactions on Nuclear Science, doi: 10.1109/TNS.2010.2063439

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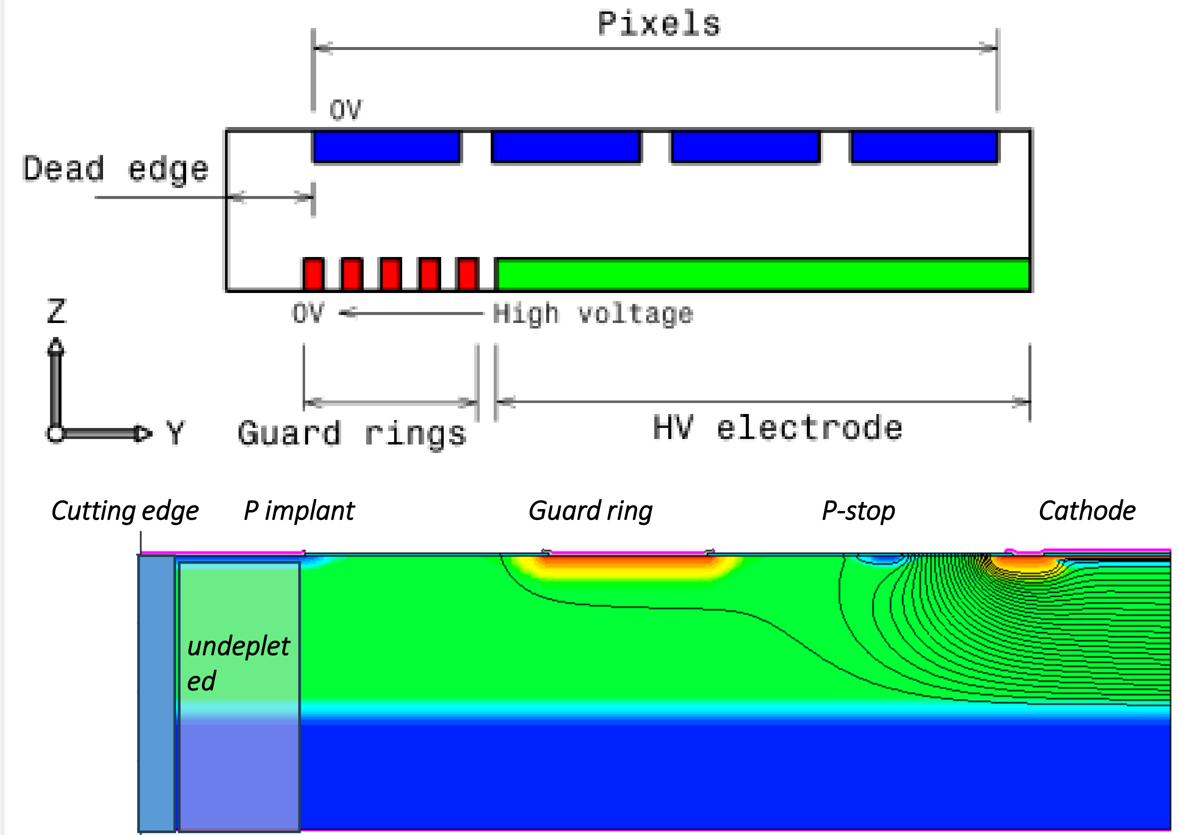
Isolation techniques

- The cutting edge of the sensor is usually damaged because of the dicing process, resulting in a very effective generation centre
- The depletion region extending laterally may reach this area, giving high leakage current
- Usually the sensor surface is terminated with a wide p^+ implant to prevent this by making the region underneath undepleted



Guard rings are used also to avoid the SC region reaching the cutting edge of the sensor

Simulation of guard ring influence on the performance of ATLAS pixel detectors for inner layer replacement DOI: 10.1088/1748-0221/4/03/P03025

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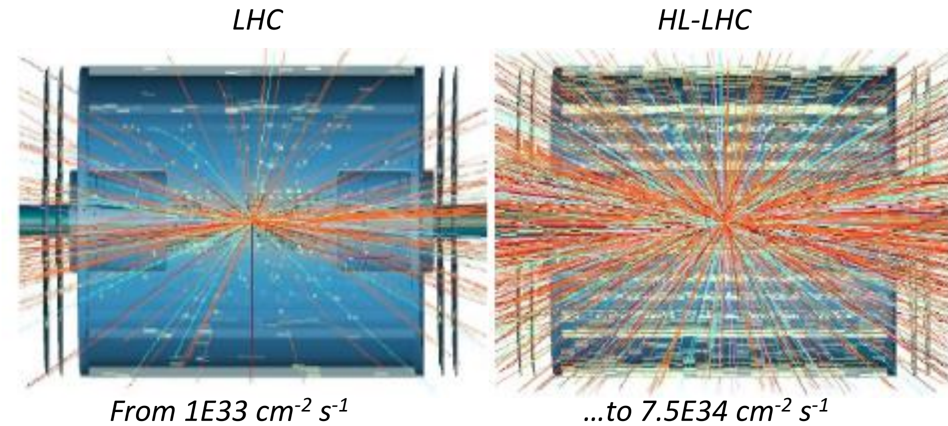
HV biasing

- Current ATLAS SCT uses independent powering for the 4088 detector modules. Each sensor has its own independent HV bias line.
- 'ideal' solution:
  - High Redundancy
  - Individual enabling or disabling of sensors and current monitoring
- The increased number of sensors in the Upgraded Tracker (>10 k modules in barrel upgrade vs. ~2 k in present barrel) implies a trade off among material budget, complexity of power distribution and number of HV bias lines.



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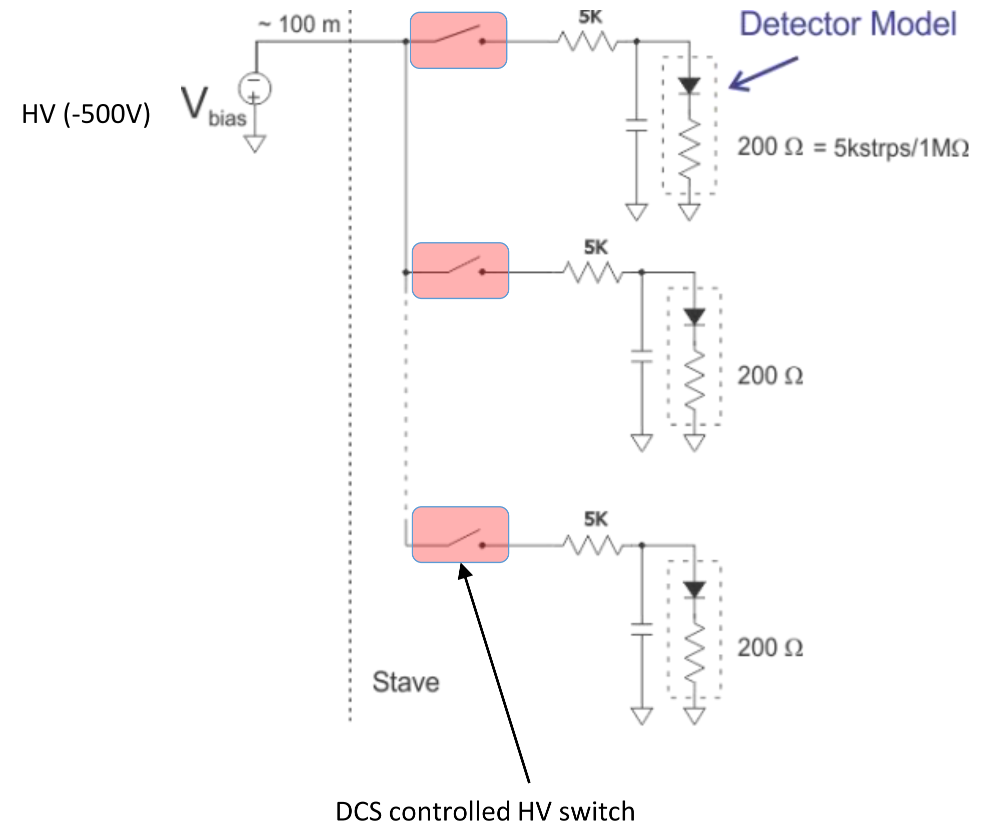
HV biasing

- Use single (or more) HV bus to bias in parallel all sensors and use one HV switch for each sensor to disable malfunctioning sensors: High Voltage Multiplexing '**HVMUX**'
- The HV switch is DCS controlled, with control signals provided by custom ASIC (Autonomous Monitor And Control, AMAC)



HV biasing

- High Voltage switches strip detector requirements:
  Rated to 500V plus a safety margin

- Must be radiation hard, nominal maximum expected ~1×10^{15} n_{eq}/cm^2 , ~ 30Mrad (Si) for strip end cap. Multiply by 1.5 to include safety margin

- On-state impedance R_{on} << 1kΩ // I_{on} ~ 10mA (for irradiated strip sensors)

- Off-state impedance R_{off} >> 1GΩ // I_{lkg} << I_{sens}

- Must be unaffected by magnetic field

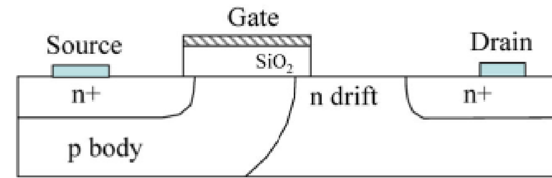
- Must maintain satisfactory performance at -30° C
- Must be small (mass/area constraint) and cheap (around 1E4 needed)

Partial list of investigated HV devices

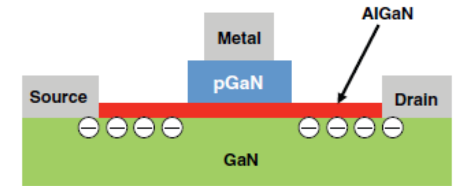
Device	Type	Voltage	Result
Crystalonic 2N6449	Si JFET	300V	FAILED
Interfet 2N6449	Si JFET	300V	FAILED
IXYS CPC5603	Si MOSFET	410V	FAILED
ROHM R6006ANX	Si MOSFET	600V	FAILED
Infineon IPA50R950CE	Si MOSFET	500V	FAILED
Semisouth SJEP170	SiC JFET	1700V	PASS – N.A.
USCi UJN1205	SiC JFET	1200V	FAILED
CREE CPMF-1200	SiC MOSFET	1200V	FAILED
ROHM S2403	SiC MOSFET	1700V	FAILED
GeneSiC GA04JT17	SiC BJT	1700V	FAILED
TranSiC FSICBH057A120	SiC BJT	1200V	FAILED
Transphorm TPH2006C	GaN JFET	600V	FAILED
EPC2012	GaN JFET	200V	PASS
GS66502B	**GaNFET**	**650V**	**PASS**
PGA26E19BV	**GaNFET**	**600V**	**PASS**

HV biasing

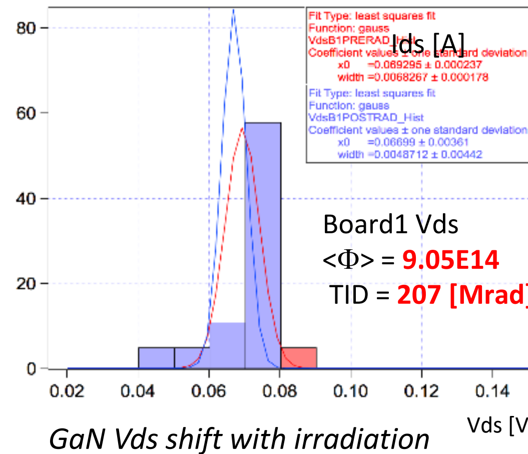
- Typical Si HV MOSFET use regions of low doping to increase high voltage capabilities: this affects their radiation hardness
- Non-ionizing and ionizing irradiation test results of GaN FET devices indicate very high radiation hardness



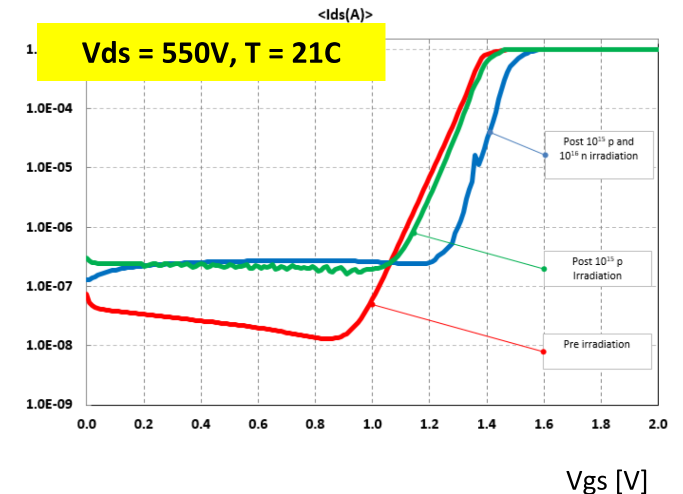
A Lateral Double-Diffused MOS (LDMOS). A long drift region of lower doping reduces the electric field



Example Xsection of a HEMT E. GaN FET. Strain-induced polarization at interface forms a 2DEG



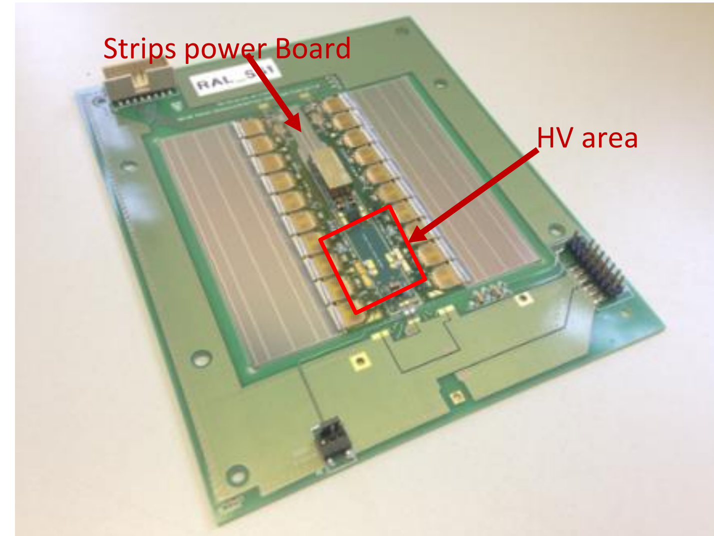
GaN Vds shift with irradiation



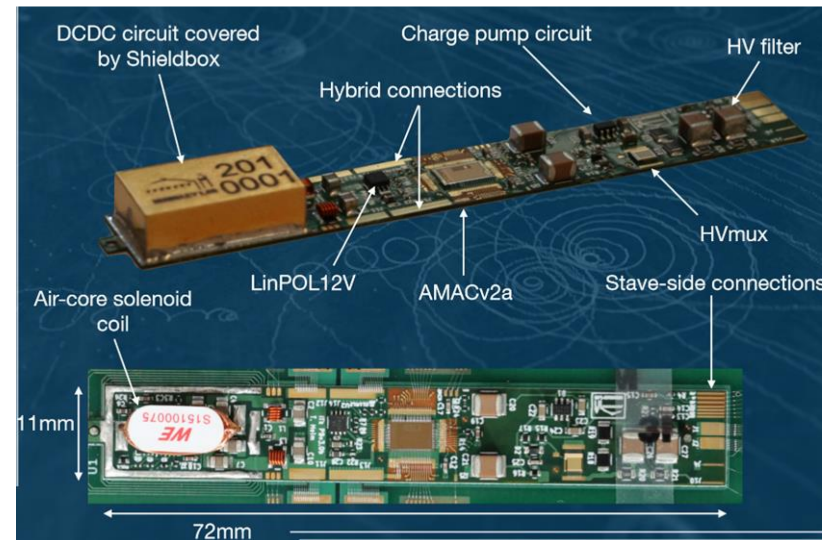
*Additional test performed on 18 devices Total **p** fluence **1.0E15, ~**TID **200Mrad(GaN)** Total n fluence **1.0E16***

HV biasing

- The HVMUX sits on the lower side of a flexi power board (PB)
- The PB final version incorporates power control and HVMUX elements in the AMAC ASIC



A barrel short strip module with two hybrids and one powerboard with HVMUX

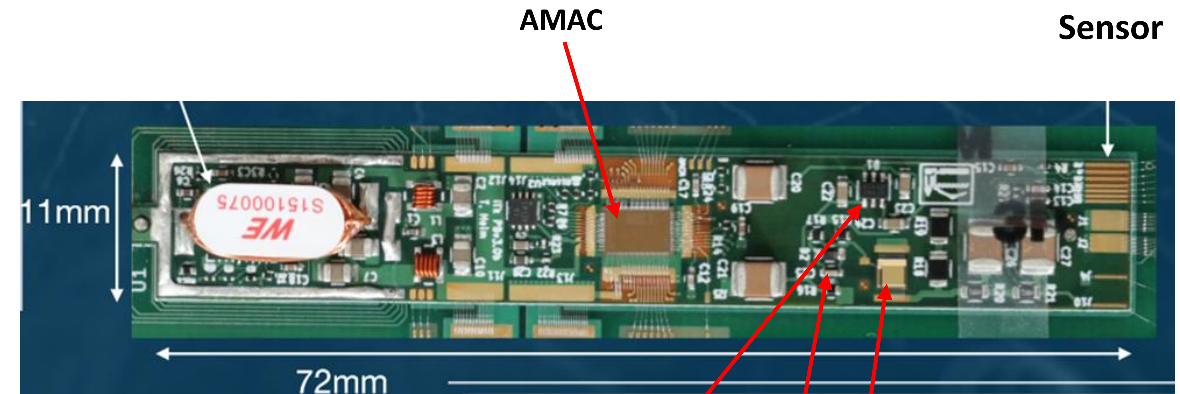


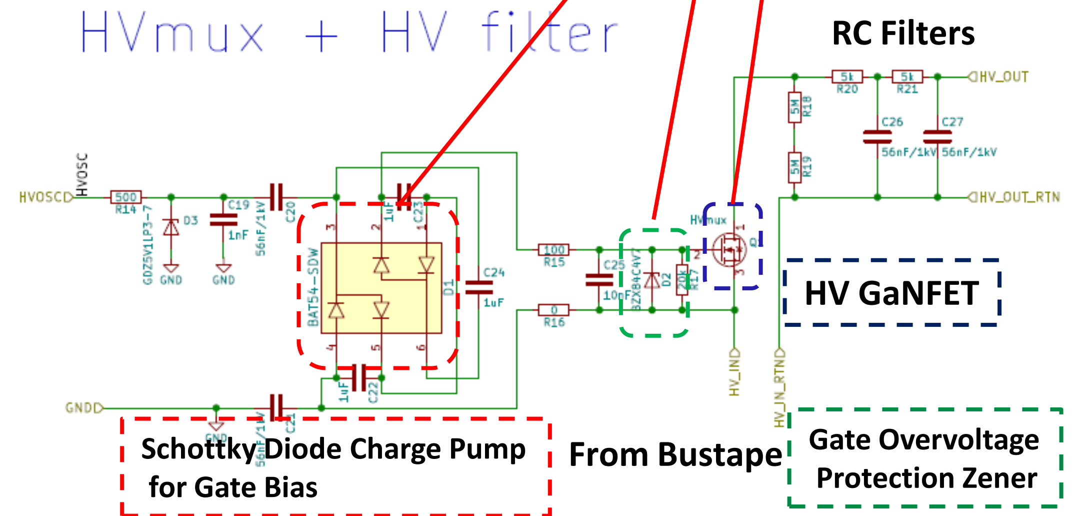
Power board v3.0b

HV biasing

- A charge pump voltage multiplier driven by AC drives the gate of a GaN FET, rated for HV
- Investigated stacked solutions demonstrated switching voltages > 1kV
- Up to 600V with the implemented ItK solution
- Baseline solution for HV bias of ItK strips

LBNL V3 PowerBoard with HV Mux





Villani, E.G., Technical Design Report for the ATLAS Inner Tracker Strip Detector, CERN-LHCC-2017-005, ATLAS-TDR-025, https://cds.cern.ch/record/2257755

Thank you

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Circuits and Layouts II Summary

- Hybrid and Monolithic technology pros and cons
- Common isolation techniques
- Example of ItK Strips HV biasing