Circuits and Layouts

I

Overview

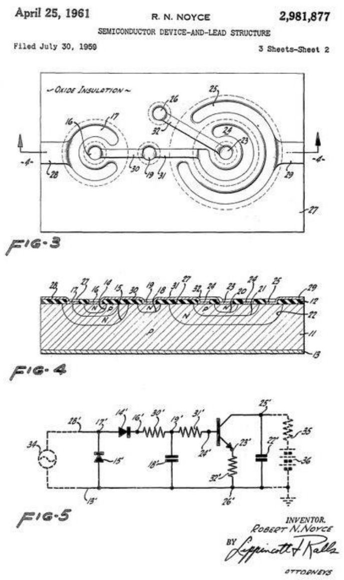
- **Introduction, definitions**
- **Layout and interconnects in IC technology**
- **Transistor MOS layouts**
- **Passive components layouts**

Introduction

- IC (integrated circuits) single silicon chip that includes active and passive interconnected devices to implement complex operations (analogue, digital)

- Planar technology: the processing steps are implemented in a thin layer of the surface of the chip

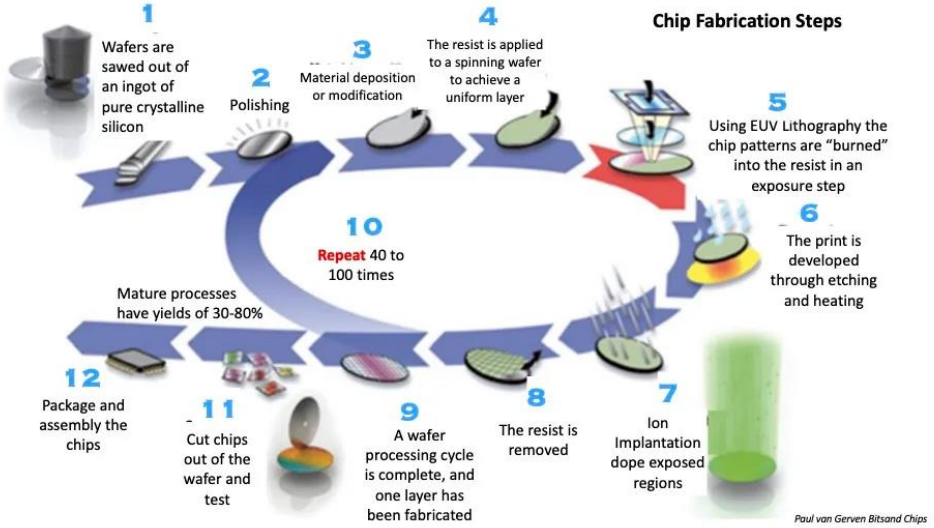
- Fabrication of chip is an extremely complex process, requiring several steps of atomic precision


April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

First planar IC patent, 1961


Chip Fabrication Steps

1 Wafers are sawed out of an ingot of pure crystalline silicon

2 Polishing

3 Material deposition or modification

4 The resist is applied to a spinning wafer to achieve a uniform layer

5 Using EUV Lithography the chip patterns are "burned" into the resist in an exposure step

6 The print is developed through etching and heating

7 Ion Implantation dope exposed regions

8 The resist is removed

9 A wafer processing cycle is complete, and one layer has been fabricated

10 Repeat 40 to 100 times

11 Cut chips out of the wafer and test

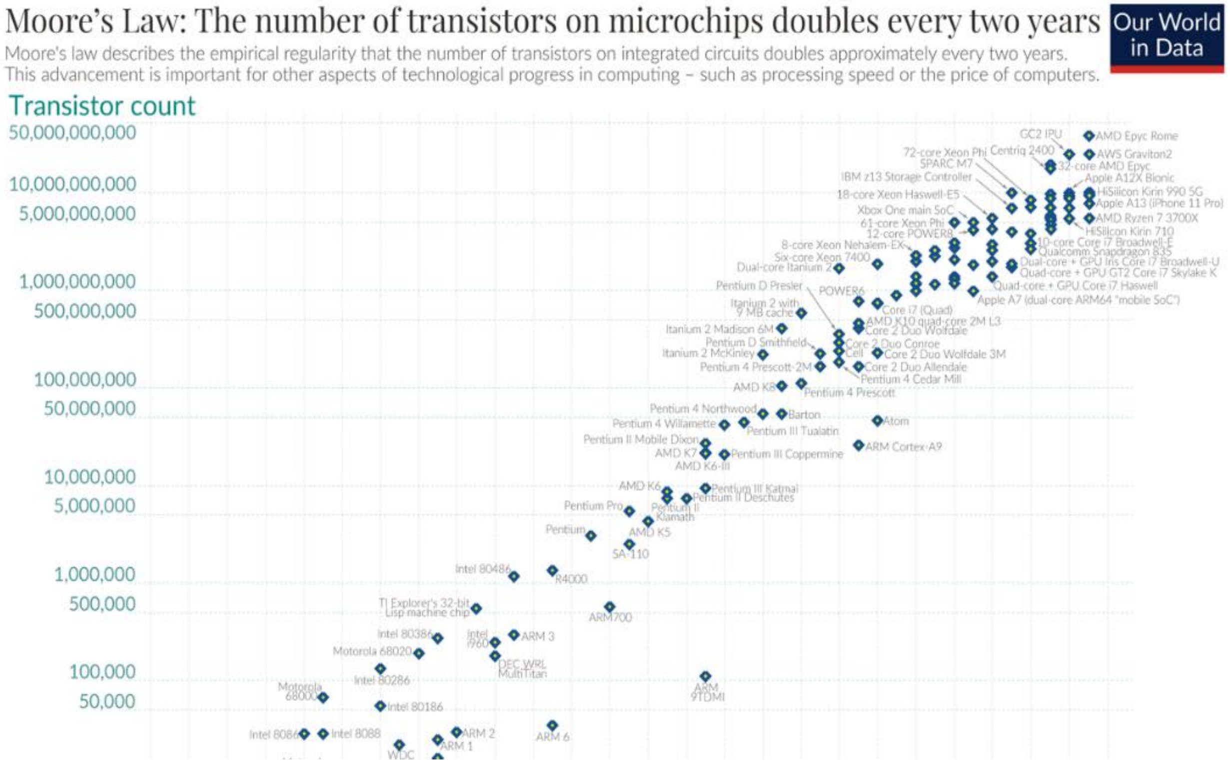
12 Package and assembly the chips

Mature processes have yields of 30-80%

Paul van Gerven Bitsand Chips

Layout and interconnects

- **Device scaling** leads to cost reduction and increased speed per transistor
- However, due to the high number of transistors on chip, **layout optimization** at chip level has become as important as transistors fabrication
- **Interconnecting** the devices has become the bottleneck for IC performances

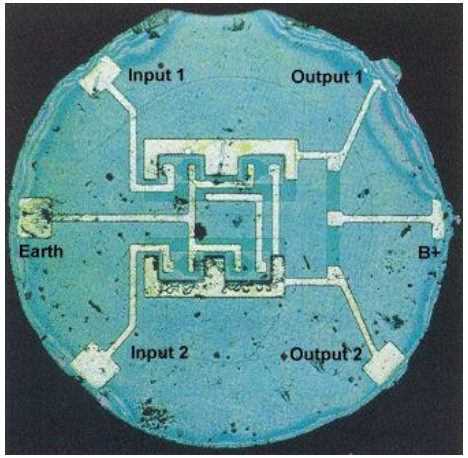


Moore's Law: The number of transistors on microchips doubles every two years

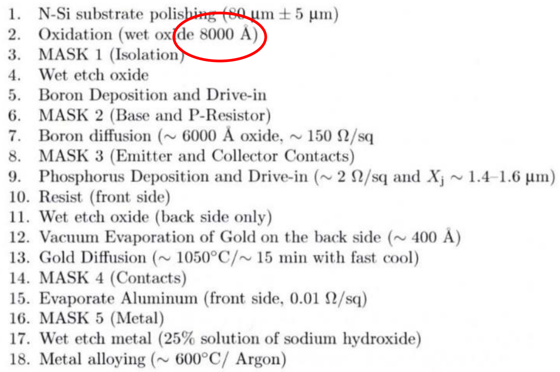
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Layouts and interconnects

- The processing steps involved in fabricating transistors and their immediate interconnect is called **Front-End-Of-Line** (**FEOL**)
- That includes implantation, oxide growth, diffusion and first metal layer deposition
- Interconnecting all the devices together with higher metals is the **Back-End-Of-Line** (**BEOL**)
- As the number of transistors on chips grew, it became impossible to make all connections in a single layer
- Added additional vertical levels of interconnects
- Simpler IC might have a few metal layers, complex ICs exceed 10 layers

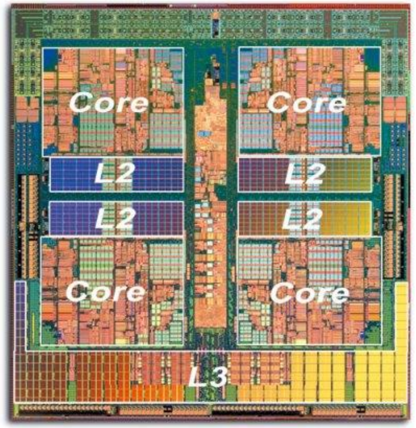


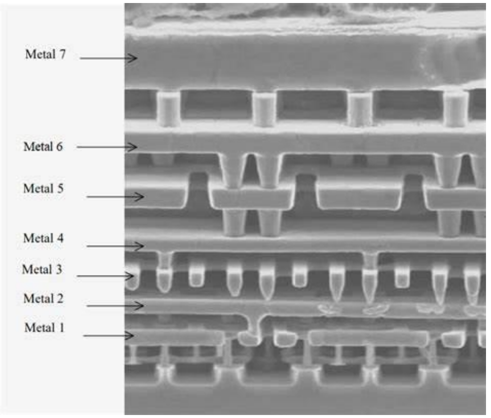
First commercial IC, Fairchild Semiconductor, 1961. Flip-Flop



1. N-Si substrate polishing (80 μm ± 5 μm)
2. Oxidation (wet oxide 8000 Å)
3. MASK 1 (Isolation)
4. Wet etch oxide
5. Boron Deposition and Drive-in
6. MASK 2 (Base and P-Resistor)
7. Boron diffusion (~ 6000 Å oxide, ~ 150 Ω/sq
8. MASK 3 (Emitter and Collector Contacts)
9. Phosphorus Deposition and Drive-in (~ 2 Ω/sq and X_j ~ 1.4–1.6 μm)
10. Resist (front side)
11. Wet etch oxide (back side only)
12. Vacuum Evaporation of Gold on the back side (~ 400 Å)
13. Gold Diffusion (~ 1050°C/~ 15 min with fast cool)
14. MASK 4 (Contacts)
15. Evaporate Aluminum (front side, 0.01 Ω/sq)
16. MASK 5 (Metal)
17. Wet etch metal (25% solution of sodium hydroxide)
18. Metal alloying (~ 600°C/ Argon)

Original Planar process flow (from Fairchild Semiconductor)

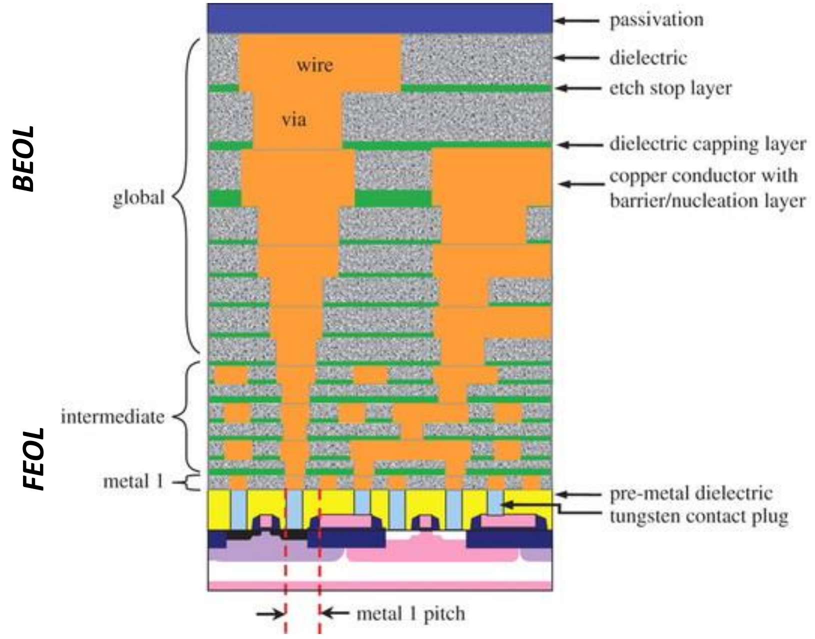


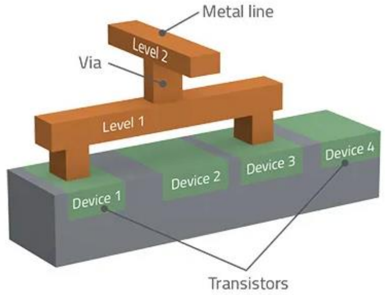


Layout and interconnects

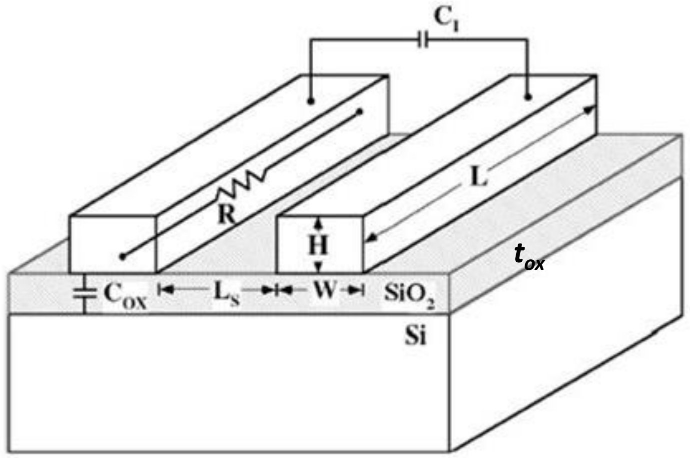
- Various levels of interconnects are present in modern ICs:
  - **Metal 1**, for short local interconnects
  - **Intermediate**, to connect devices within blocks
  - **Global interconnects**, for long, low resistivity connections, including power, grounds

- Various levels are connected by vias and separated by dielectrics





Layout and interconnects



$$R = \rho \frac{L}{WH}$$

$$C_{ox} = \varepsilon_{ox}\varepsilon_o \frac{WL}{t_{ox}}$$

$$C_I = \varepsilon_{ox}\varepsilon_o \frac{HL}{L_s}$$

$$C_{tot} \cong C_I + C_{ox}$$

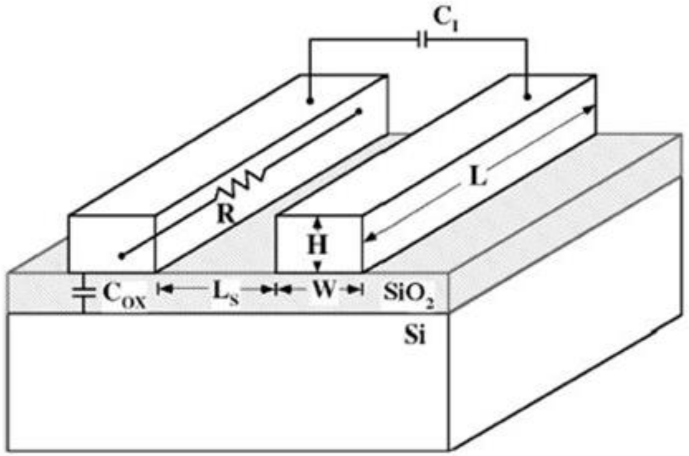
$$\tau_I \cong \varepsilon_{ox}\varepsilon_o \rho \frac{L^2}{WH}\left(\frac{W}{t_{ox}} + \frac{H}{L_s}\right)$$

- **Interconnects** and their **layouts** are of increasing importance as the feature size of circuit elements become smaller

- **Delay times** of interconnect transmission line

Layout and interconnects

- As the technology size decreases:
  - W, L_s and H decrease
  - t_{ox} decrease at ~ the same rate as W and H i.e. by a scaling factor λ
  - The distance L for local interconnect decreases as the sized of devices gets smaller (~ λ)
  - Time delay τ_{iloc} **for local interconnect** remains ~ constant or slightly decreases

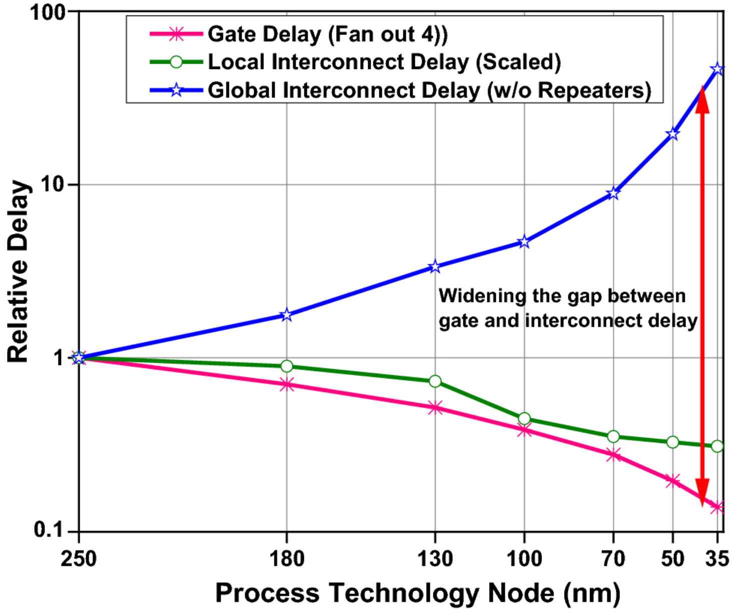


$$\tau_i \cong \varepsilon_{ox}\varepsilon_o \rho \frac{L^2}{WH}\left(\frac{W}{t_{ox}} + \frac{H}{L_s}\right)$$

$$\tau_{iloc} \propto \varepsilon_{ox}\varepsilon_o \rho \frac{\lambda^2}{\lambda^2}$$

Layout and interconnects

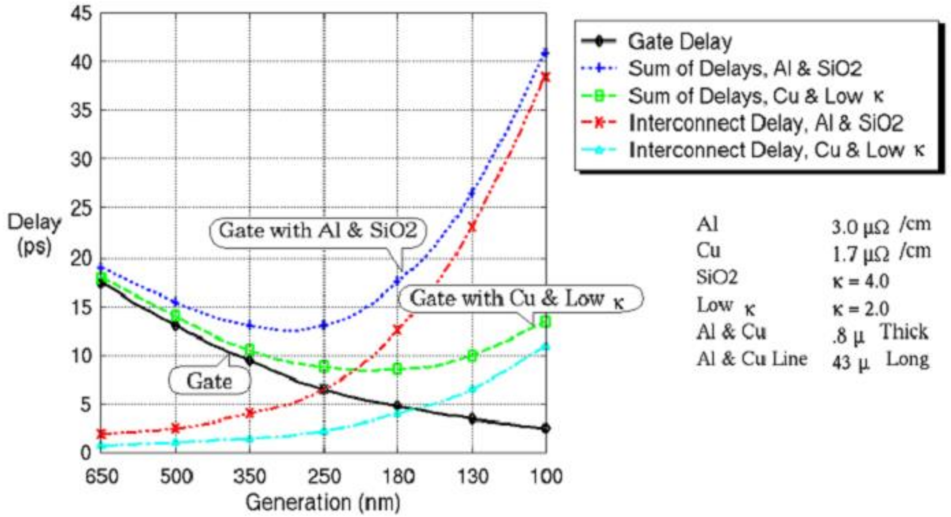
- As the technology size decreases:
  - Area S of the die tends to increase
  - Length of global interconnect increases √S
  - Time delay τ_{igIo} for **global interconnect** tends to increase



$$\tau_{igIo} \cong \varepsilon_{ox}\varepsilon_{o}\rho\frac{S}{\lambda^2}$$

Layout and interconnects

- Time delay τ_{igIo} for **global interconnect** tends to increase as the technology size decreases
- **Different materials** can be used for the interconnect to reduce ρ and ε



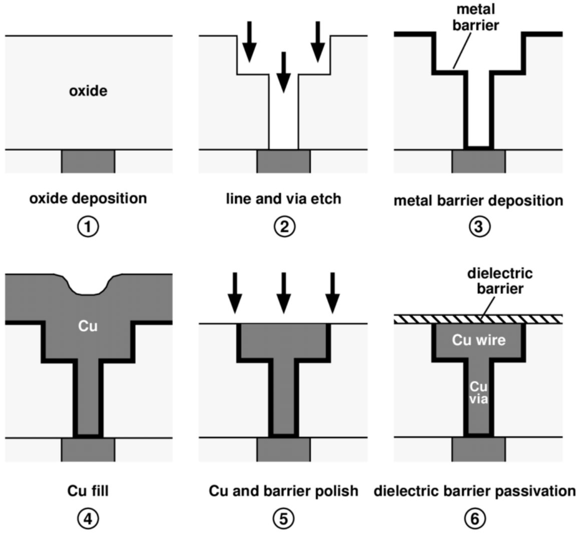
The global interconnect delay vs. technology node for standard and advanced materials

$$\tau_{igIo} \cong \varepsilon_{ox}\varepsilon_{o}\rho\frac{S}{\lambda^2}$$

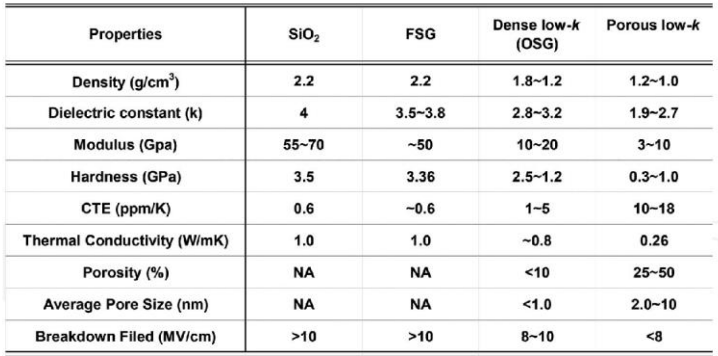
Layout and interconnects

- Reducing ρ has been achieved by using Cu instead of Al (**Damascene*** process)
- Reduce ε is more challenging: **low-K** dielectrics can be obtained using F and other dopants but resulting dielectric show poorer quality
- **Air gaps** are also used (ε =1) in some locations in <10 nm nodes

from ancient sword making technique in **Damascus, Syria*



Dual Damascene process. An additional metal barrier (W) is deposited first to avoid Cu contamination of Si. Cu deposited by electroplating. CMP is needed as Cu does not plasma etch[1].



Properties	SiO_2	FSG	Dense low-*k* (OSG)	Porous low-*k*
Density (g/cm^3)	2.2	2.2	1.8~1.2	1.2~1.0
Dielectric constant (k)	4	3.5~3.8	2.8~3.2	1.9~2.7
Modulus (Gpa)	55~70	~50	10~20	3~10
Hardness (GPa)	3.5	3.36	2.5~1.2	0.3~1.0
CTE (ppm/K)	0.6	~0.6	1~5	10~18
Thermal Conductivity (W/mK)	1.0	1.0	~0.8	0.26
Porosity (%)	NA	NA	<10	25~50
Average Pore Size (nm)	NA	NA	<1.0	2.0~10
Breakdown Filed (MV/cm)	>10	>10	8~10	<8

Low- dielectrics have been used for < 100 nm nodes. Reliability issues with very low k-dielectrics

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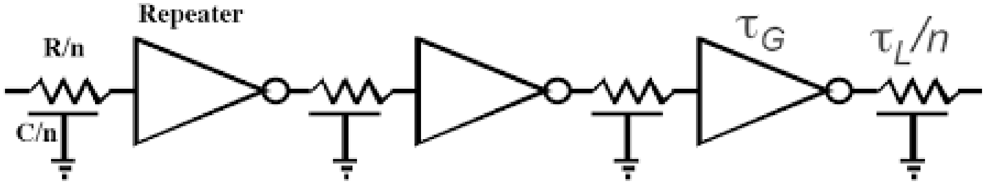
[1] *C. K. Hu and J. M. E. Harper, Copper Interconnections and Reliability, Mater. Chem. Phys., vol. 52, p. 5-16, 1998.*

Layout and interconnects

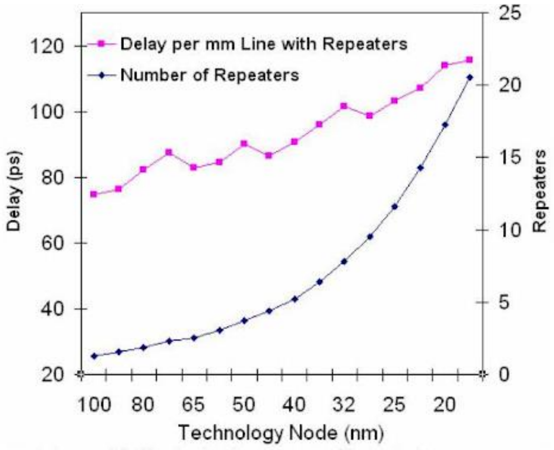
- Another way to reduce the interconnect delay is to use pass transistors (or repeaters)
- A long interconnect L is broken into n shorter lines, with the delay of each section reduced quadratically
- A small repeaters' delay τ_g reduces the global delay τ_{igIo}
- The repeater solution increases the occupied area and the power consumption



*A long interconnect line **L** is broken into **n** segments, each of length **L/n***

$$\tau_{igIo} \cong \varepsilon_{ox}\varepsilon_o\rho\frac{L^2}{\lambda^2} \qquad \tau_{gIo} \cong \varepsilon_{ox}\varepsilon_o\rho\frac{1}{\lambda^2}\left(\frac{L^2}{n^2}\right)n + n\tau_g$$

$$n\tau_g < \varepsilon_{ox}\varepsilon_o\rho\frac{1}{\lambda^2}L^2\left(1-\frac{1}{n}\right)$$



Global interconnection delay and repeaters vs. node

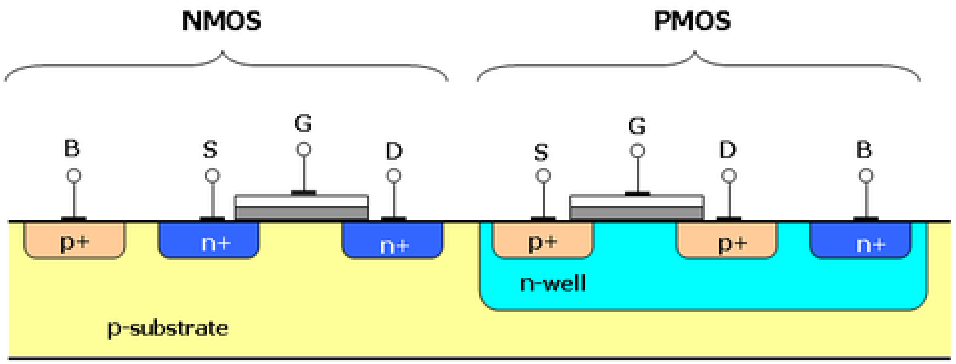
(source: http://www.monolithic3d.com/3d-ic-edge1.html)

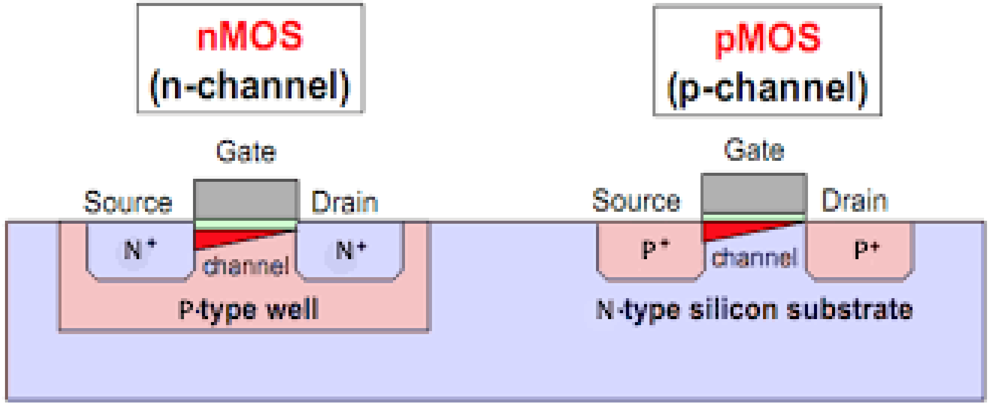
MOS transistor layout

- Very often standard silicon wafers are P type and devices, including MOS transistors, are implemented in them

- This stems from the fact that NMOS are intrinsically faster than PMOS (e^- mobility higher than h^+)

- Fastest NMOS is obtained from high resistivity (low doping) P substrate rather than lower resistivity (higher doping) P well

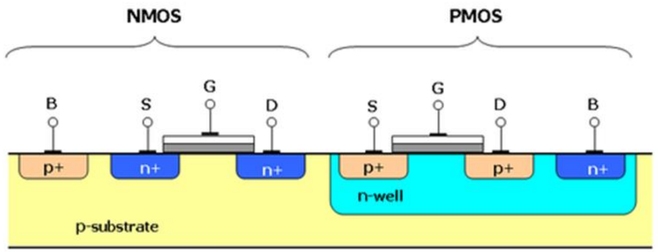


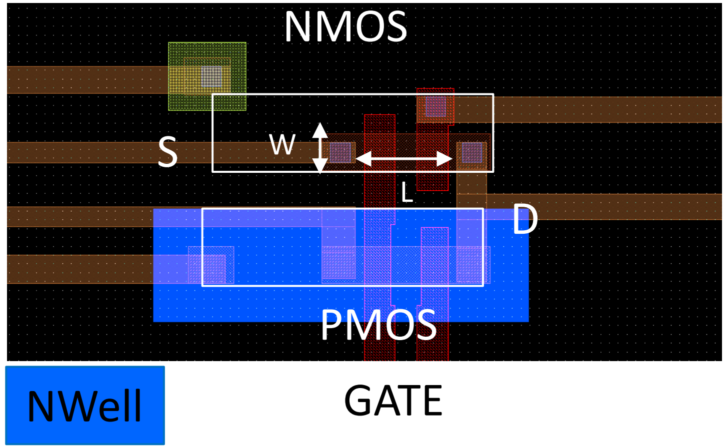


MOS transistor layout

- In **digital circuits**, the transistors are normally designed with minimum size, to increase density of functions/storage /area

- In **analog circuits** a large **form factor** β = W/L is required, to increase the transcoductance g_m





$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

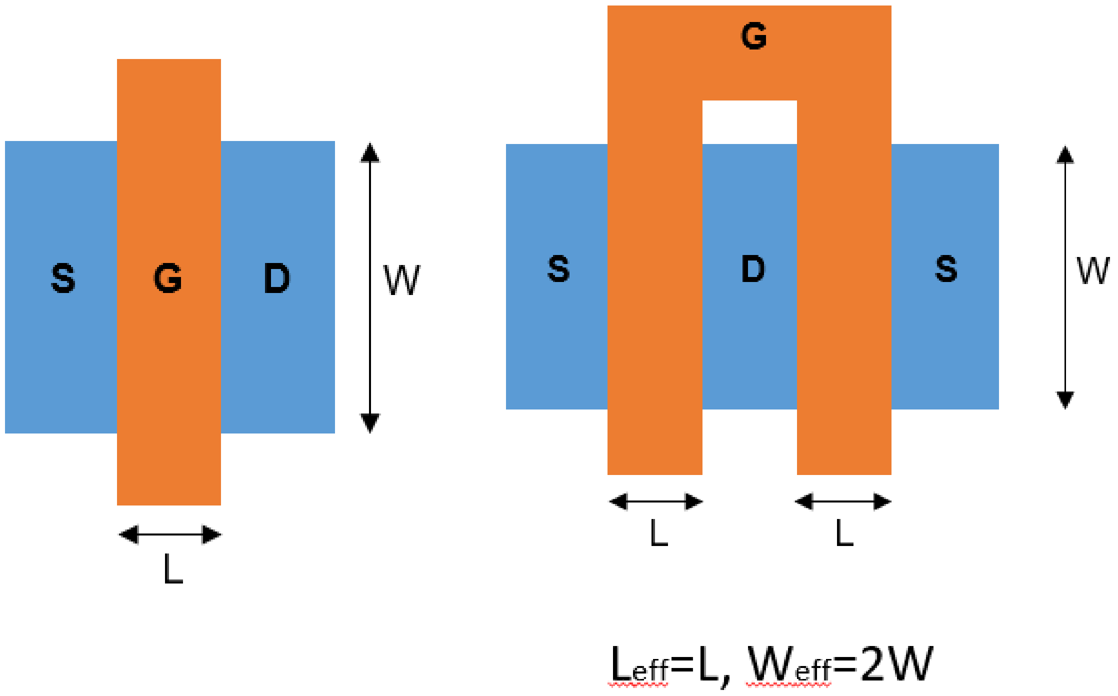
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu C_o \frac{W}{L}\left(V_{GS} - V_T\right)$$

MOS transistor layout

- In the layout of **analog transistors** the form factor is crucial as it determines g_m (straight structures preferable)

- However, a big value of W might increase Gate resistance/capacitance

- Special layout issues in analog design:
  - multi-finger structure



$L_{eff}=L$, $W_{eff}=2W$

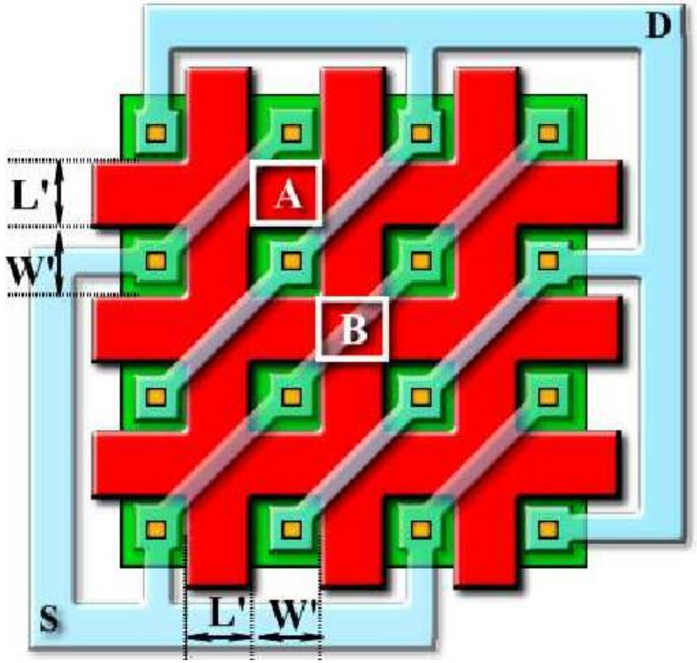
Single finger

Two fingers: W are summed
Capacitance x 2
Resistance /2
To first approx., RC remains the same as in single finger

MOS transistor layout

- Multi finger structures decrease the Gate resistance but increase the parasitic effects (drain-gate coupling, gate to substrate)

- Special structure (Waffle structure) used for RF CMOS applications



$$\left(\frac{W}{L}\right)_{\mathrm{WAFFLE}} = N_A \frac{W'}{L'} + N_B (0.55871)$$

$$N_A = N_R \cdot (N_C + 1) + N_C \cdot (N_R + 1)$$

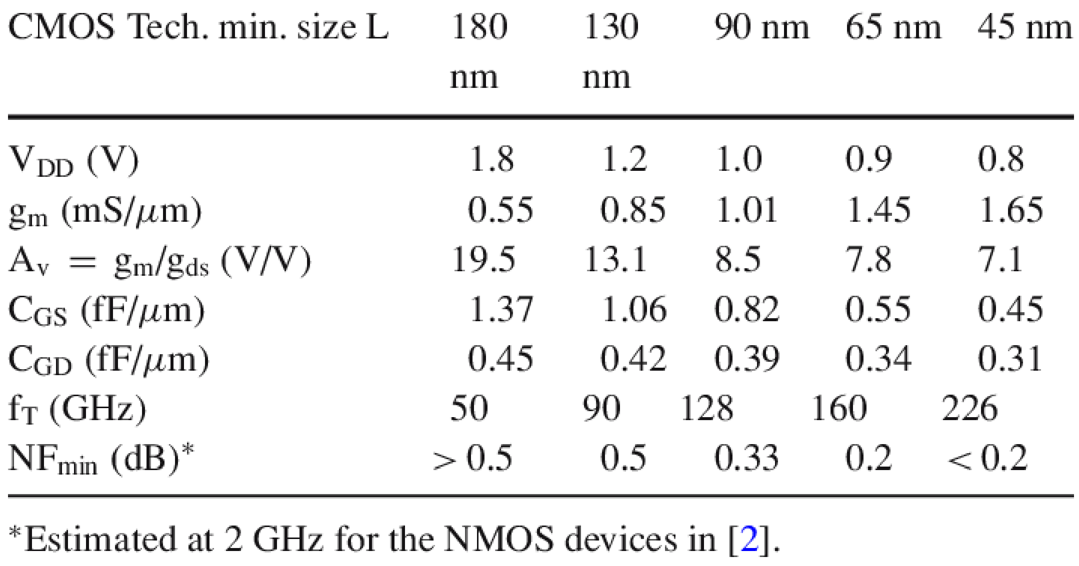
$$N_B = N_R \cdot N_C$$

P. Vacula 1,2, M. Husák, M. 2013
Waffle MOS channel aspect ratio calculation with Schwarz-Christoffel Transformation

MOS transistor layout

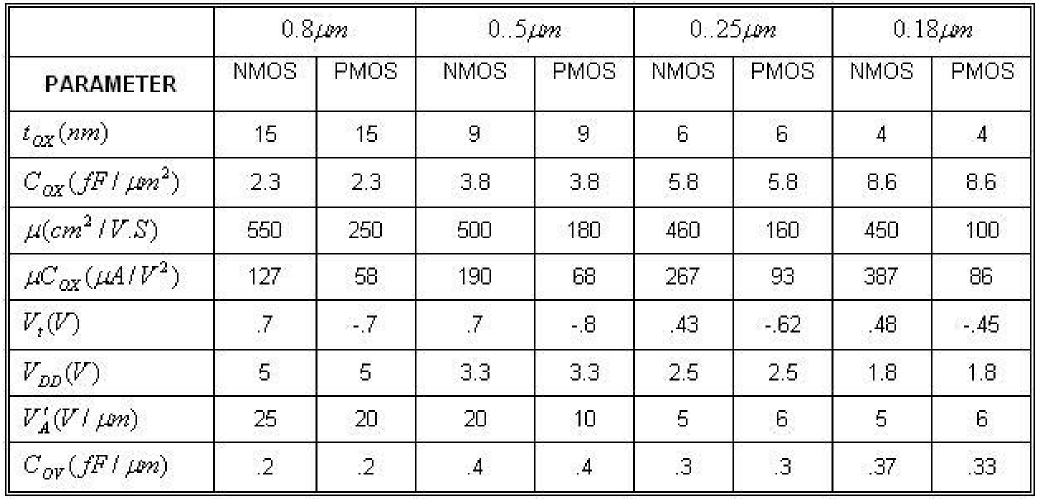
- Typical figures of CMOS process vs. size

- Scaling down does not imply better device characteristics per se



CMOS Tech. min. size L	180 nm	130 nm	90 nm	65 nm	45 nm
V_{DD} (V)	1.8	1.2	1.0	0.9	0.8
g_m (mS/μm)	0.55	0.85	1.01	1.45	1.65
$A_v = g_m/g_{ds}$ (V/V)	19.5	13.1	8.5	7.8	7.1
C_{GS} (fF/μm)	1.37	1.06	0.82	0.55	0.45
C_{GD} (fF/μm)	0.45	0.42	0.39	0.34	0.31
f_T (GHz)	50	90	128	160	226
NF_{min} (dB)*	> 0.5	0.5	0.33	0.2	< 0.2

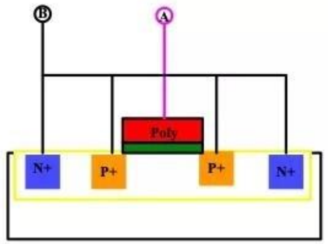
*Estimated at 2 GHz for the NMOS devices in [2].



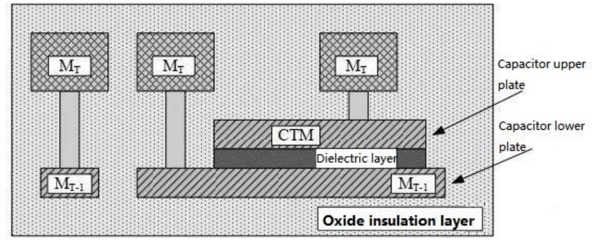
	0.8μm		0..5μm		0..25μm		0.18μm	
PARAMETER	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$t_{ox}(nm)$	15	15	9	9	6	6	4	4
$C_{ox}(fF/\mu m^2)$	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6
$\mu(cm^2/V.S)$	550	250	500	180	460	160	450	100
$\mu C_{ox}(\mu A/V^2)$	127	58	190	68	267	93	387	86
$V_t(V)$	.7	-.7	.7	-.8	.43	-.62	.48	-.45
$V_{DD}(V)$	5	5	3.3	3.3	2.5	2.5	1.8	1.8
$V'_A(V/\mu m)$	25	20	20	10	5	6	5	6
$C_{ov}(fF/\mu m)$	.2	.2	.4	.4	.3	.3	.37	.33

Passive components layout

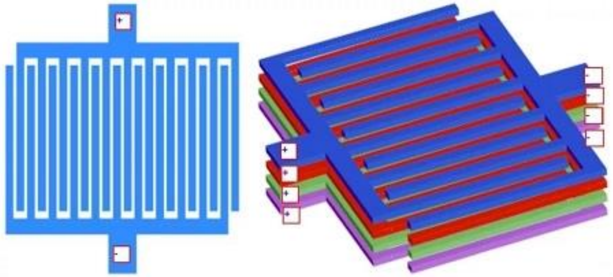
- Integrated **Capacitors** are normally obtained by structures close to the silicon substrate
- Three type of capacitors:
  - **MOS** (Metal Oxide Semiconductor)
  - **MiM** (Metal Insulator Metal)
  - **MoM** (Metal Oxide Metal) use interdigitated capacitors formed by metal layers



***MOS** capacitor: capacitance values changes with voltage, small area*



***MIM** use different layers of metal and interposed dielectric to form a capacitor. Similar to plate capacitor, good stability but require additional masks*



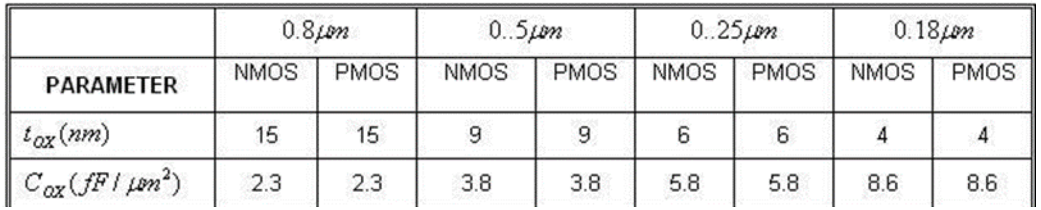
***MOM** use interdigitated capacitors formed by metal connections, placed in close proximity – preferred choice for advanced CMOS, also no additional mask required*

Passive components layout

- Typical values of capacitance

- Typical dielectric layers are SiO_2 or Si_3N_4

- Use of high k materials is common in more advanced CMOS technologies

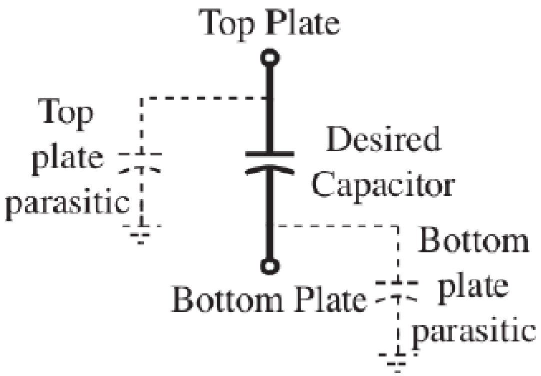


	0.8μm		0..5μm		0..25μm		0.18μm	
PARAMETER	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$t_{ox}(nm)$	15	15	9	9	6	6	4	4
$C_{ox}(fF/\mu m^2)$	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$t_{ox} = 4\ nm$$

$$C = 8.6\ fF/\mu m^2$$



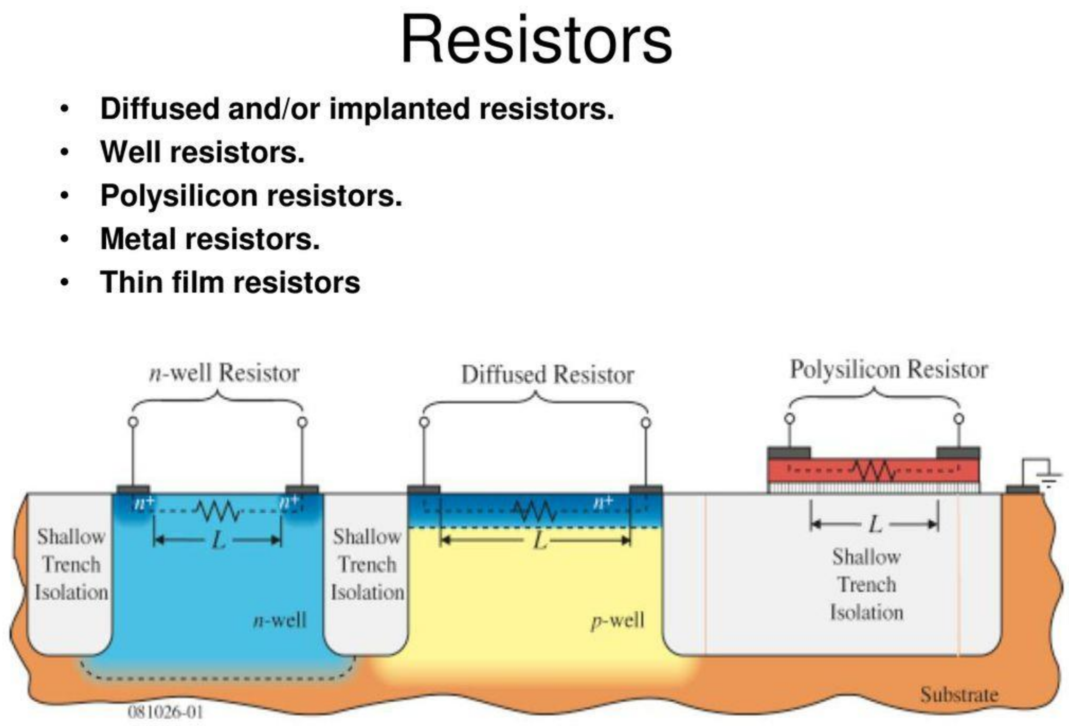
MIM/MOMs parasitic

$$C_{t,p} = 0.1\ \%\ C$$
$$C_{b,p} = 1\ \%\ C$$

Passive components layout

- Integrated **Resistors** are normally obtained by thin strips of resistive layers

- Insulation from surrounding achieved by oxide layers or reversed biased junctions



Resistors

- **Diffused and/or implanted resistors.**
- **Well resistors.**
- **Polysilicon resistors.**
- **Metal resistors.**
- **Thin film resistors**

$Nwell:\ \rho_{\blacksquare} \sim 1\ k\Omega/\blacksquare$

$Poly:\ \rho_{\blacksquare} \sim 10\ \Omega/\blacksquare$

$Metallic:\ \rho_{\blacksquare} \sim 0.1\ \Omega/\blacksquare$ $R = \rho_{\blacksquare}\frac{L}{W}$

Passive components layout

- Integrated **Inductors** are obtained by using different layouts of metal layers
- Used in some RF CMOS applications

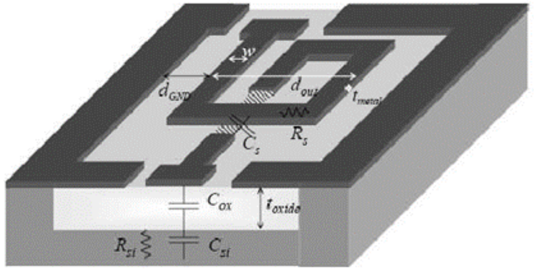


Fig 1 – Inductor typical layout

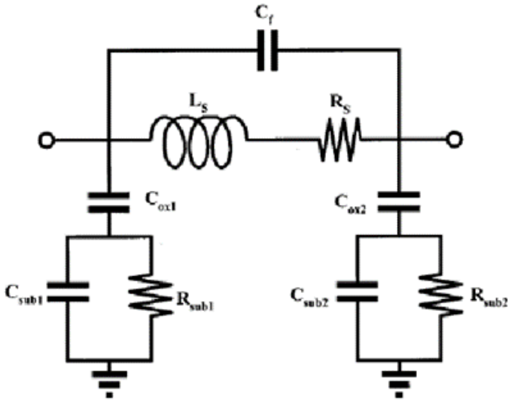
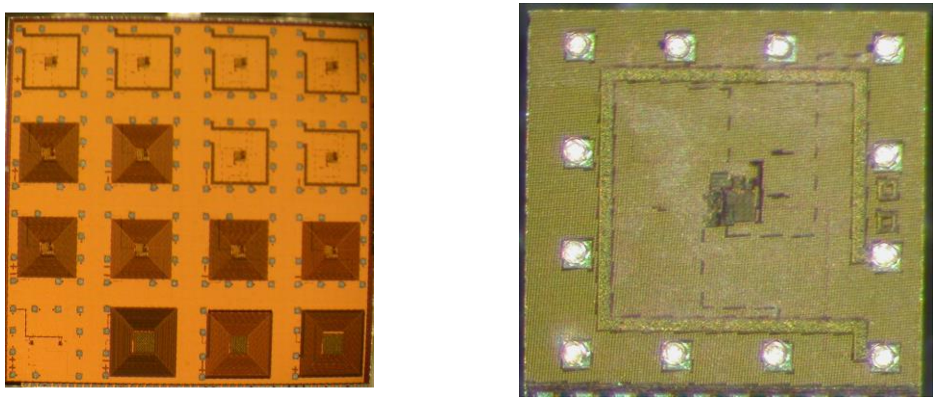


Fig 2 – Inductor model

Yishay, Roee Ben et al. “High performance MEMS 0.18µm RF- CMOS inductors.” 2008 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (2008): 1-7.



E.G. Villani, et al., A monolithic 180 nm CMOS dosimeter for In Vivo Dosimetry medical application, Radiation Measurements, Volume 71, 2014, Pages 389-391, ISSN 1350-4487,https://doi.org/10.1016/j.radmeas.2014.07.007.

Thank you

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- Layouts and interconnects in IC
  - FEOL and BEOL different characteristics
  - Interconnect delays and ways to mitigate them

- Transistors layouts in IC
- Passive components layouts in IC