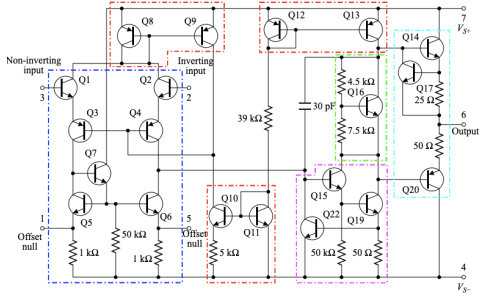
Introduction into Electronics

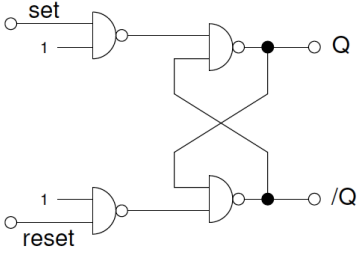
(1) Reminder: Electrical circuits
(2) Analog electronics
(3) Digital electronics
(4) Circuit analysis, circuit topologies



Literature:

Paul Horowitz, Winfield Hill
The Art of Electronics
Cambridge University Press (2015)

D. Sundararajan
Introductory Circuit Theory
Springer (2019)

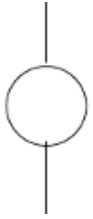


Introduction into Electronics

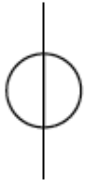
(1) Reminder: Electrical circuits

Basic elements

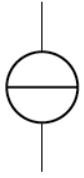
Power source:



DC voltage source:



DC current source:

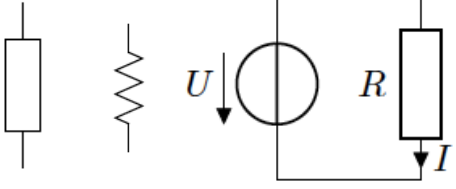


AC source:

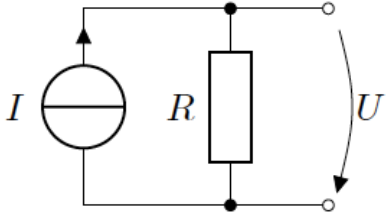
$U(t) = U_0 \sin(\omega t)$

$\hat{U} = U_{eff} = U_0/\sqrt{2}$

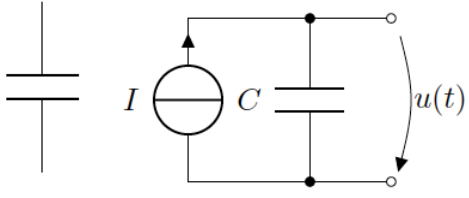
Resistance:



$$U = R \cdot I$$

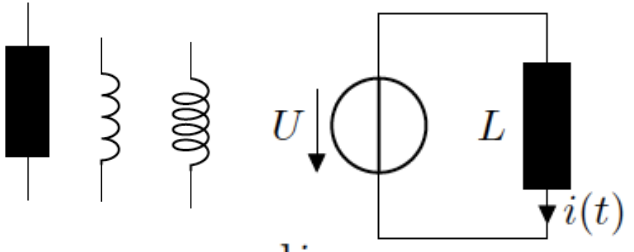


Capacitance:



$$Q = C \cdot U \qquad i(t) = \frac{\mathrm{d}q}{\mathrm{d}t} = C \cdot \frac{\mathrm{d}u}{\mathrm{d}t}$$

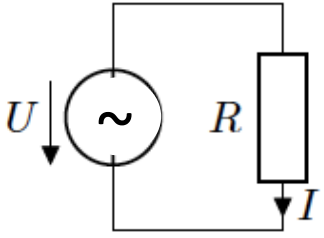
Inductance:



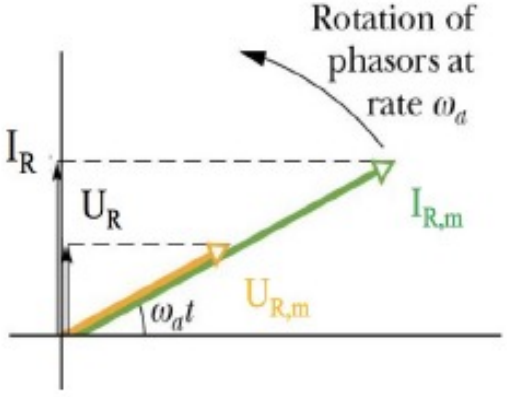
$$u(t) = L\frac{\mathrm{d}i}{\mathrm{d}t}$$

AC resistance

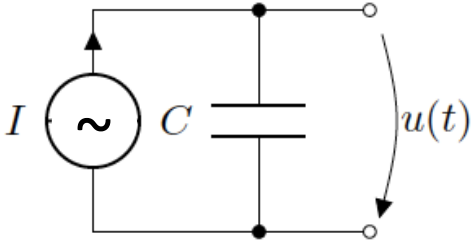
Resistance:



$$I_R = \frac{U_R}{R}$$

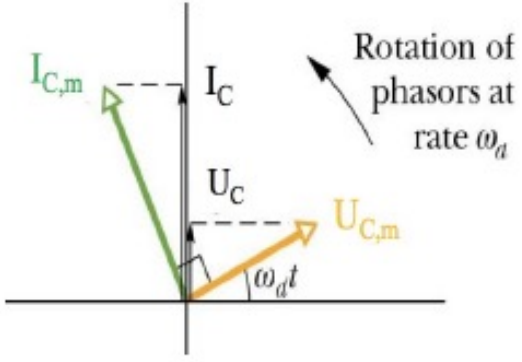


Capacitance:

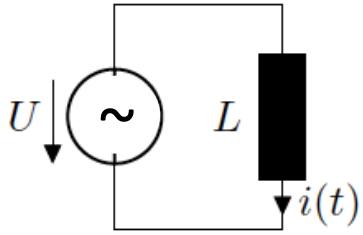


$$\hat{U}_C = \hat{I}_C \, X_C$$

$$X_C = \frac{1}{i\omega C}$$

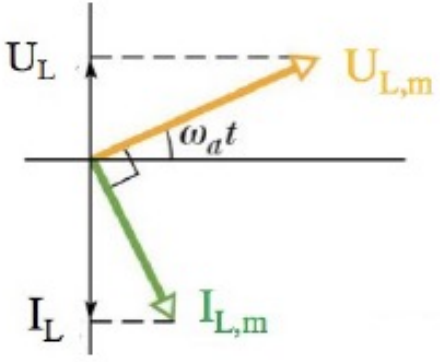


Inductance:



$$\hat{U}_L = \hat{I}_L \, X_L$$

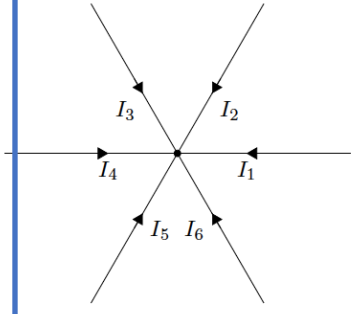
$$X_L = i\omega L$$



Networks (more later)

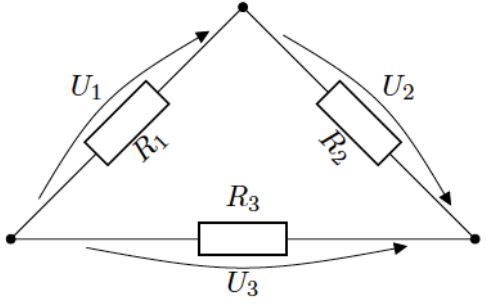
Junction rule:

$$\sum_{k=1}^{n} I_k = 0$$

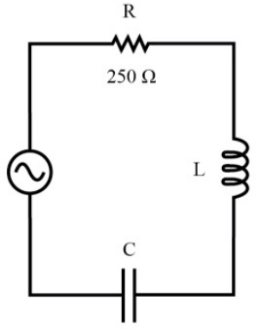


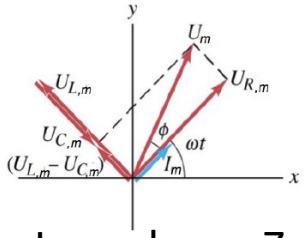
Loop rule

$$\sum_{k=1}^{n} U_k = 0$$



Impedance in AC circuits



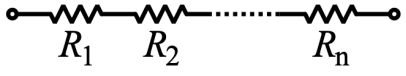


Impedance Z:

$$\hat{I} = \frac{\hat{U}}{Z}$$

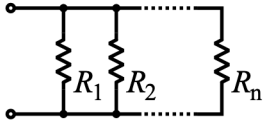
$$Z = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$$

Resistance in series:



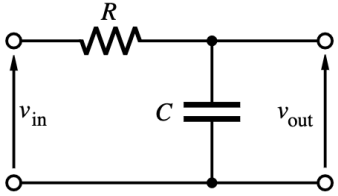
$$R_{\text{total}} = R_s = R_1 + R_2 + \cdots + R_n$$

Resistance in parallel:

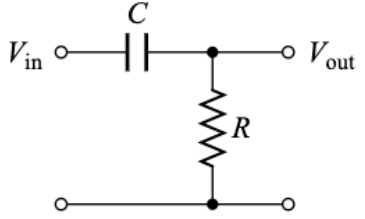


$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n}$$

Low pass



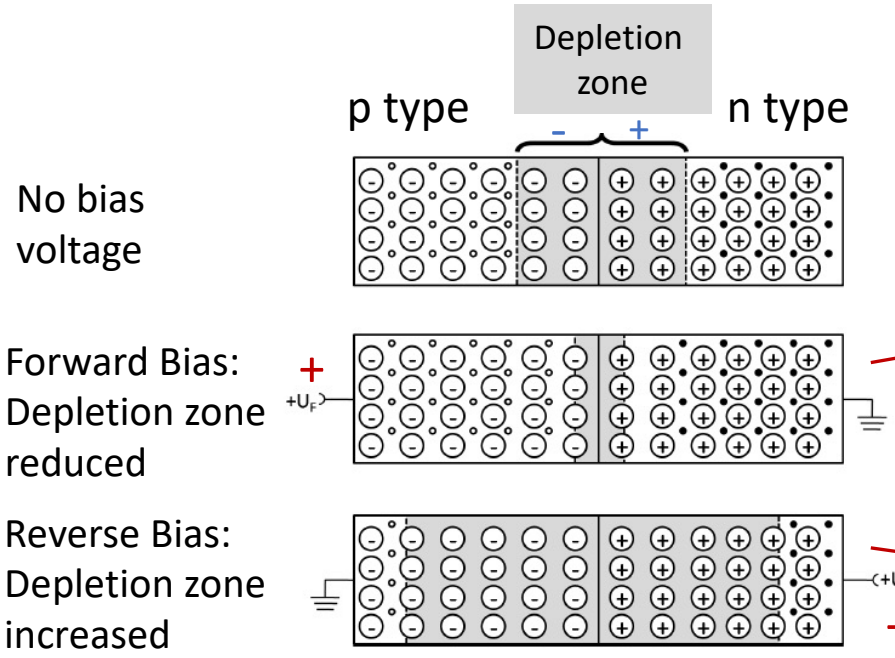
high pass

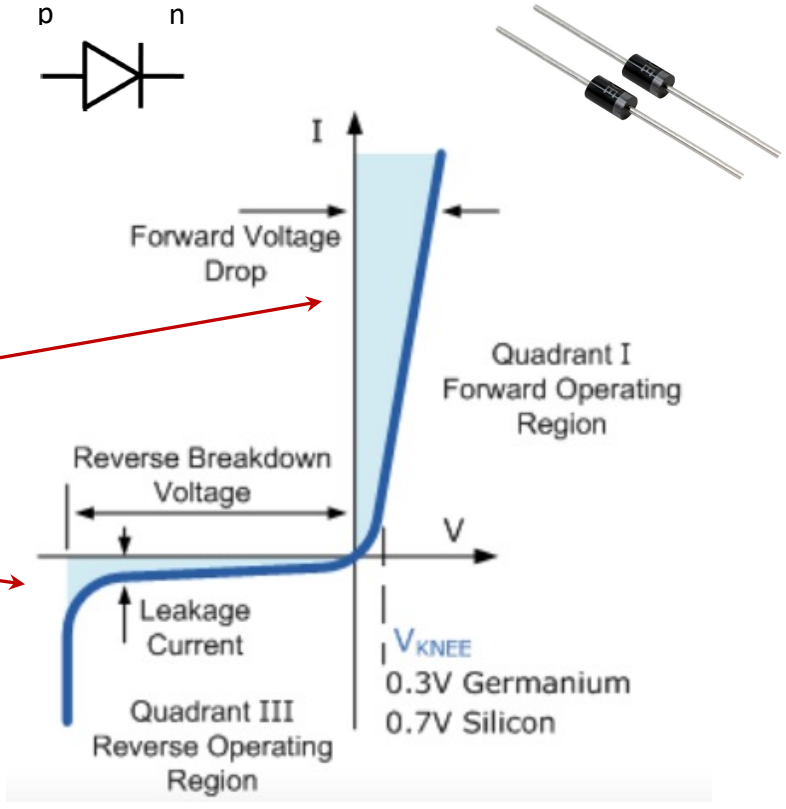


$$X_C = \frac{1}{i\omega C}$$

(2) Analog electronics

Diode: pn junction and biasing





Current-voltage characteristic

Electrons cross the junction from n to p type → depletion zone, barrier voltage

Diode: forward biasing

Ideal diode (forward bias):

$$I(U) = I_S \cdot \left(e^{\frac{U}{U_T}} - 1 \right)$$

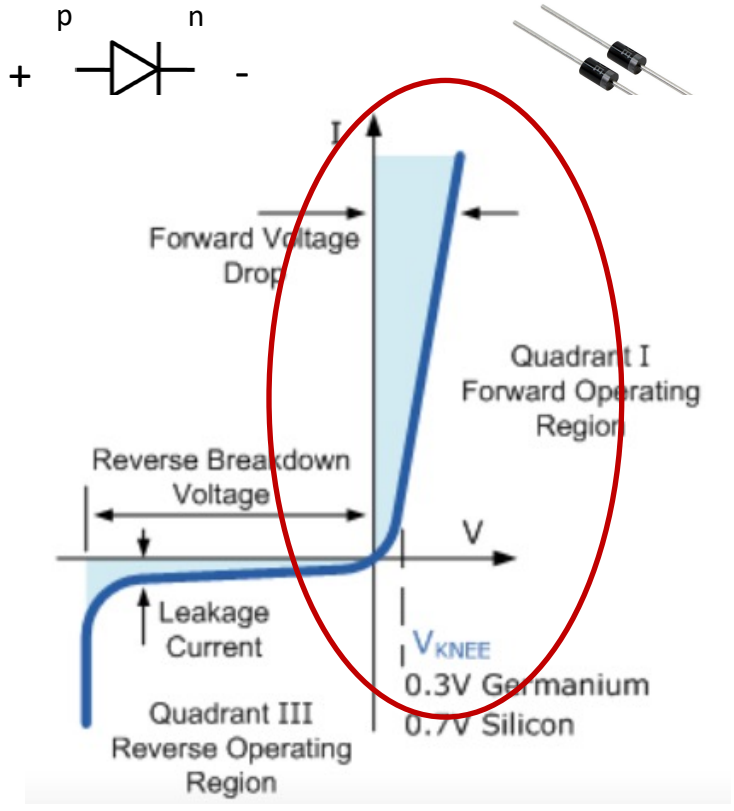
I_S: leakage current ≈ 1-100 µA
U_T: = kT/e ≈ 40 mV

Real diode (forward bias):

I(U) only > 0
for U > Barrier Voltage (≈ 0.3-0.8V)

Differential resistance:

$$r = \frac{dI}{dU}$$



Current-voltage characteristic

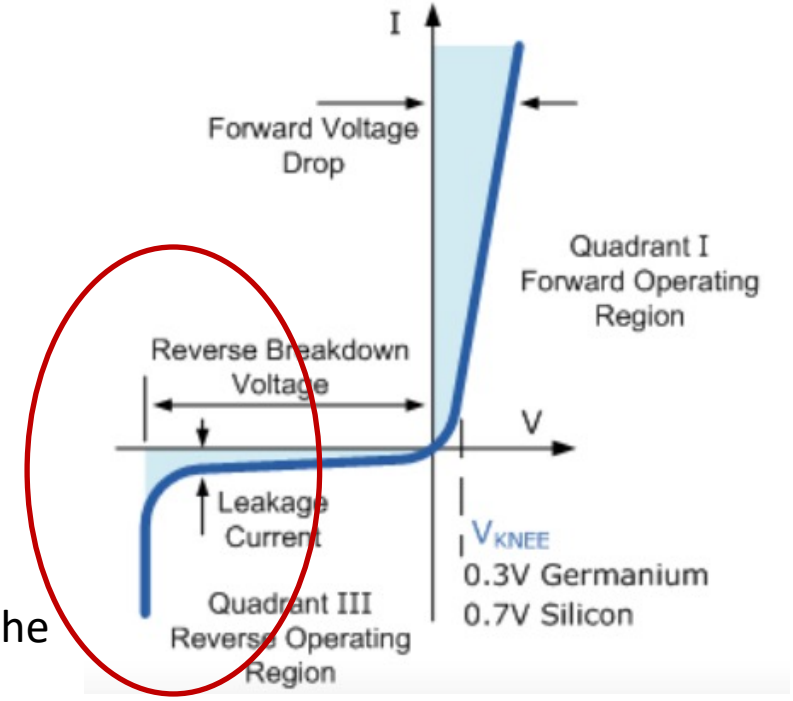
Zener diodes: reverse biasing

Conventional diodes will typically be destroyed if operated with large reverse-bias voltages.

But a Zener diode is designed to be operated with reverse bias. It is typically heavily doped leading to a small depletion zone.

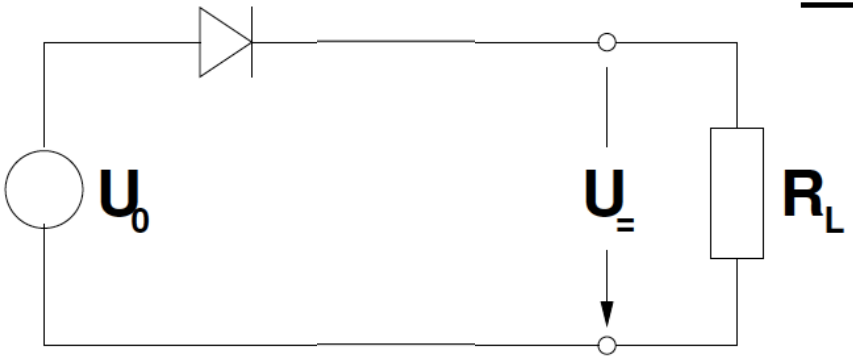
Resistance breaks down at the Zener voltage: mostly through tunneling of electrons from the p-type valence band into the n-type conduction band

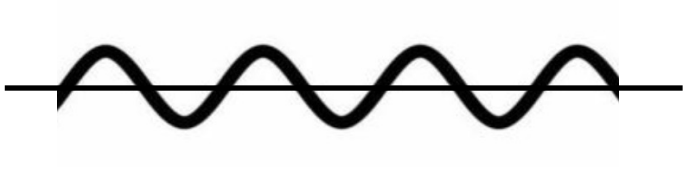
→ Voltage stabilizer, reference voltage



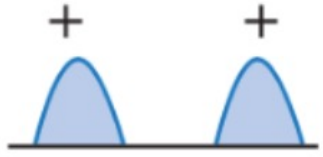
Circuits with diodes (1)

Half-wave rectifier

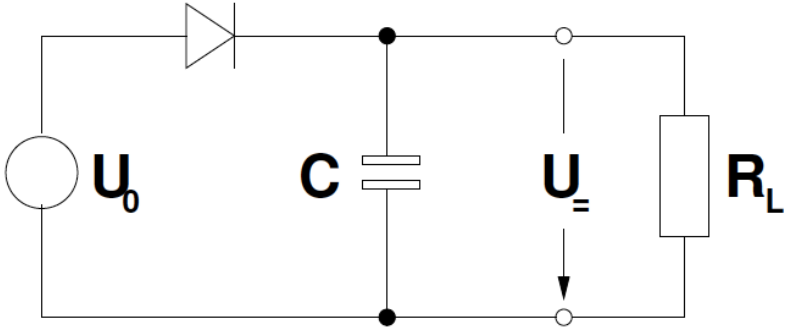




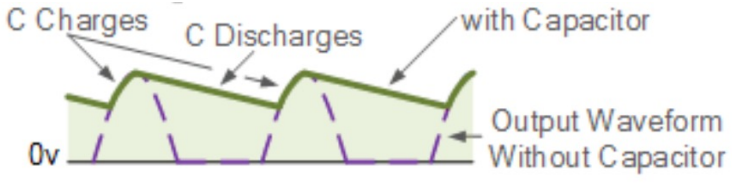
Blocks negative half waves



Half-wave rectifier with smoothing capacitor

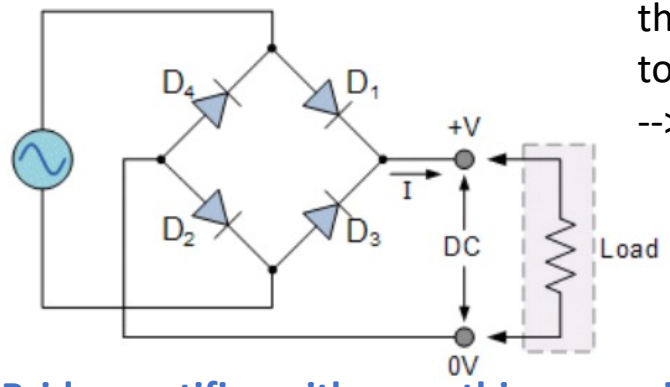


Half waves smoothened



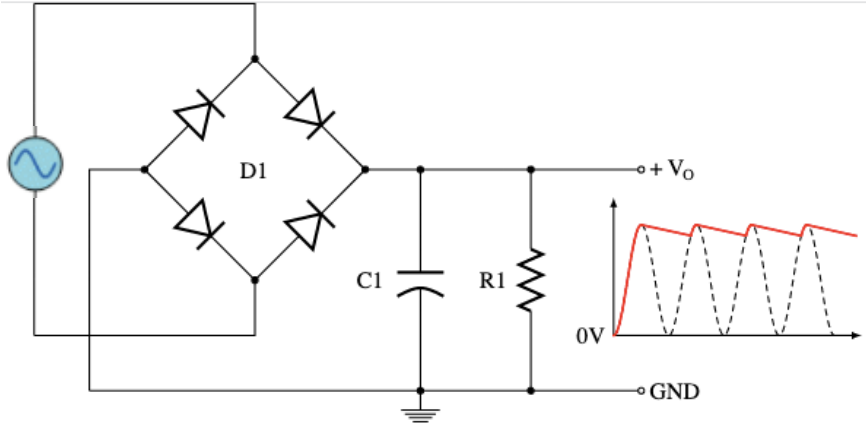
Circuits with diodes (2)

Full-wave Bridge rectifier



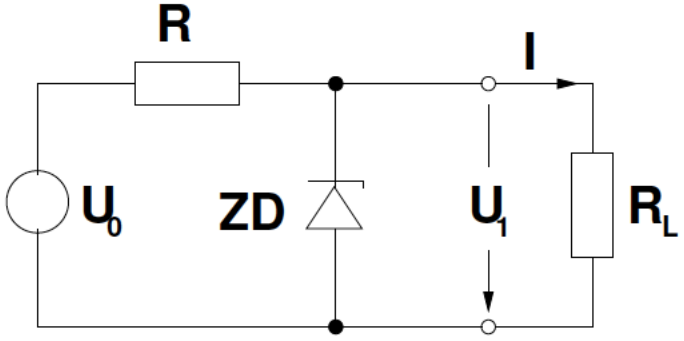
Diodes are arranged such that
the positive pole is always connected
to the same point.
--> Inverts negative half waves

Bridge rectifier with smoothing capacitance



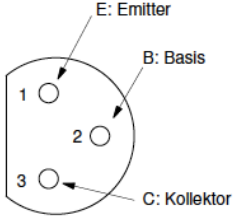
Voltage regulation/limitation:

If the initial voltage becomes larger than the Zener voltage the Zener current Increases → resistance drops

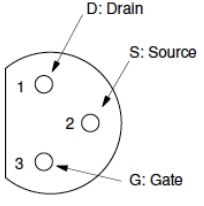


Transistors

- Active, controllable semiconductor devices.
- Amplify and switch signals and power
- Main types:
  - **Bipolar junction transistor (BJT)**
    - here: **npn transistor**
    - pnp transistor: works in an analogous manner

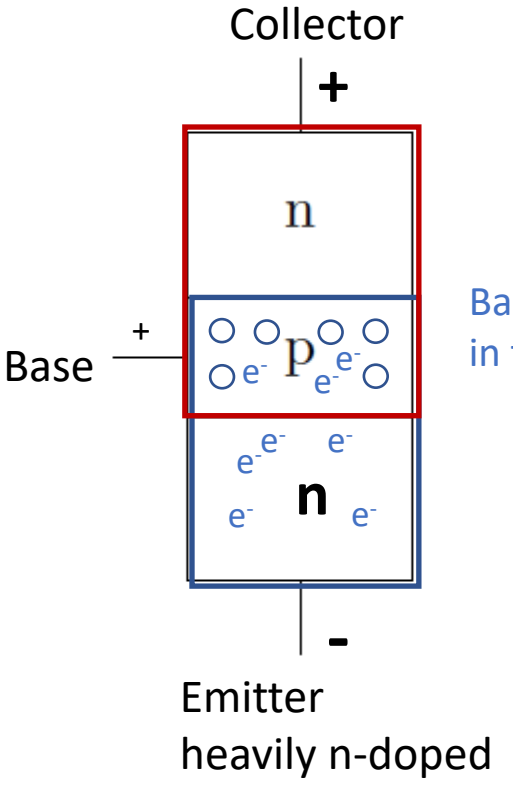


  - **Field Effect Transistor (FET)**
    - MOSFET: **NMOS**/PMOS
    - CMOS: combines NMOS an PMOS

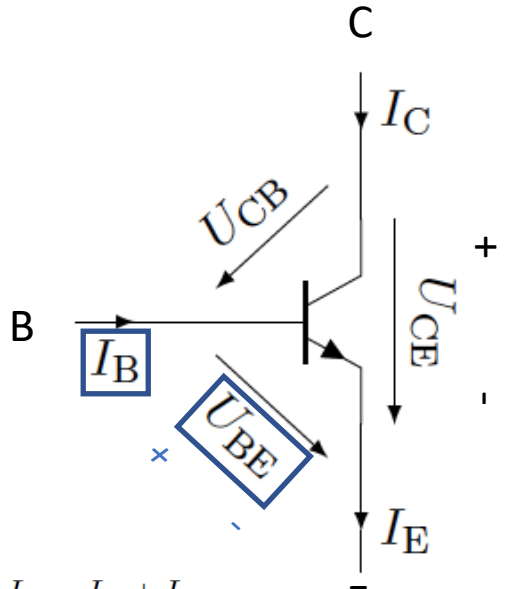


Contemporary Integrated Circuits (IC) are in general not build from discrete transistors but need to understand the transistor principle to understand IC

Bipolar Junction Transistor



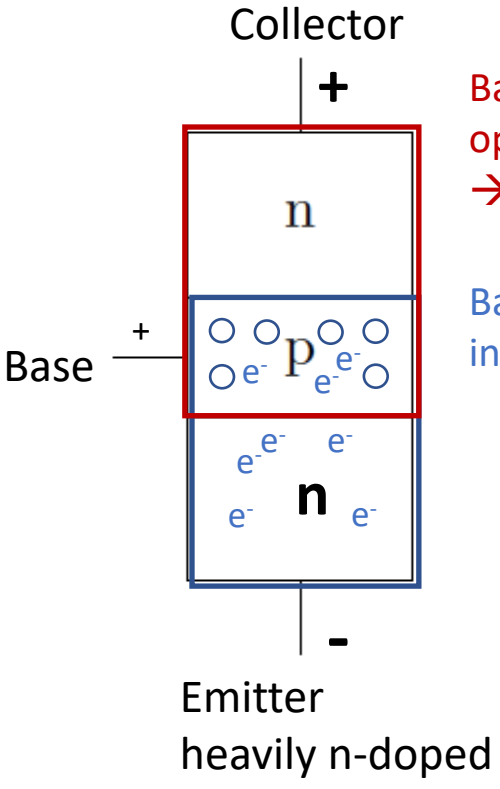
Base-Emitter diode: operated in forward direction



$$I_E = I_C + I_B$$

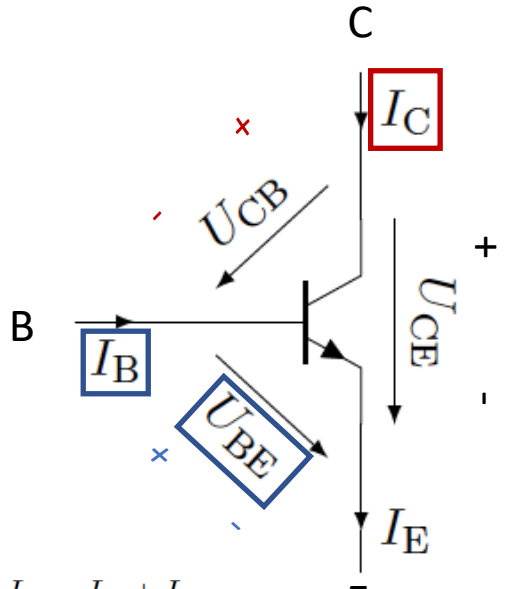
$$U_{CE} = U_{CB} + U_{BE}$$

Bipolar Junction Transistor



Base-Collector diode:
operated in reverse bias
→ "leakage" collector current I_C

Base-Emitter diode: operated
in forward direction



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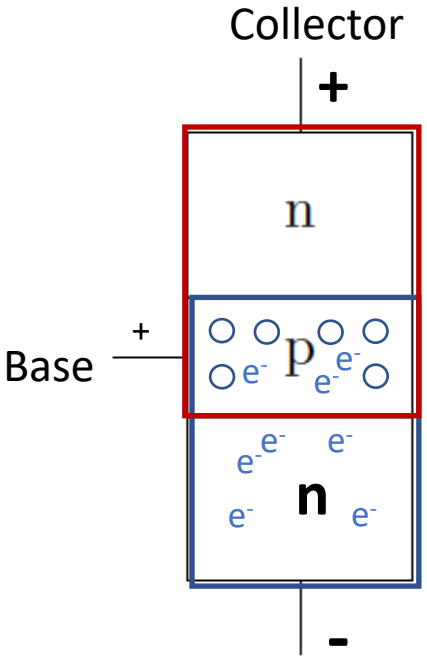
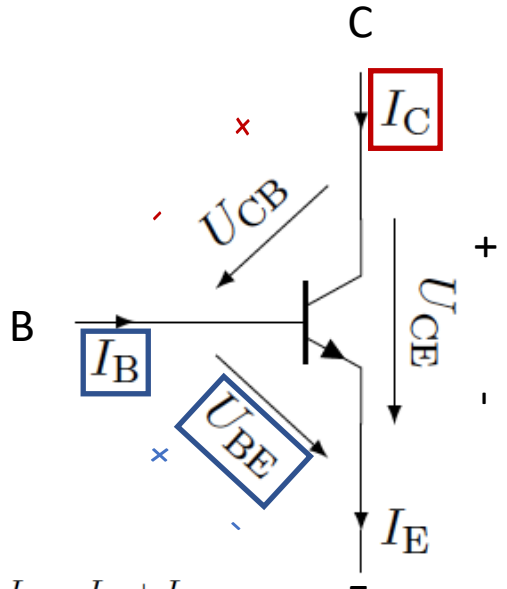
Bipolar Junction Transistor



Base-Collector diode:
operated in reverse bias
→ "leakage" collector current I_C

Base-Emitter diode: operated in forward direction
→ electrons drift into the base
→ some electrons reach the p-n transition region of the Base-Collector diode
→ increase collector current I_C



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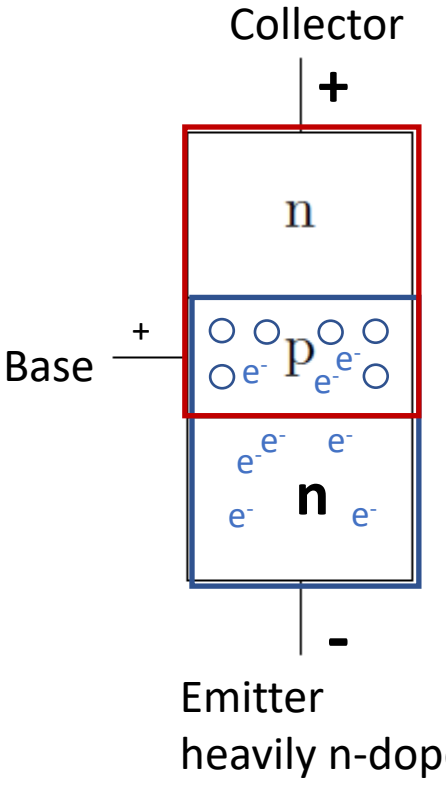
Bipolar Junction Transistor



Base-Collector diode:
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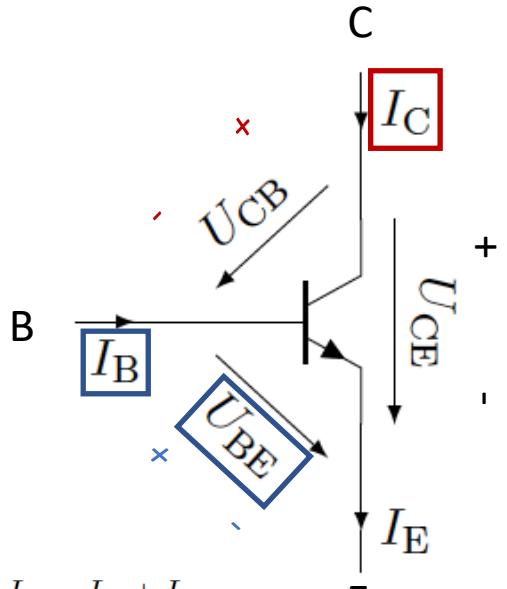


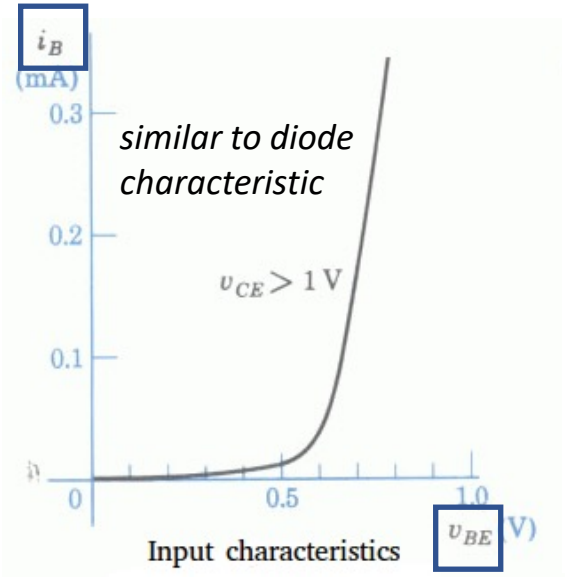
$$I_E = I_C + I_B$$

$$U_{CE} = U_{CB} + U_{BE}$$

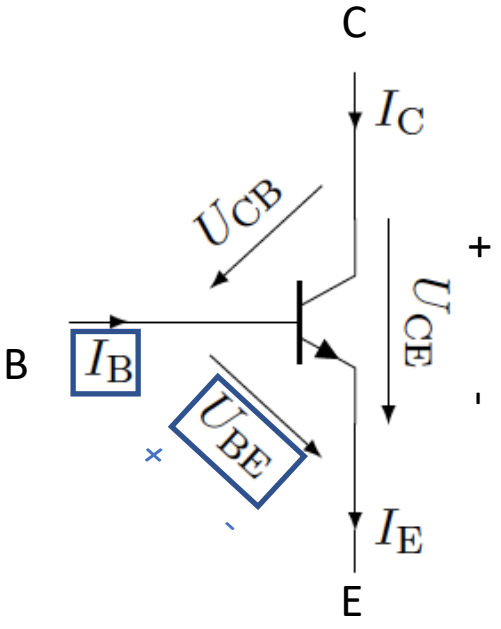
I_B/U_{BE} → control → I_C

npn BJT: characteristics (1)

Input characteristics

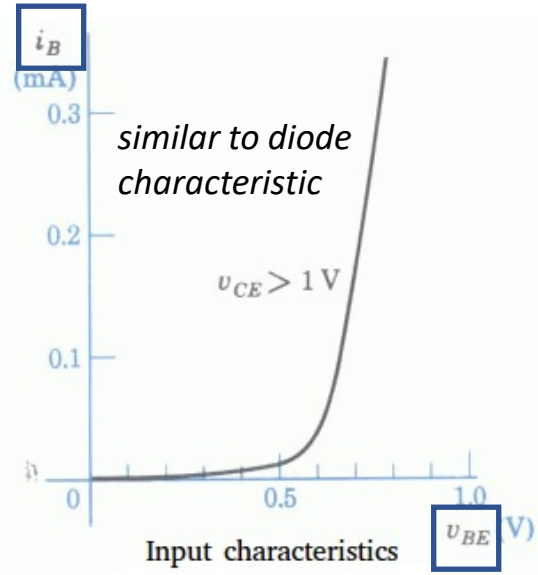


similar to diode characteristic

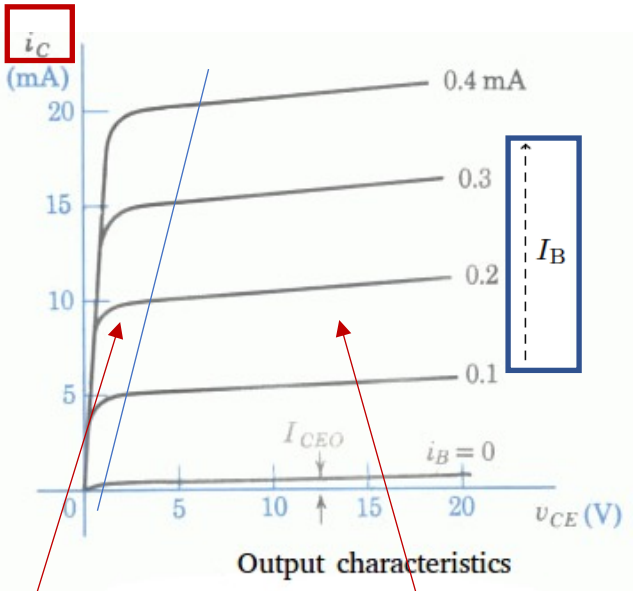


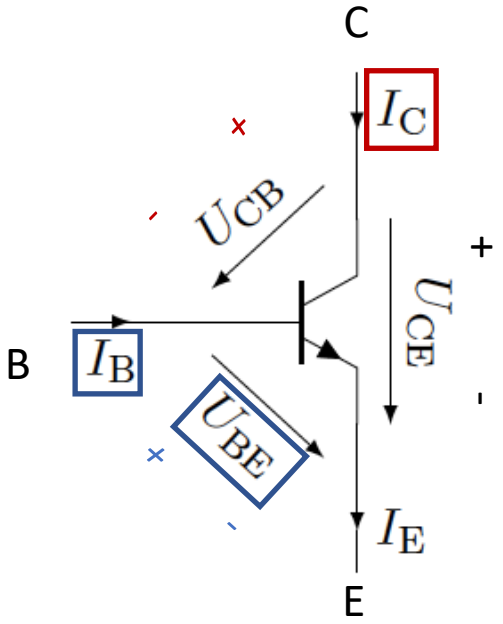
npn BJT: characteristics (1)

Input characteristics



Output characteristics





Saturation region:

Small changes in U_{CE} lead to large change in I_C

→ switches etc.

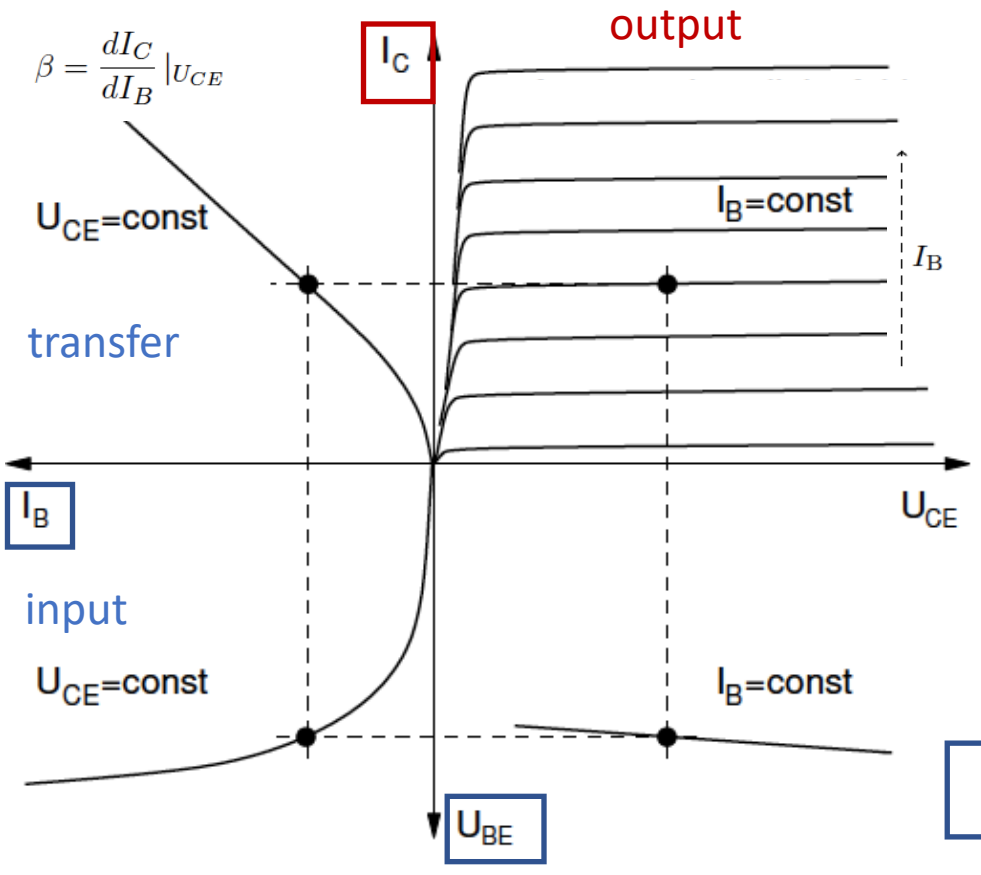
Active region:

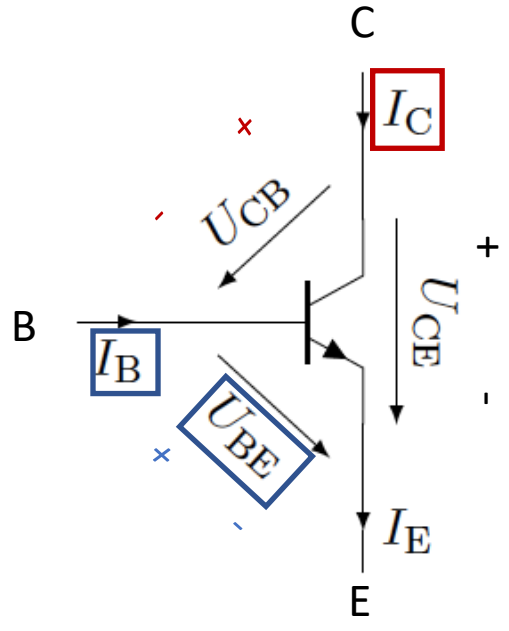
Small change in base current I_B lead to large change in collector current, nearly independent of U_{CE}

→ Current amplification etc.

npn BJT: characteristics (2)

- working point in active region

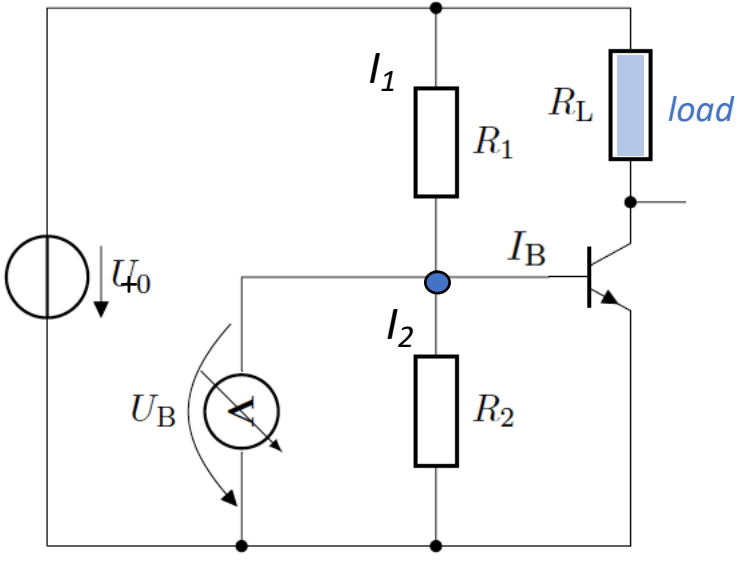




I_B/U_{BE} → control → I_C

Selecting the working point

Example circuit



(Calculation: see later)

Voltage divider biasing

The voltage U_B across R_2 forward-biases the BE junction

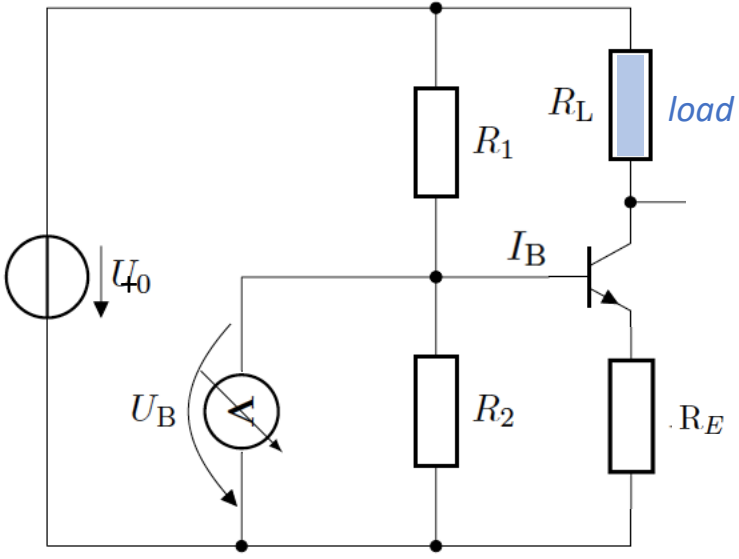
$$U_B = U_0 \cdot \frac{R_2}{R_1 + R_2} - I_B \cdot \frac{R_1 R_2}{R_1 + R_2}$$

If R_1, R_2 are sufficiently small, the base current does not impact the base voltage

$$I_B \cdot R_1 \ll U_0 \quad \rightarrow \quad U_B \approx U_0 \cdot \frac{R_2}{R_1 + R_2}$$

Selecting the working point

Example circuit



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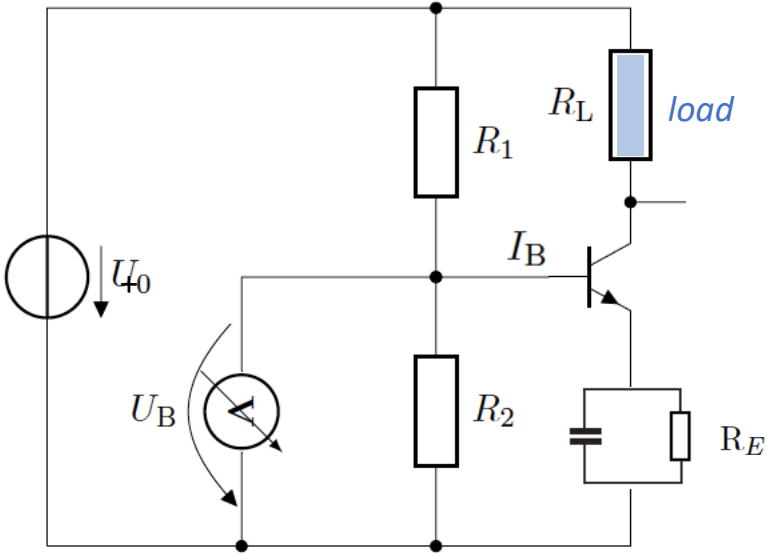
Stabilizing WP by adding emitter resistance R_E

Reduces U_{BE} if base current I_B becomes too large.

Selecting the working point

Example circuit



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$$I_B \cdot R_1 \ll U_0 \quad \rightarrow \quad U_B \approx U_0 \cdot \frac{R_2}{R_1 + R_2}$$

Stabilizing WP by adding emitter resistance R_E

$$X_C = \frac{1}{i\omega C}$$

Reduces U_{BE} if base current I_B becomes too large.
Effect on AC signal can be mitigated by adding a capacitor in parallel
→ R_E || R_C reduced for high frequencies, $R \approx R_E$ for low frequencies

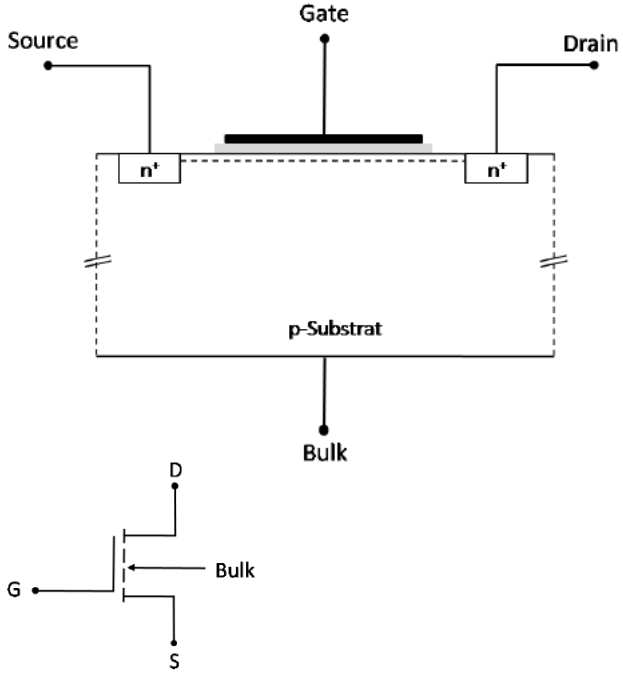
FET

BJT not suited for Integrated Circuits (IC): base currents would overheat the IC
→ use FETs: similar operation as with BJT but:

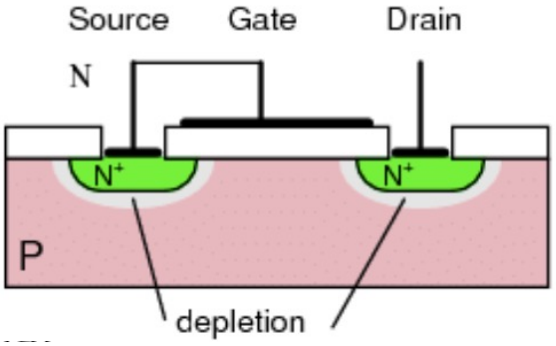
- controlled with negligible currents
- smaller area
- transfer characteristics more linear
- less noise

Example n-channel MOSFET (Metal-Oxide-Silicon FET):

- p-doted substrate
- n-doted channels: Source, Drain
- Gate isolated from substrate by e.g. SiO_2
  - → no Gate-Source/Drain currents

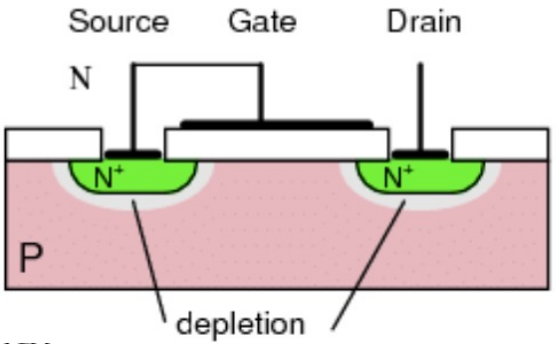


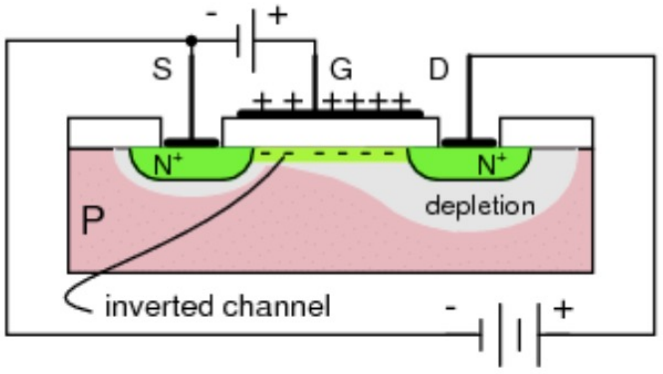
N-channel MOSFET: operation



- No source drain current

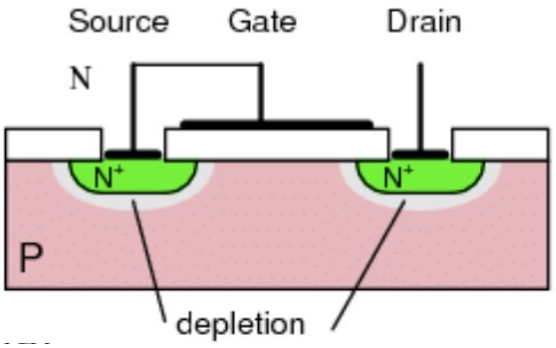
N-channel MOSFET: operation

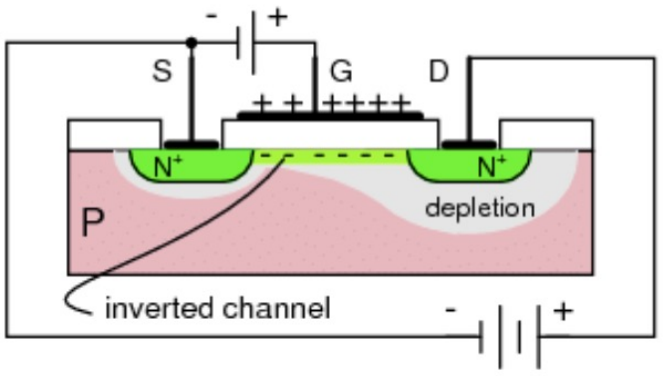




- No source drain current
- Electrons from p-doted substrate drawn towards positively charged gate
- → channel allows for S-D current I_D

N-channel MOSFET: operation





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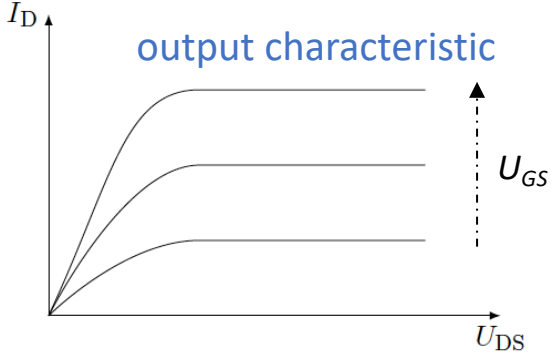
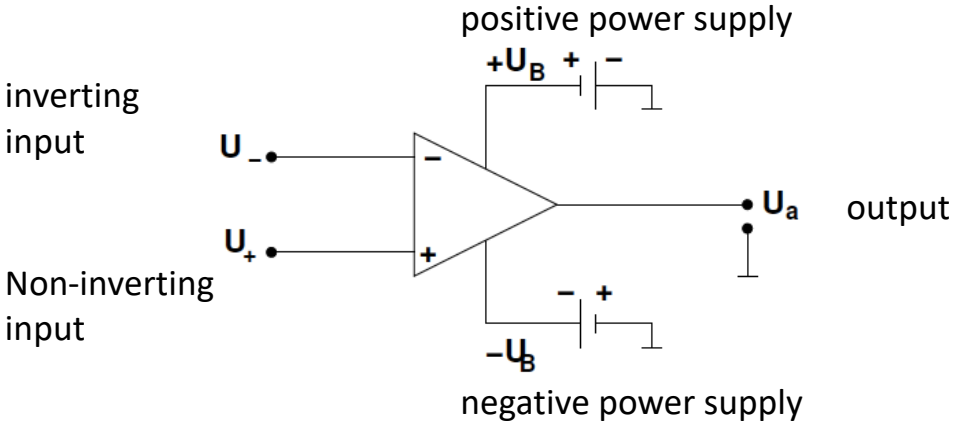
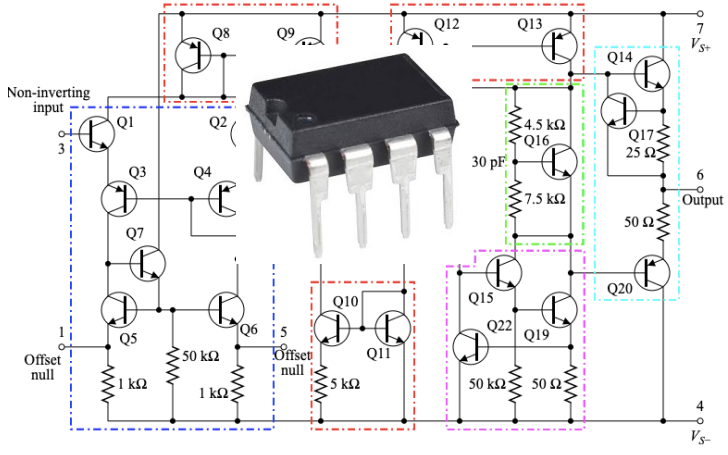


Typically, smaller transconductance than BJT (output current /input voltage)

Operational amplifier (op amp)

Difference amplifier with two inputs and one output

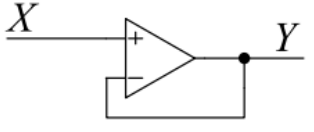




Characteristics:

- Output voltage proportional to the difference between the input voltages: very high amplification (> 10000-100000)
- If used with negative feedback (U_a connected with U-) the op amp regulates U+ = U- [1]
- Negligible input current (into the op amp) [2]
- The maximum output voltage is the power supply voltage

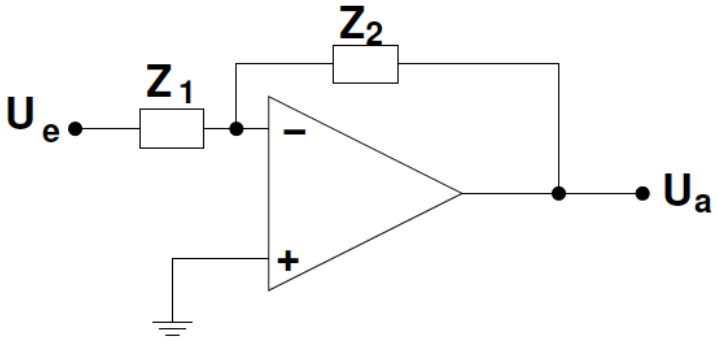
$$U_a = v_0 \cdot (U^+ - U^-)$$



negative feedback

Op amp circuits

Inverting amplifier



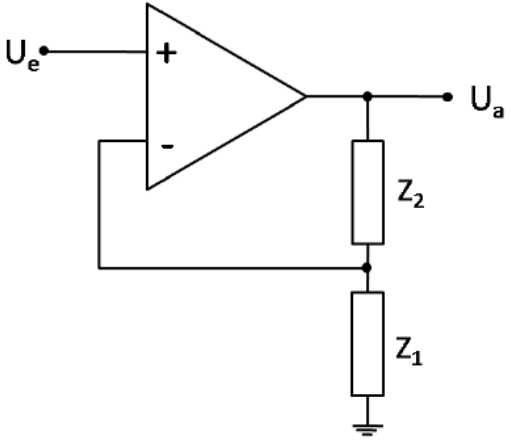
[2] → $I_1 = \frac{U_e - U^-}{Z_1} = \frac{U^- - U_a}{Z_2} = I_2$

[1] → $U^- = 0\ \mathrm{V}$ (virtual ground)

→ $U_a = -\frac{Z_2}{Z_1} U_e$

- If used with negative feedback (U_a connected with U-) the op amp regulates U+ = U- [1]
- Negligible input current (into the op amp) [2]

Non-inverting amplifier



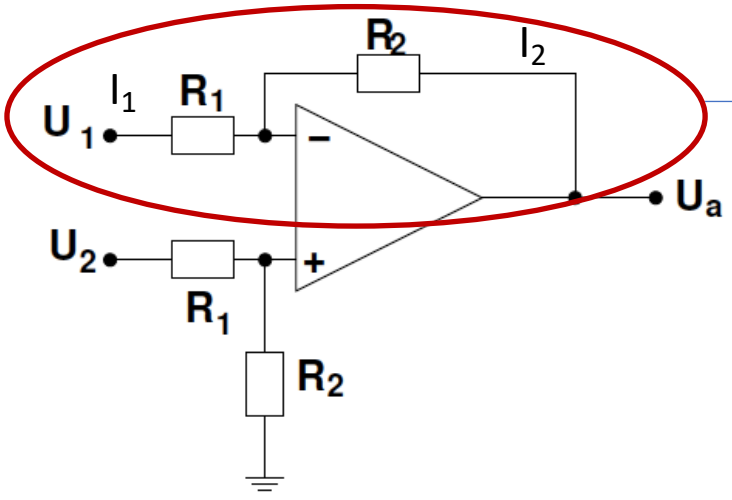
Negative feedback from voltage divider:

[1] → $U_e = U- = \frac{Z_1}{Z_1+Z_2} Ua$

→ $U_a = \left(\frac{Z_2}{Z_1} + 1\right) U_e$

Op amp circuits

Differential amplifier



[1] $U_- = U_+ = U$

[2] $I_1 = \frac{U_1 - U}{R1} = I_2 = \frac{U - Ua}{R2}$

$\rightarrow \frac{U_1 R_2}{R_1} - \frac{U R_2}{R_1} = U - Ua$

$\rightarrow U_a = U\,\frac{R_2 + R_1}{R_1} - U_1 \frac{R_2}{R_1}$ (*)

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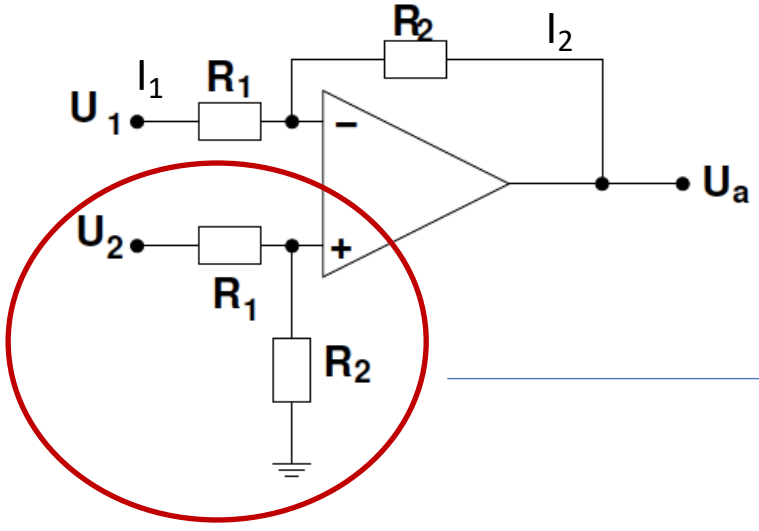
- Negligible input current (into the op amp) [2]

Op amp circuits

Differential amplifier



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$\rightarrow U_a = U \frac{R_2 + R_1}{R_1} - U_1 \frac{R_2}{R_1}$ (*)

$U = U_2 \frac{R_2}{R_1 + R_2}$ (voltage divider) (**)

- If used with negative feedback (U_a connected with U-) the op amp regulates U+ = U- [1]
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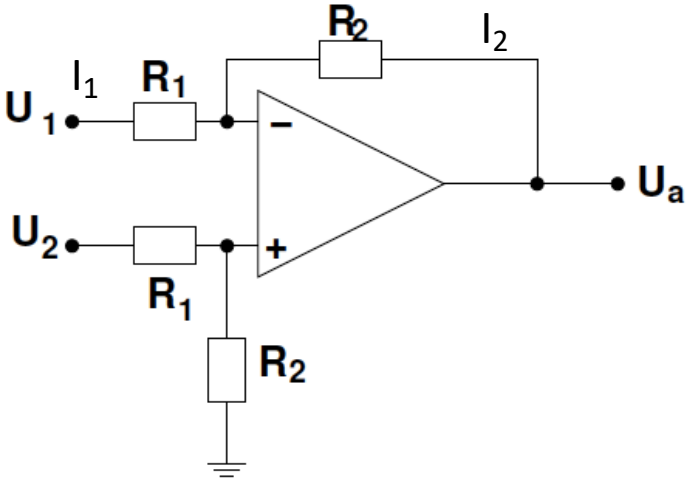
Op amp circuits

Differential amplifier



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$U = U_2\,\frac{R_2}{R_1 + R_2}$ (voltage divider) (**)

(**) in (*)

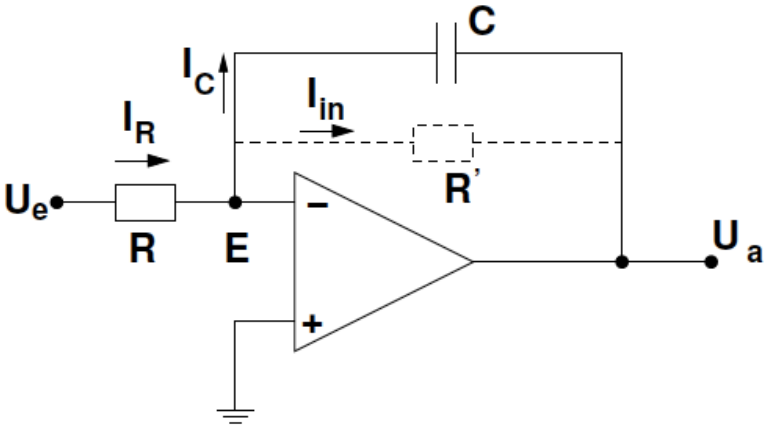
→ $U_a = U_2\,\frac{R_2}{R_1 + R_2}\,\frac{R_1 + R_2}{R_1} - U_1 \frac{R_2}{R_1}$

→ $U_a = \frac{R_2}{R_1}\,(U_2 - U_1)$

- If used with negative feedback (U_a connected with U-) the op amp regulates U+ = U- [1]
- Negligible input current (into the op amp) [2]

Op amp circuits

Integrator

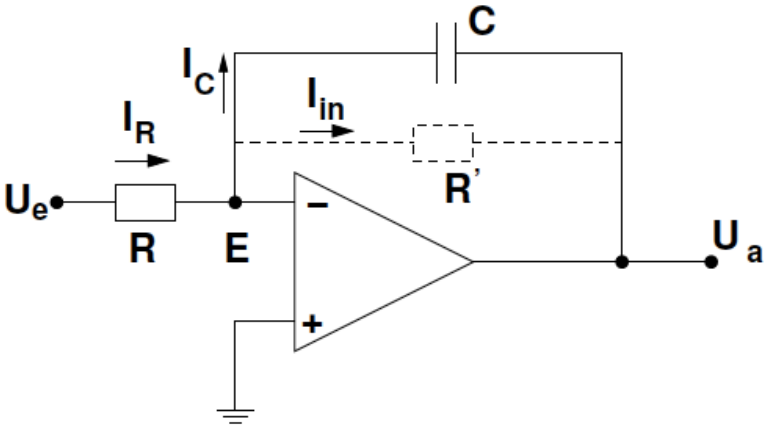


Virtual ground offset by input current
→ op amp passes a current that charges the capacitor to maintain the virtual ground

$$I_R = \frac{U_e}{R} \approx I_c$$

Op amp circuits

Integrator



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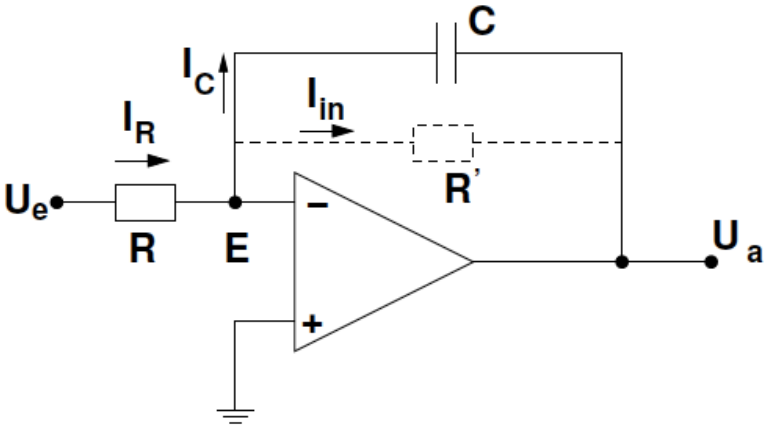
Capacitor equation:

- Differential: $I = C \frac{dU}{dt}$
- Integrated: $U = \frac{1}{C}\int I dt$ (*)

Op amp circuits

Integrator



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$$I_R = \frac{U_e}{R} \approx I_c$$

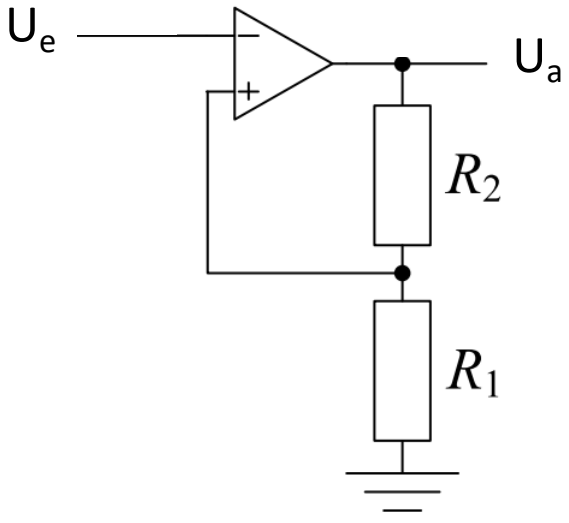
with(*):

$$U_a = -\frac{1}{RC}\int_0^t U_e \, dt$$

→ The output voltage is proportional to the time integrated input voltage

Op amp circuits

Schmitt trigger: positive feedback

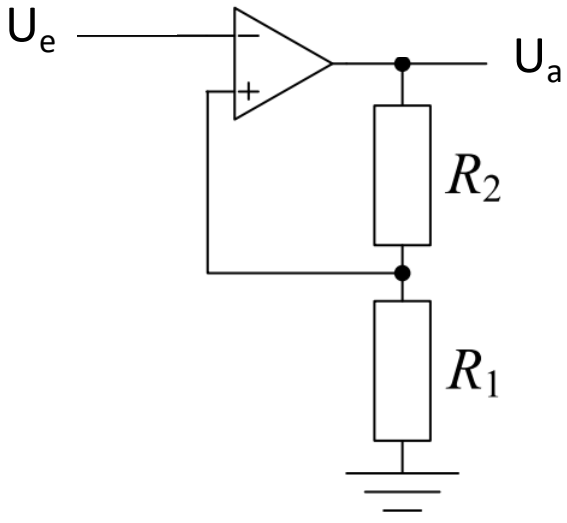


$$U_a = v_0 \cdot (U^+ - U^-)$$

If U_a rises, the difference between U_- and U_+ will rise. This causes U_a to rise even further until maximum output voltage (given by the power supply voltage) is reached

Op amp circuits

Schmitt trigger: positive feedback



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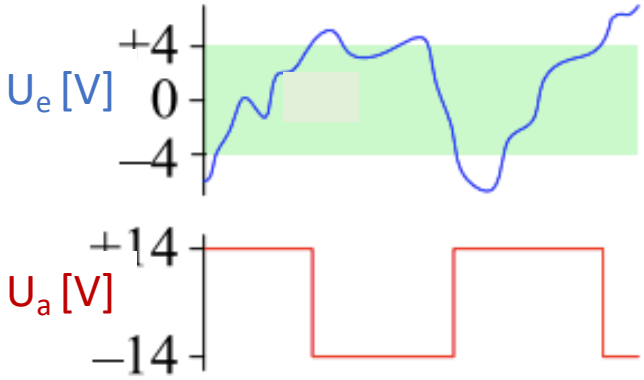
If U_a rises, the difference between U_- and U_+ will rise. This causes U_a to rise even further until maximum output voltage (given by the power supply voltage) is reached

Example: U_{max} = 14V, R_1 = 10Ω, R_2 = 4Ω

If U_a = 14V, U+ = 4V. If U_e exceeds 4V, $U_- > U_+$ and U_a flips to -14V



(3) Digital electronics

Digital electronics

Work with only two voltage levels (depend on type and input/output)

- High: 1, typically 2-5V
- Low : 0, typically 0-1.5V

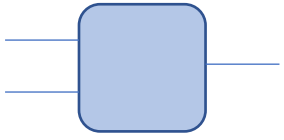
- Hexadecimal 4-bit groups:

0000	0	0100	4	1000	8	1100	C
0001	1	0101	5	1001	9	1101	D
0010	2	0110	6	1010	A	1110	E
0011	3	0111	7	1011	B	1111	F

Example:

- Decimal: 2024
- Binary: 0000 0111 1110 1000
- Hexadecimal: 07E8

- Boolean algebra



AND OR

x	y	$x \wedge y$	$x \vee y$
0	**0**	0	0
1	**0**	0	1
0	**1**	0	1
1	**1**	1	1

NOT

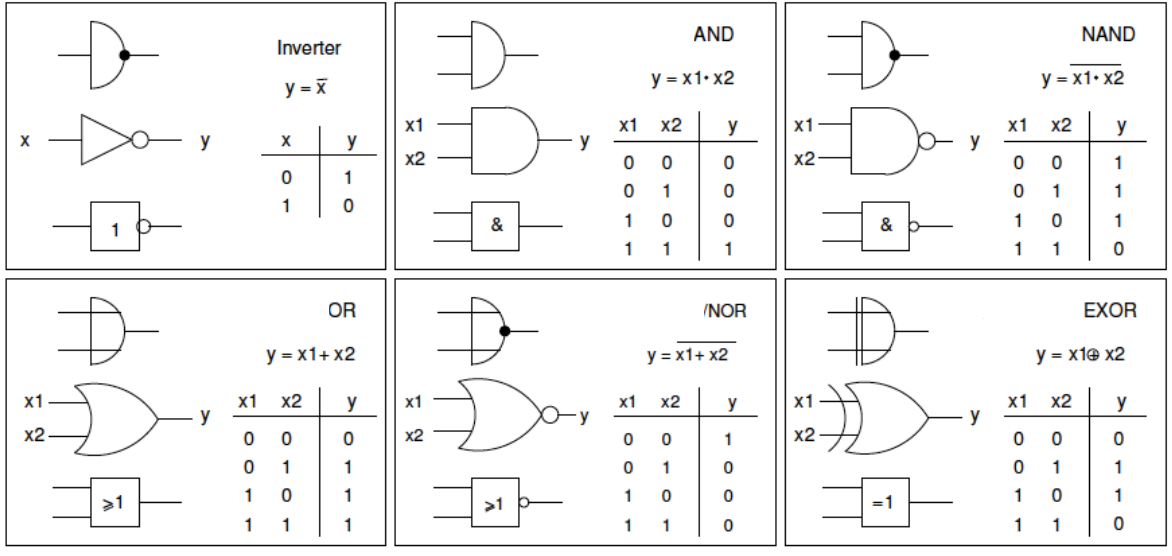
x	$\neg x$
0	1
1	0

Laws:

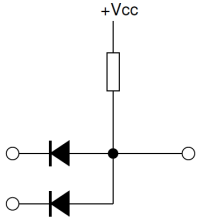
- Associativity
- Commutativity
- Distributivity

Logical operations

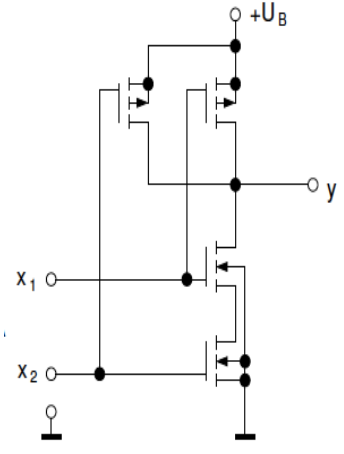
Full table of symbols, including secondar operations



Simple diode-based AND gate



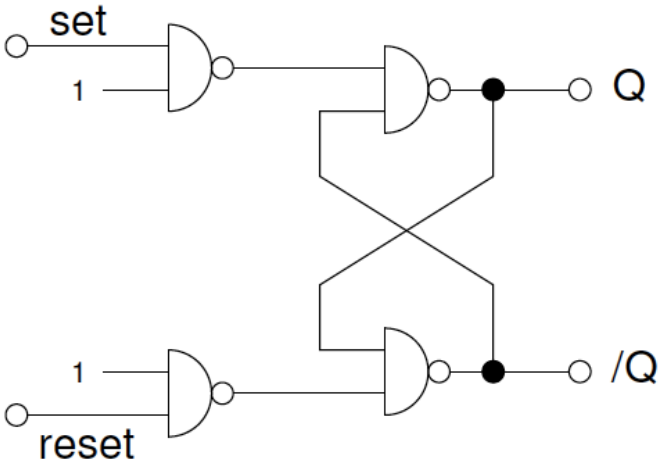
CMOS-based NAND gate



Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

Simple SR Latch



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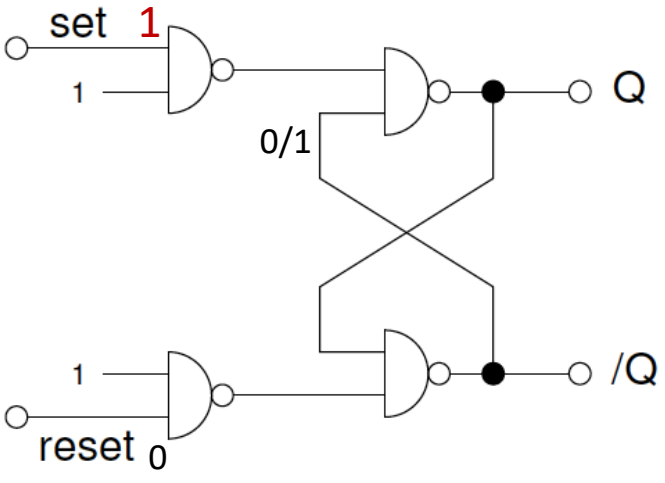

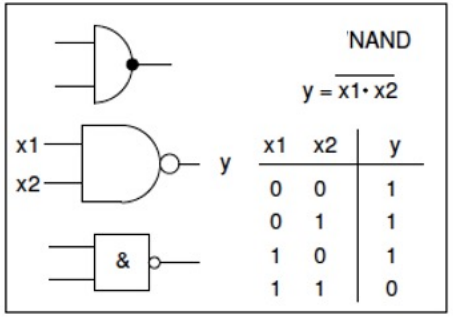

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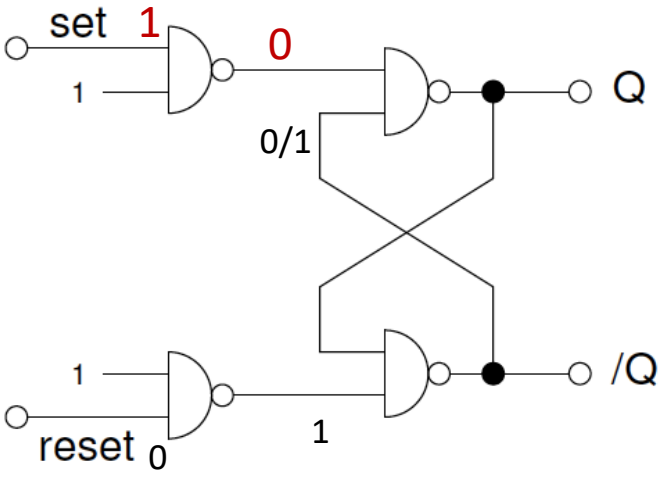

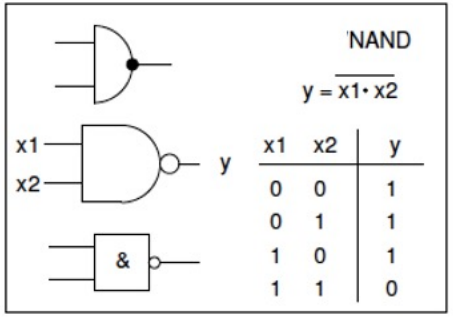

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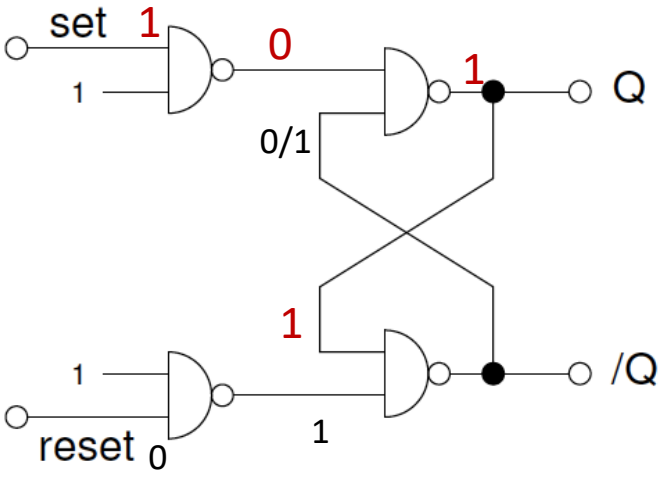

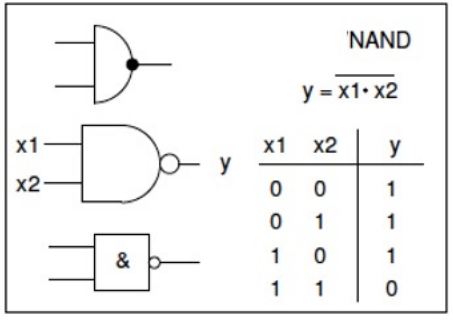

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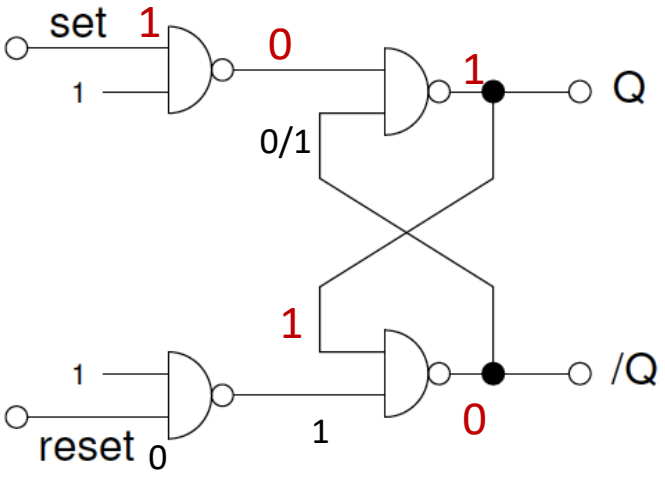

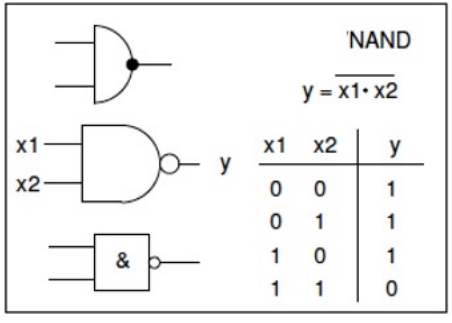

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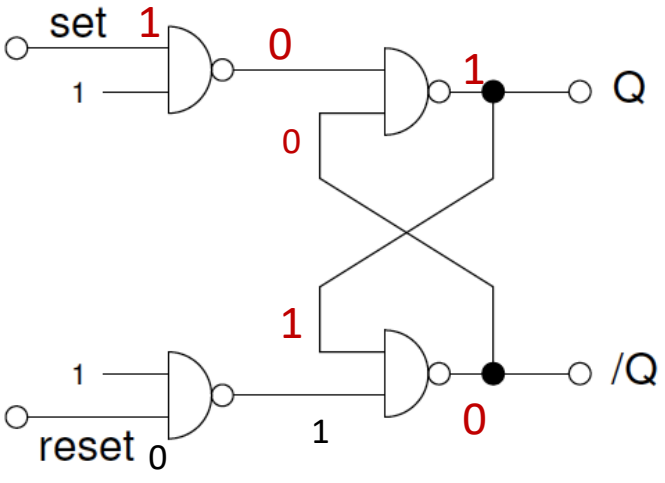
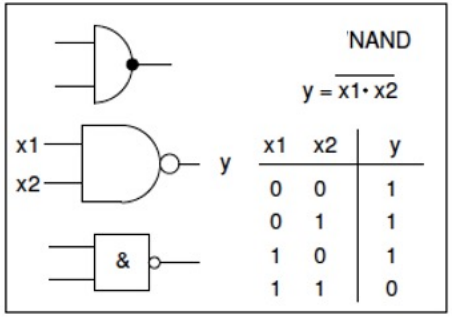
Simple SR Latch



stable situation



Flip Flop: SR latch

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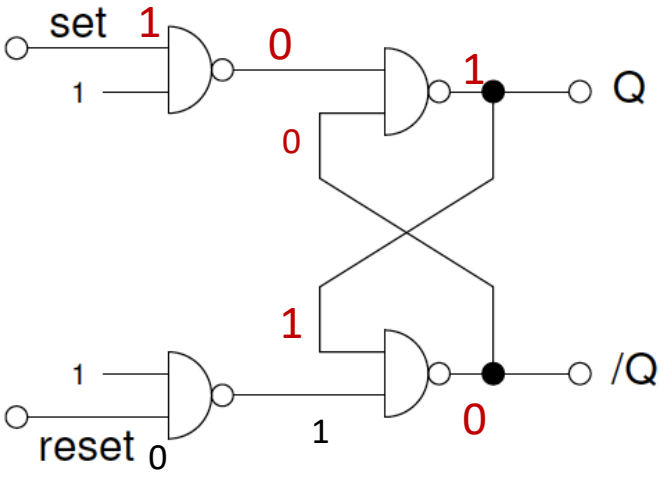

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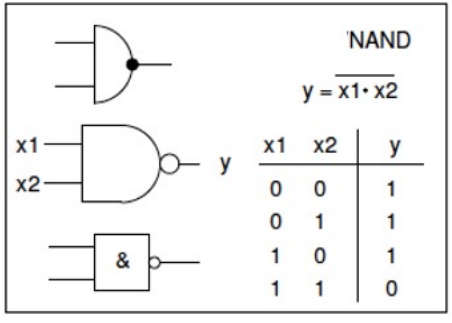


Likewise, setting the reset to 1 and the set to 0, will lead to the inverse stable Situation

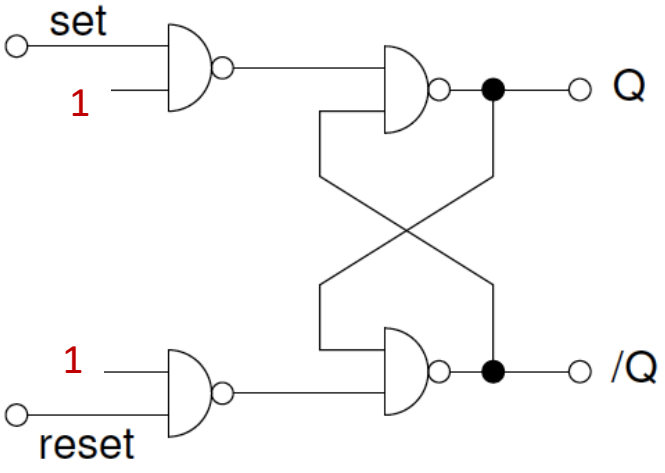
If the second inputs are 0, Q does not change latch is "opaque"

→ Gated or clocked SR latch

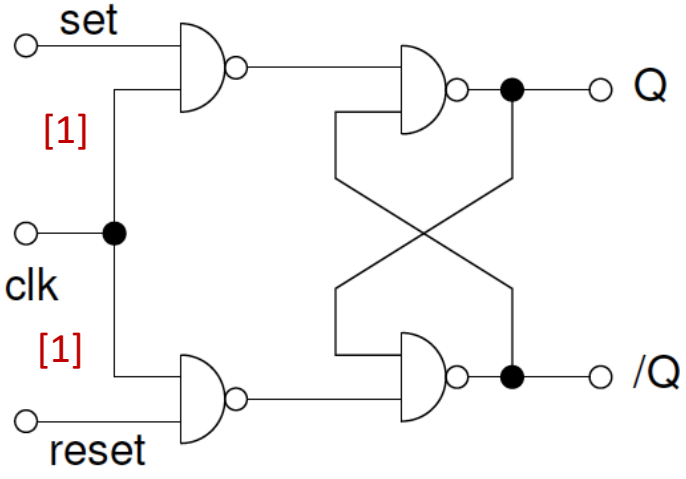
Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

Simple SR Latch



Clocked SR Latch

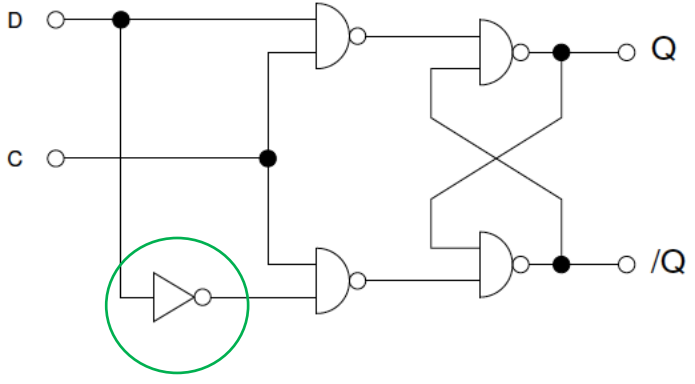


clk provides "1" in a clocked way

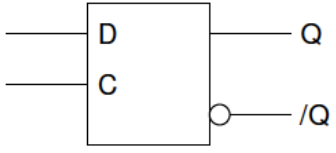
D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

D- Latch: only “set” input needed, due to inverter



symbol:



Truth table:

C	D	Q	$\overline{Q}$	Comment
0	X	Q_{prev}	$\overline{Q}_{prev}$	No change
1	0	0	1	Reset
1	1	1	0	Set

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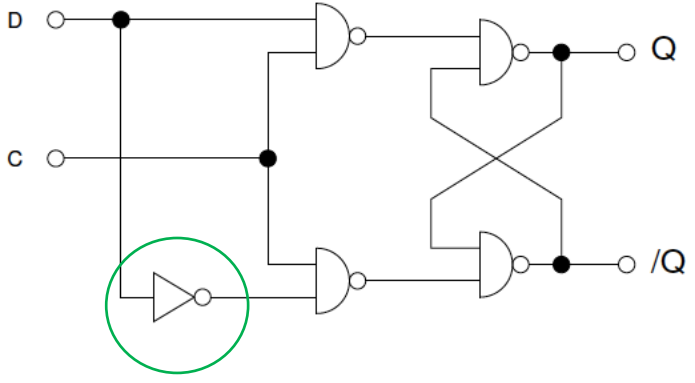

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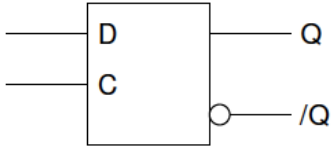
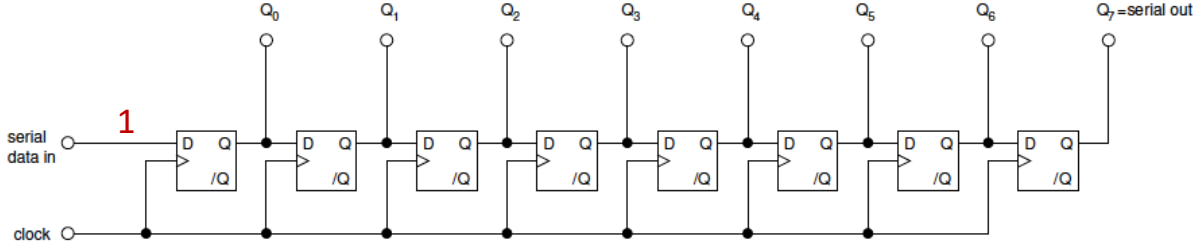


…. can be used to construct serial shift register



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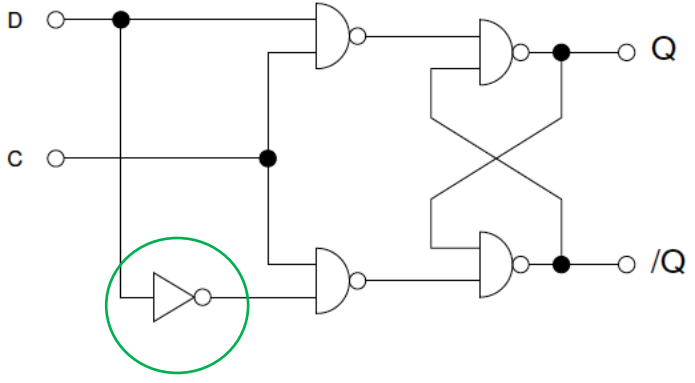

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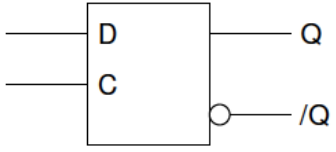

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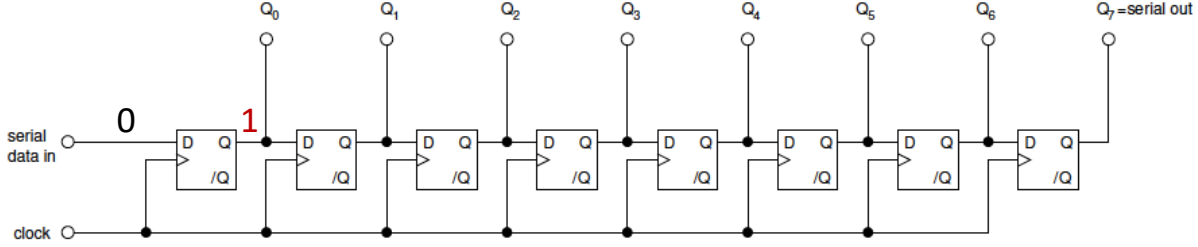

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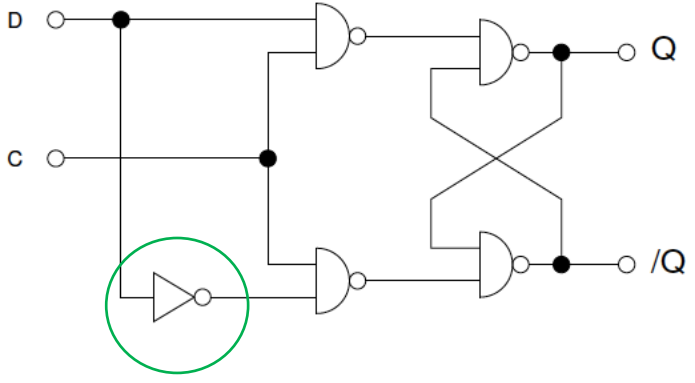

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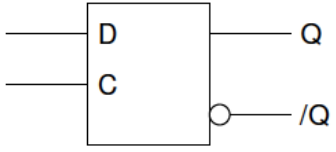

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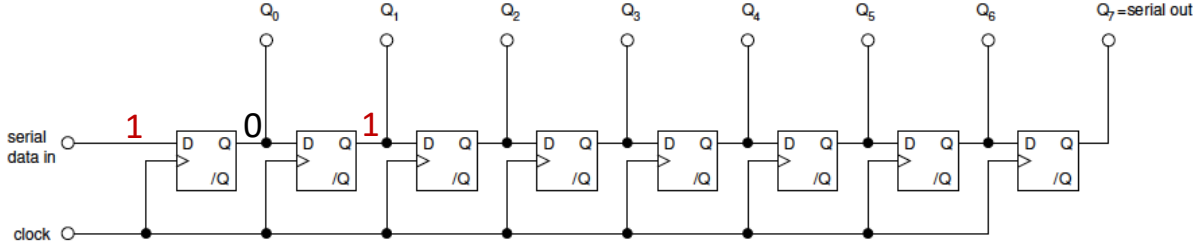

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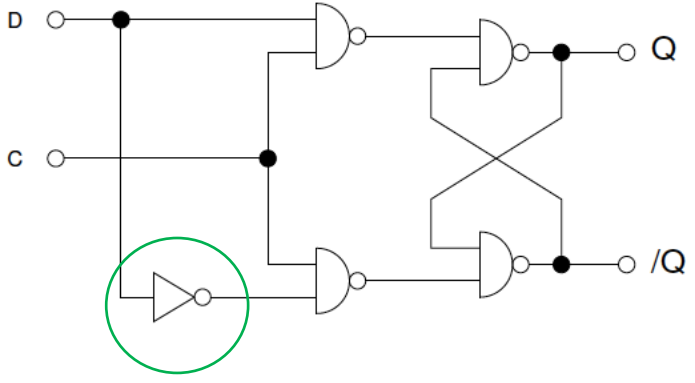

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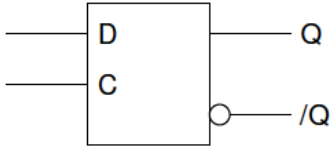

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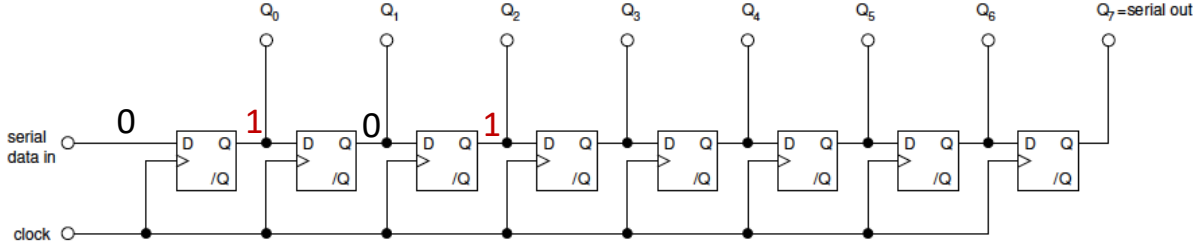


(4) Circuit analysis, topologies

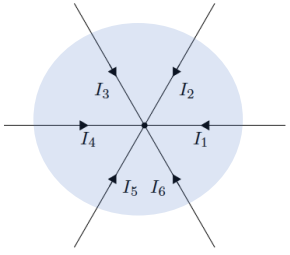
Circuit analysis

Basic circuit analysis can be performed based on the two Kirchhoff laws:

Junction rule or
Kirchhoff's Current Law (KCL):

The currents flowing out of any closed Region of a circuit sum to 0

$$\sum_{k=1}^{n} I_k = 0$$



Loop rule or
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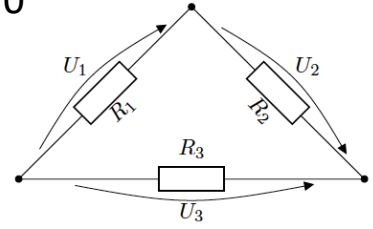

How can we apply these laws to calculate the circuits in an efficient way ?

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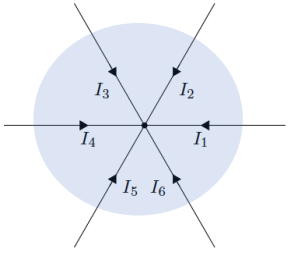

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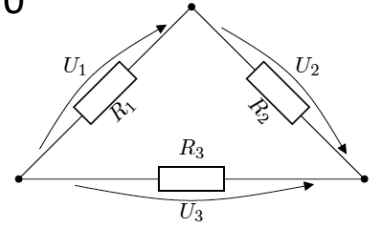


How can we apply these laws to calculate the circuits in an efficient way ?

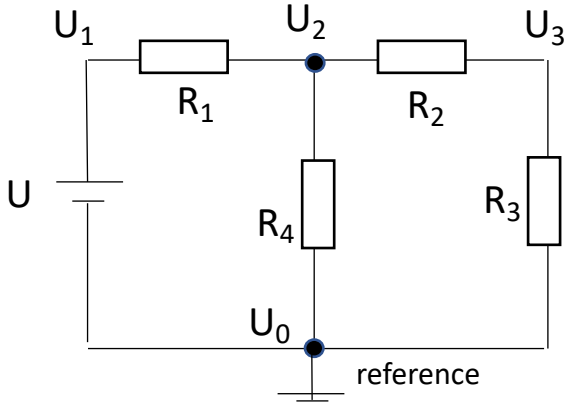
→ Nodal analysis: identify nodes and applies KCL for each node
→ Mesh current analysis: identify essential meshes, assign mesh current and apply KVL
→ Thevenin equivalent: replace part of the network by source + resistance in series
→ Norton equivalent: replace part of the network by source and resistance in parallel

Nodal Analysis

Node: section of the circuit which connects components.
Aim: determine the voltage at each node relative to a reference node, then use them to derive the other relevant quantities

Steps:

- Identify all nodes and assign voltage variables (treat floating or dependent sources as super nodes with internal equation)
- Choose reference node
- Write a KCL equation at each node
- Solve the system of equations (e.g. via matrix inversion)



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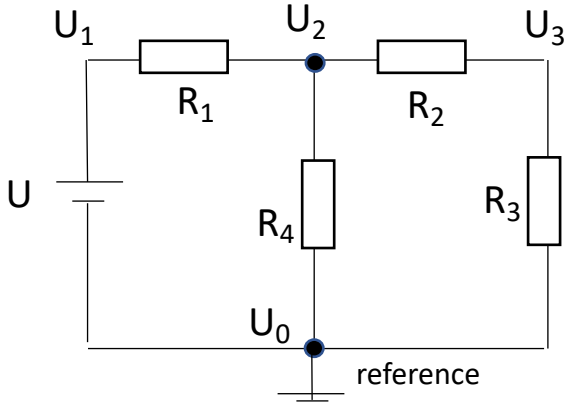

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Example: U_0: $U_0 = 0V$

U_1: $U_1 = U$

U_2 KCL: $\frac{U_1 - U_2}{R_1} = \frac{U_2 - U_0}{R_4} + \frac{U_2 - U_3}{R_2}$

U_3 KCL: $\frac{U_2 - U_3}{R_2} = \frac{U_3 - U_0}{R_3}$

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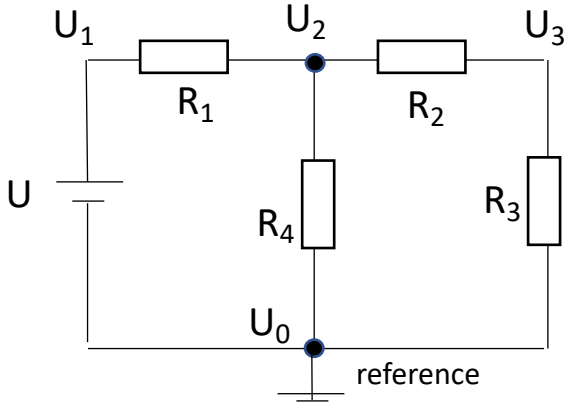

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- conveniently using conductance $G = \frac{1}{R}$ -

$$\rightarrow \begin{bmatrix} G_1+G_2+G_4 & -G_2 \\ G_2 & -G_2-G_3 \end{bmatrix} \begin{pmatrix} U_2 \\ U_3 \end{pmatrix} = \begin{pmatrix} G_1 U \\ 0 \end{pmatrix}$$

- invert matrix or solve by substitution -

$$\rightarrow U_3 = \frac{G_1 G_2 U}{G_2(G_1+G_4)+G_3(G_1+G_2+G_4)} \rightarrow U_2$$

Mesh current Analysis

Essential mesh: loop in the circuit that does not contain any other loop.
Aim: determine the current through each mesh
then use them to derive the other relevant quantities

Steps:

- Identify all essential meshes and assign mesh current
  (special treatment for dependent sources and current sources which are part of two meshes)
- Apply the KVL for each mesh
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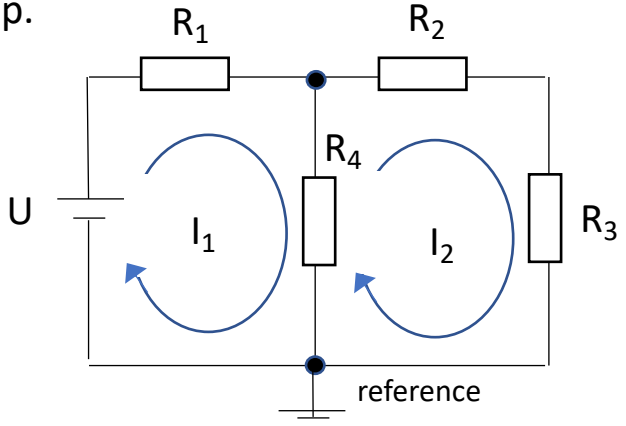

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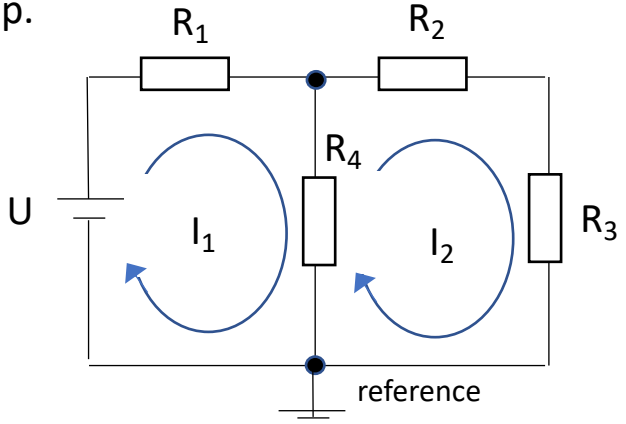

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Mesh 2: $R_4(I_2 - I_1) + R_2 I_2 + R_3 I_2 = 0$

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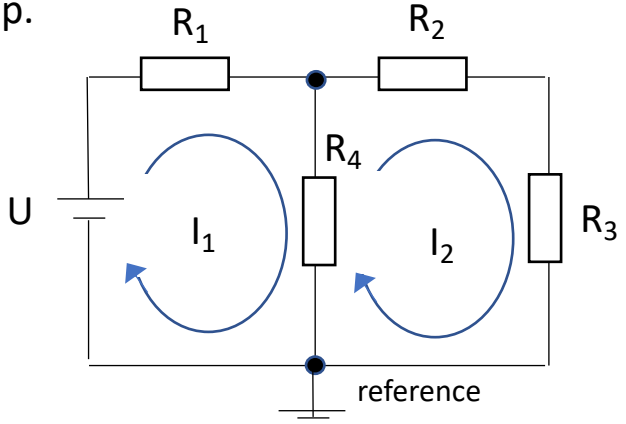

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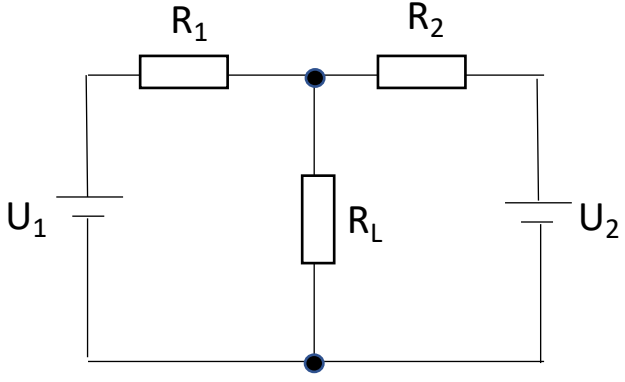
- invert matrix or solve by substitution -

$$\rightarrow I_1 = \frac{(R_2+R_3+R_4)\,U}{(R_1+R_4)(R_2+R_3+R_4)-R_4{}^2} \rightarrow I_2$$

Thevenin equivalent circuit

Thevenin's theorem: Any linear circuit containing several voltages and resistances can be replaced by just one single voltage in series with a single resistance connected across the load"

Example circuit:



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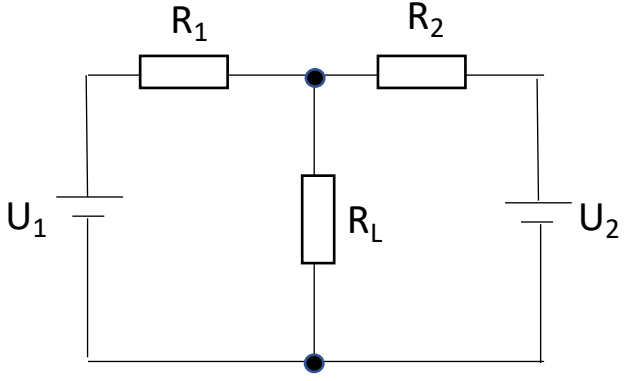
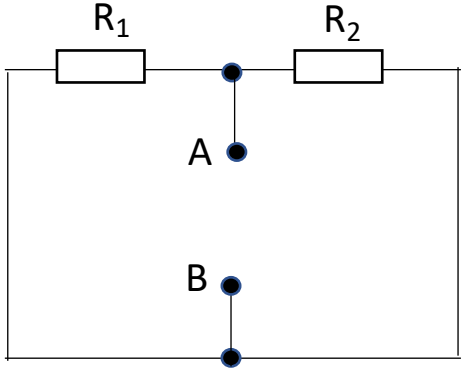


Step1: remove load and shorten sources. Then calculate total Thevenin resistance R_T wrt A/B



$$R_T = R_1||R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

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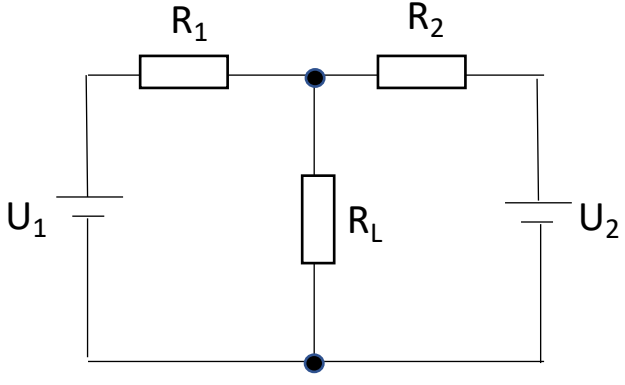

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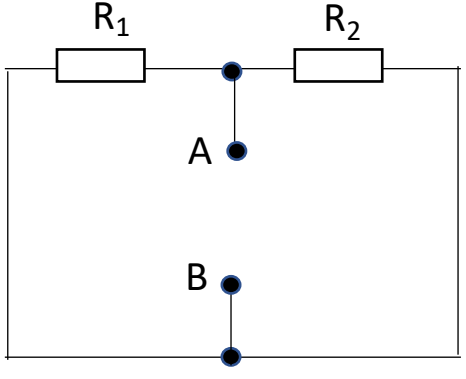
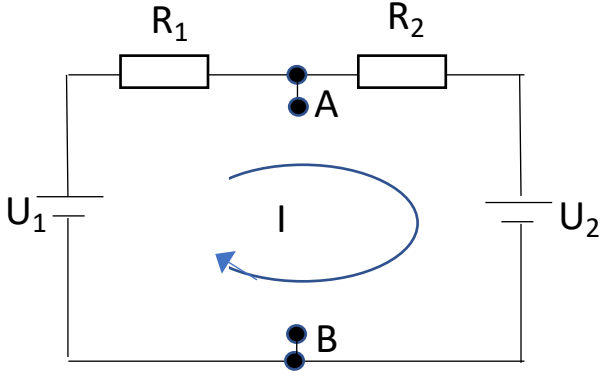


$$R_T = R_1||R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Step2: Reconnect sources. Calculate Thevenin voltage U_T

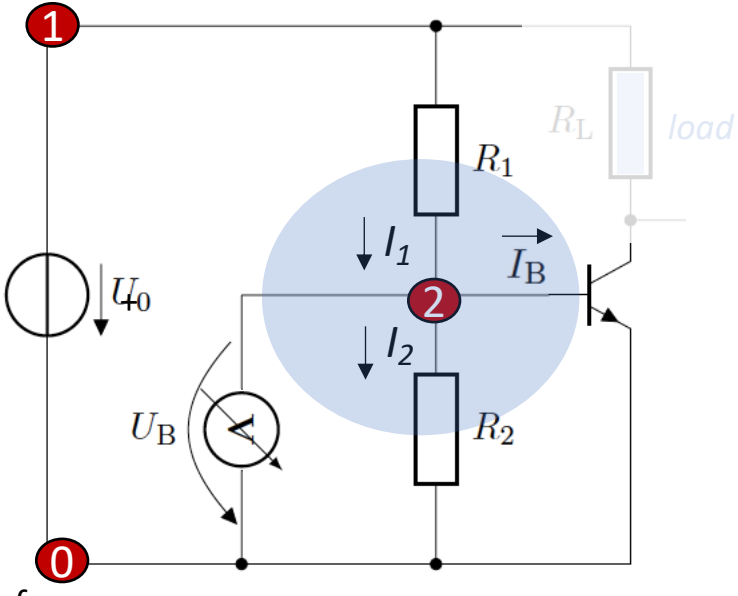


$$I = \frac{U_1 - U_2}{R_1 + R_2}$$

$$U_T = UA_B = U_1 - IR_1 = U_2 + IR_2 = \frac{R_1 U_2 + U_1 R_2}{R_1 + R_2}$$

Example: nodal analysis

Revisiting Voltage divider biasing circuit



Reminder: The voltage U_B across R_2 forward-biases the BE junction

Here: can use **nodal analysis**:
Apply Kirchhoff's current law (KCL) at node 2

Reminder the I_B – U_B relation does not follow Ohms law but a diode-like input characteristics (which for this exercise, we pretend not to know)

U1: $U_1 = U_0$ (1)
U2 KCL: $I_1 = I_2 + IB$ (2)

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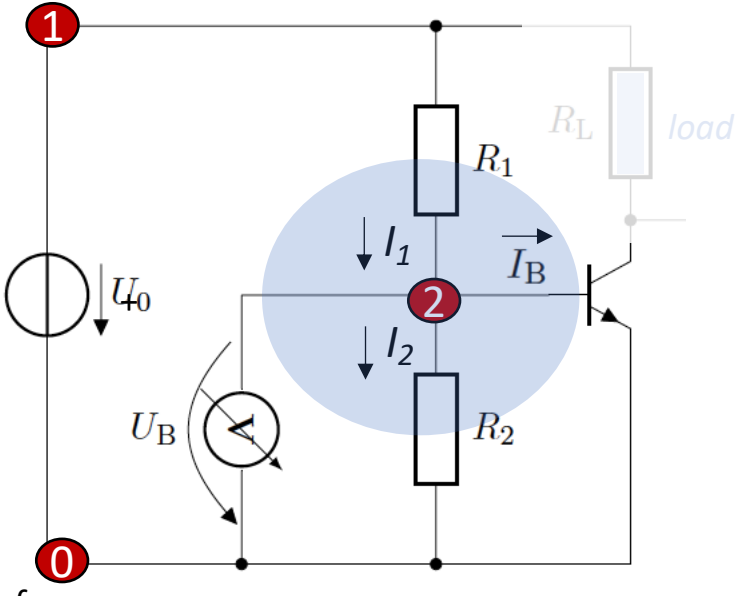

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U_1: $U_1 = U_0$ (1)

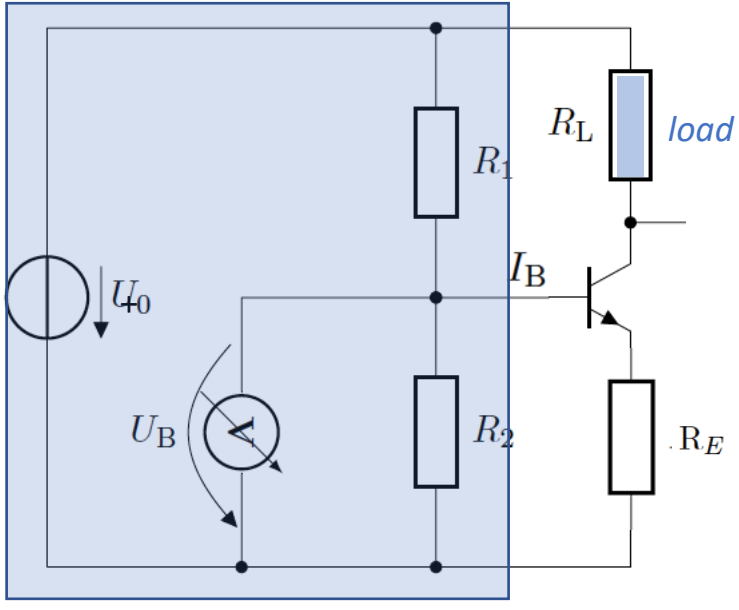
U_2 KCL: $I_1 = I_2 + IB$ (2)

(1) & (2) $\rightarrow \frac{U_0 - UB}{R_1} = \frac{U_B}{R_2} + I_B \rightarrow U_0 - UB = UB\frac{R_1}{R_2} + IB\,R_1 \rightarrow U_B\frac{R_1+R_2}{R_2} = U_0 - I_B\,R_1$

$\rightarrow U_B = U_0\frac{R_2}{R_1+R_2} - I_B\frac{R_1R_2}{R_1+R_2}$

Example: Thevenin equivalent

Voltage divider biasing with emitter resistance



Reminder: We can stabilize the working point by adding an emitter resistance

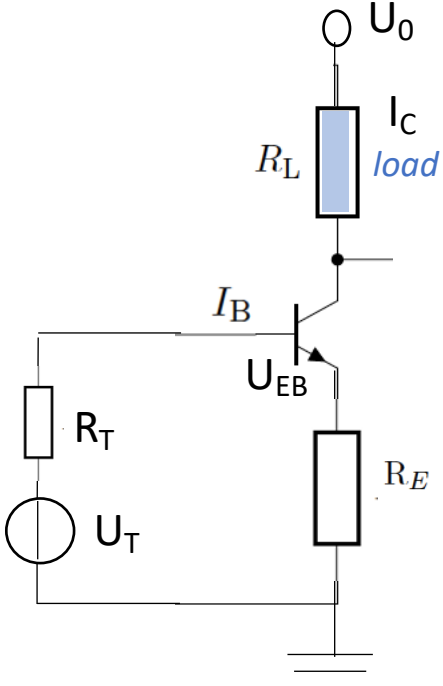
In order to simplify the calculations, we want to replace the voltage divider by the Thevenin equivalent

- Thevenin voltage: $U_T = U_0 \frac{R_2}{R_1+R_2}$

- Thevenin resistance: $R_T = R_1||R_2 = \frac{R_1 R_2}{R_1+R_2}$

Example: Thevenin equivalent

Voltage divider biasing with emitter resistance



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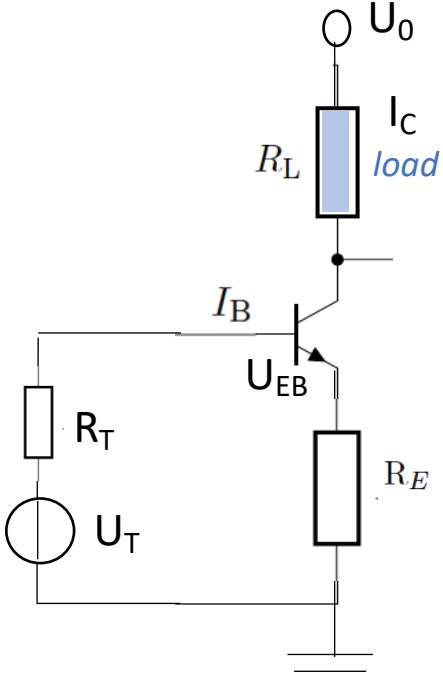

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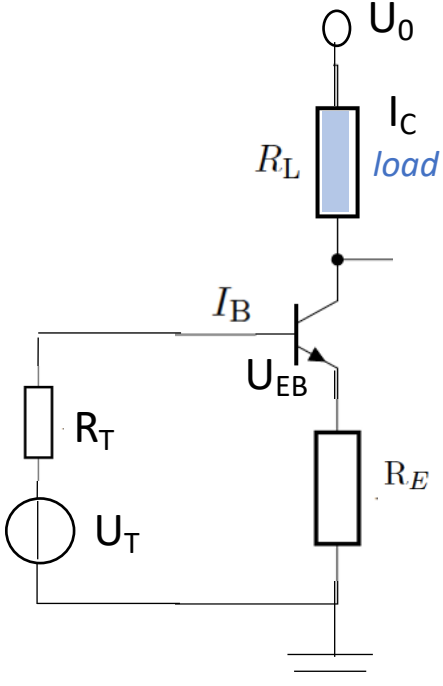

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with $I_C = \beta\, I_B$ (transfer characteristics):

$$U_T = I_B R_T + U_{BE} + RE\, I_B\,(1+\beta)$$

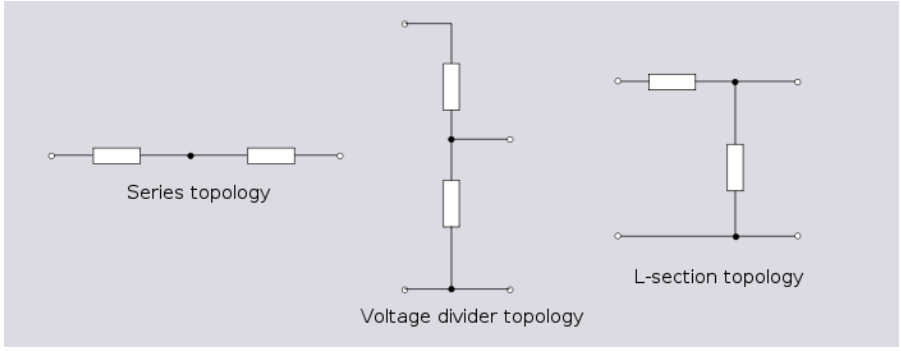
$$\rightarrow I_B = \frac{U_T - UB_E}{R_T + RE(1+\beta)} \rightarrow I_C = \beta IB \rightarrow \ldots.$$

Circuit topologies

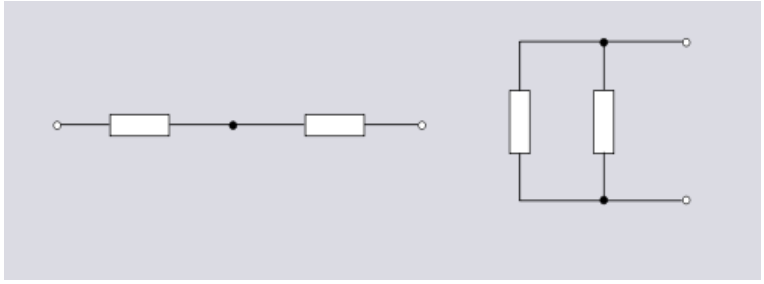
The formal layout of the equations following the application of Kirchhoff's rules applied to a circuit does not depend on the type of device connected in the branches. It only depends on the topology of the circuit.

Circuit Topology describes how components in a network are connected. Circuits with different physical layout can have the same topology.

Example: three circuits with the same topology:



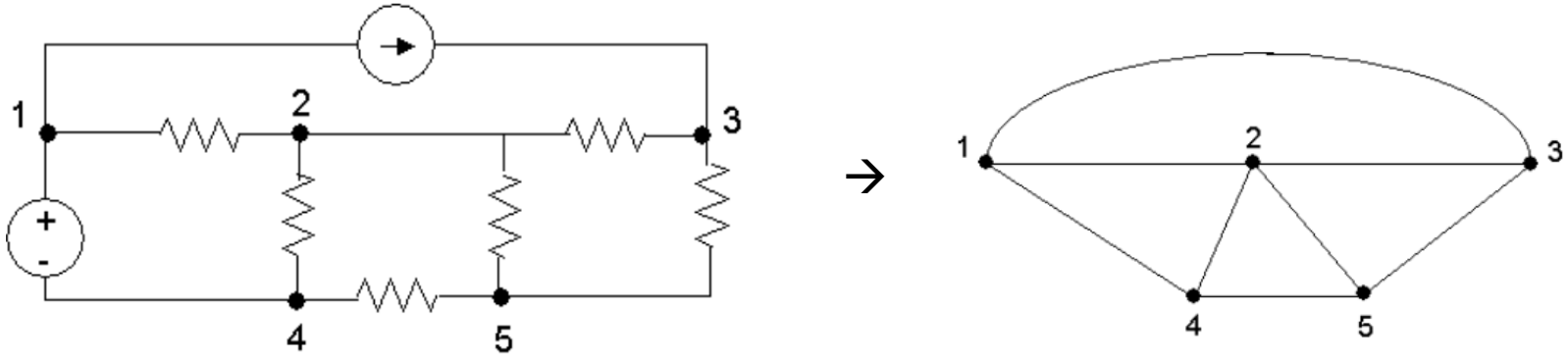
Example: There are only two topologies for a network with 2 branches: series and parallel.



Graph theory

Mathematical ***Graph theory*** is used to analyze the topology:
Graphs represents the aspects of a network connected to its topology. The devices are left out.
→ a line represents a device. A nod represents all points at the same potential.

Example: ***circuit*** ***graph***



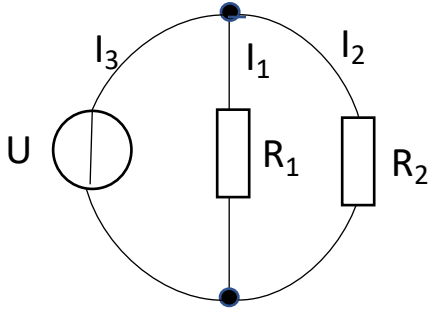
The graph representation makes it easier to analyze complex circuits.
Graphs are ***equivalent*** if they can be transformed into each other by translation, rotation, reflection, stretching or crossing/knotting the branches,

Graph theory: dual graph

*Each graph has a **dual graph** with the following elements exchanged:*

- *R ←→ 1/R*
- *L ←→ C*
- *U ←→ I*
- *U source ←→ I source*
- *mesh ←→ node*

graph



$$I_3 = -I_1 - I_2 = U(\frac{1}{R_1} + \frac{1}{R_2})$$

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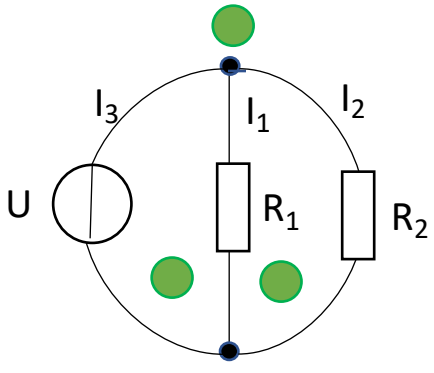

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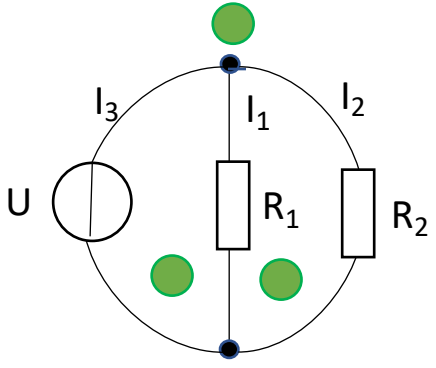
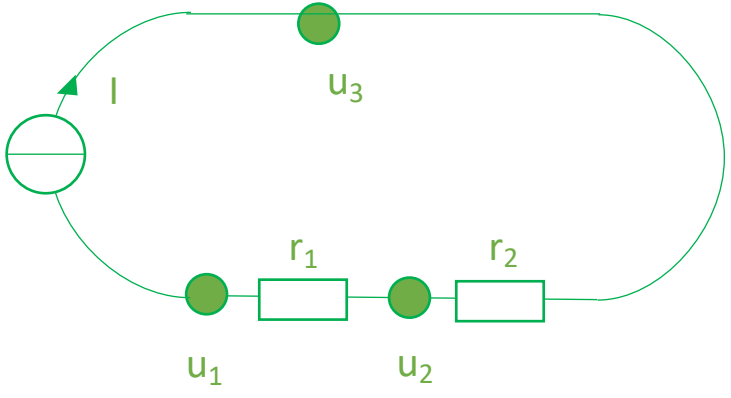


←→

dual graph



converted parallel circuit into serial circuit

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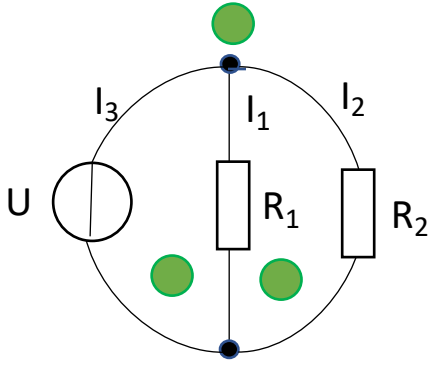

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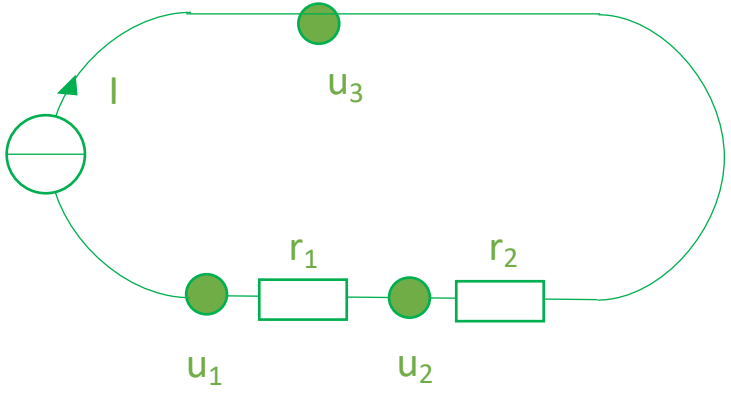


converted parallel circuit into serial circuit

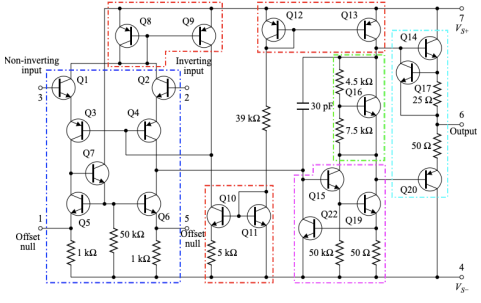
both solutions are equivalent as U ←→ I

$$I_3 = -I_1 - I_2 = U(\frac{1}{R_1} + \frac{1}{R_2})$$

$$u_3 - u_1 = I(r_1 + r_2) = I(\frac{1}{R_1} + \frac{1}{R_2})$$

Literature

(1) Reminder: Electrical circuits
(2) Analog electronics
(3) Digital electronics
(4) Circuit analysis, circuit topologies



Literature:

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The Art of Electronics
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D. Sundararajan
Introductory Circuit Theory
Springer (2019)