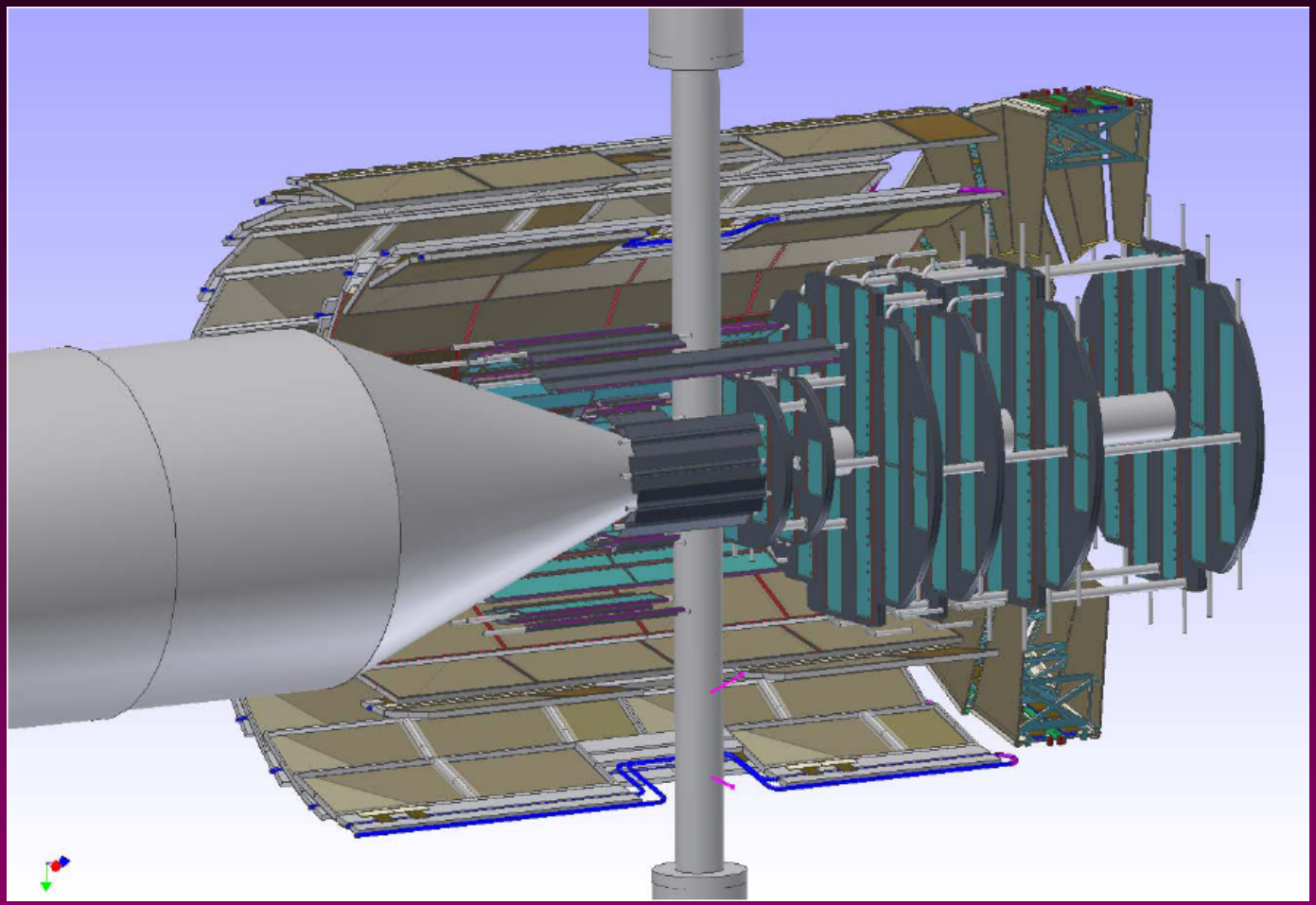
Pixel detector

Sezione di Torino

PANDA Micro Vertex Detector
pixel readout architecture

PANDA MVD

Sezione di Torino



- Barrel :

Layer 1 : radius 28 mm, SPDs

Layer 2 : radius 53 mm, SPDs

Layer 3 : radius 92 mm, SSDs

Layer 4 : radius 120 mm, SSDs

- Forward :

Disks 1-2 : radius 37.5 mm, SPDs

Disks 3-4 : radius 75 mm, SPDs

Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel specs

Sezione di Torino

Pixel size	100 × 100 μm^2
Chip active area	11.4 × 11.6 mm^2 (116 rows, 110 cols)
dE/dx measurement	ToT, 12 bits dynamic range
Max input charge	50 fC
Noise floor	<32 aC (200 e$^-$)
Clock frequency	155.52 MHz
Time resolution	6.45 ns (1.9 ns *r.m.s.*)
Power consumption	< 500 mW/cm^2
Max event rate	*see next slide*
Total ionizing dose	< 100 kGy

Data rates *(worst case scenario)*

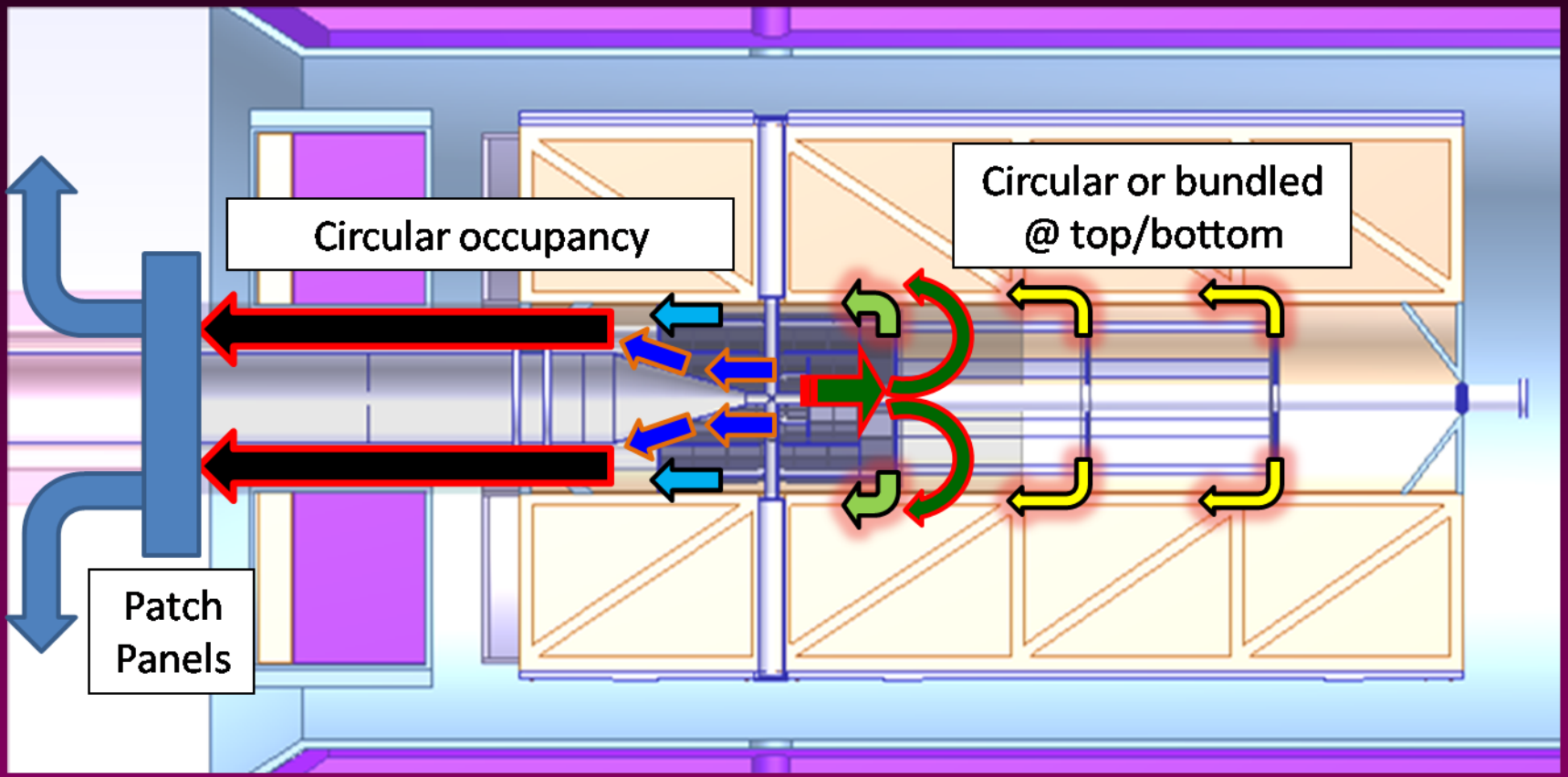
Sezione di Torino

antiproton-	proton (disk)	Au (barrel)
Particle rate per $cm^2 \cdot s$	$6 \cdot 10^6$	$1.6 \cdot 10^6$
Data rates per cm^2 (per chip)[Mb/s] :		
no multiple hit *(avg)*	300 (397)	80 (110)
multiple hits, 100 µm sensor *(avg)*	450 (595)	120 (160)
multiple hits, 200 µm sensor *(avg)*	750 (992)	200 (260)
multiple hits, 100 µm sensor *(max)*	675 (893)	180 (240)
multiple hits, 200 µm sensor *(max)*	1125 (1488)	300 (398)

Chip sensitive area : 1.32 cm^2
Avg rate : $20 \cdot 10^6$ annihilations/s
Max rate : $30 \cdot 10^6$ annihilations/s

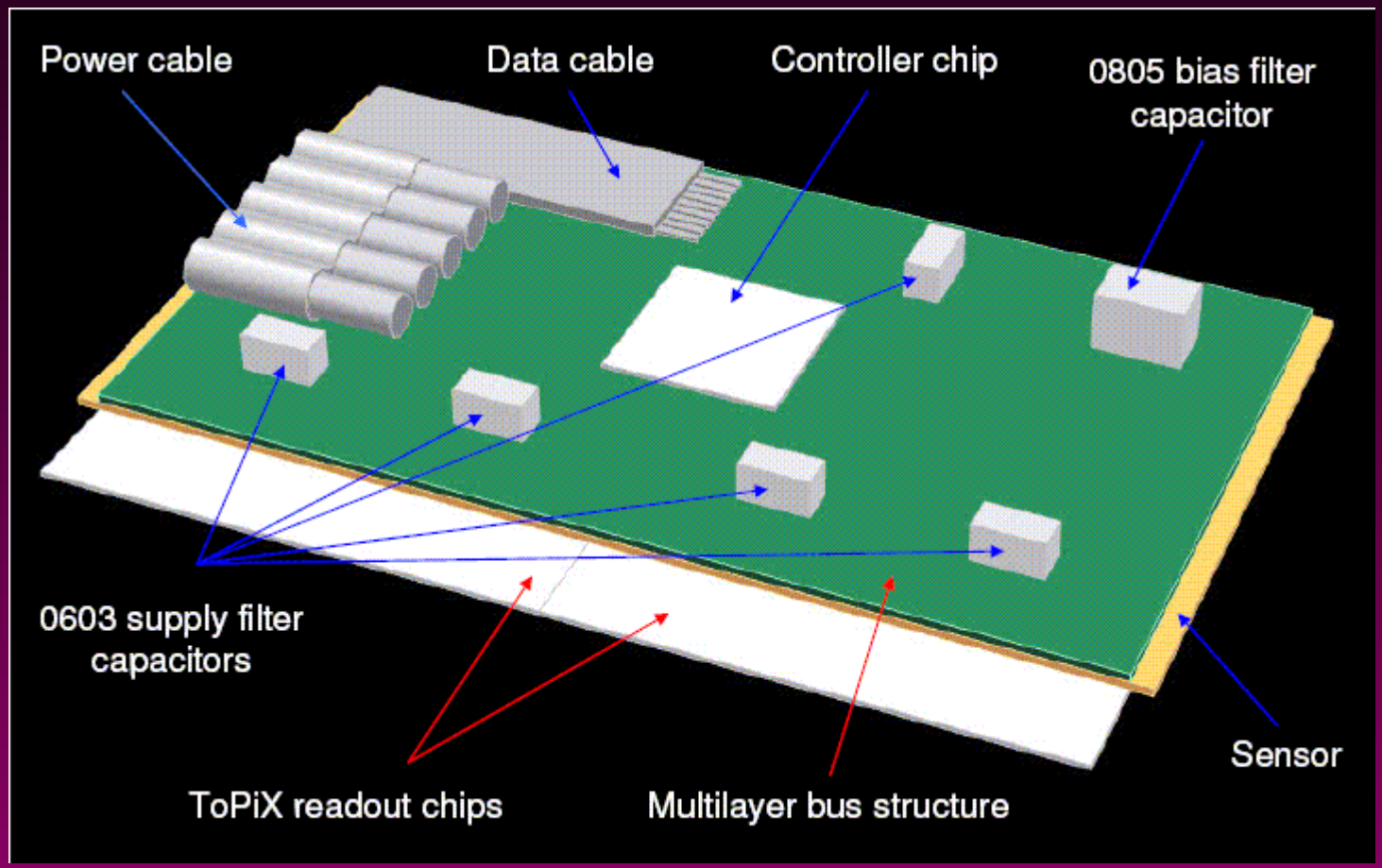
Routing direction

Sezione di Torino



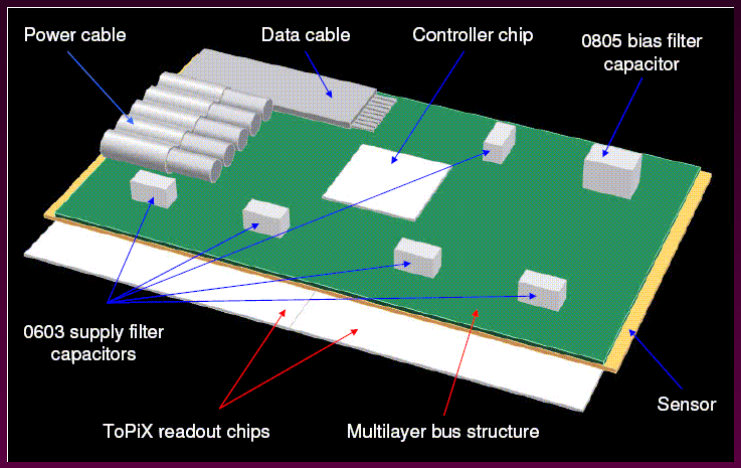
Module concept

Sezione di Torino

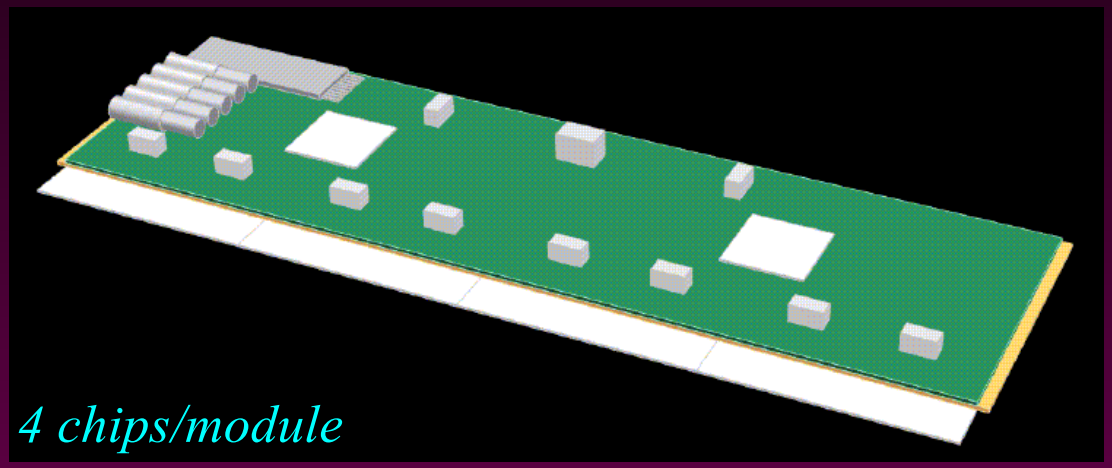


Module types

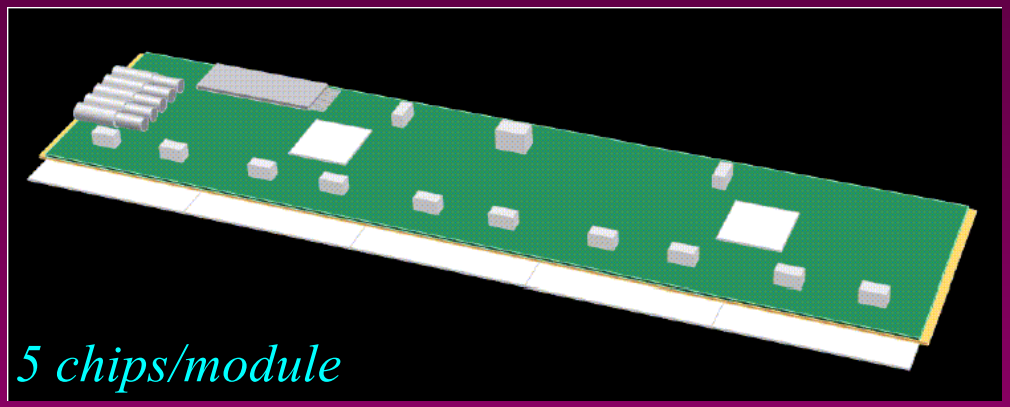
Sezione di Torino



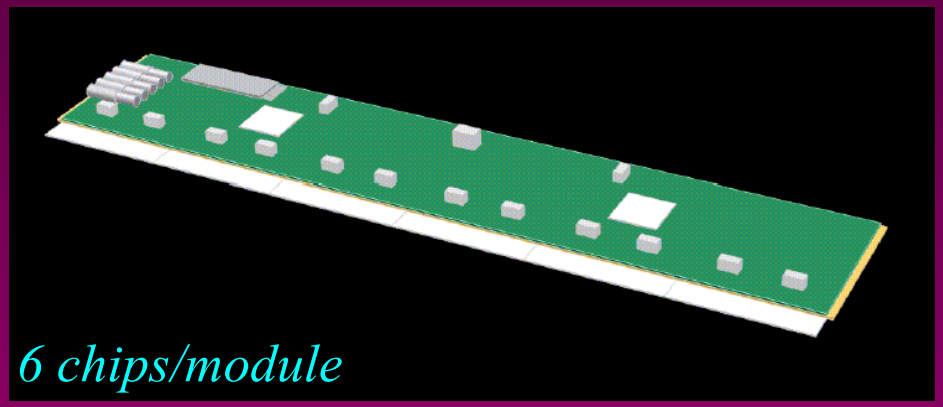
2 chips/module



4 chips/module



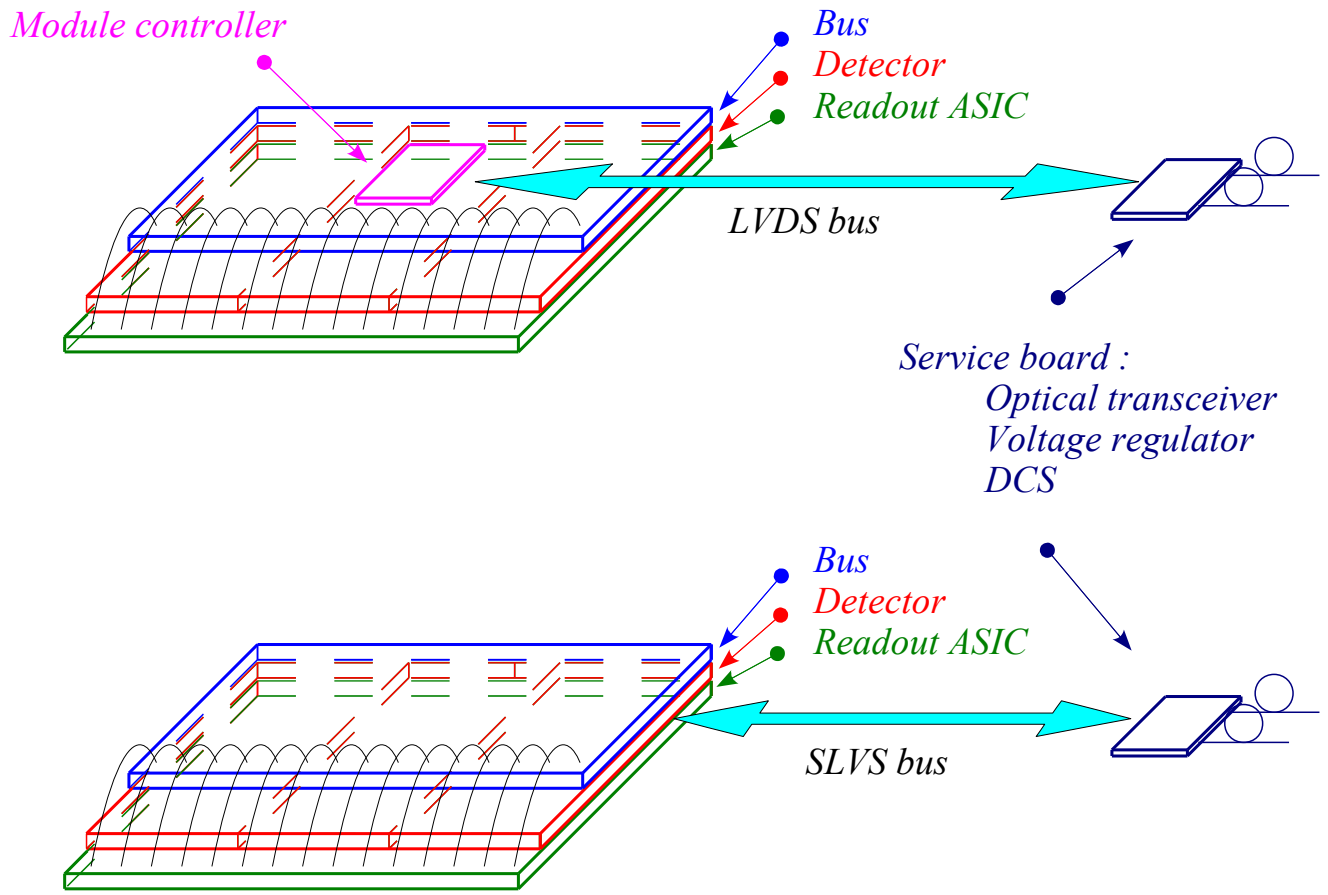
5 chips/module



6 chips/module

Readout scheme

Sezione di Torino



Option 1

Option 2

Readout options

Sezione di Torino

- Option 1
  - ☺ reduced number of cables
  - ☺ simpler ToPiX control logic
  - ☺ better management of data rate increase
  - ☹ requires an extra chip
- Option 2
  - ☺ no need of an extra chip
  - ☺ interface already under development at CERN
  - ☹ more cables

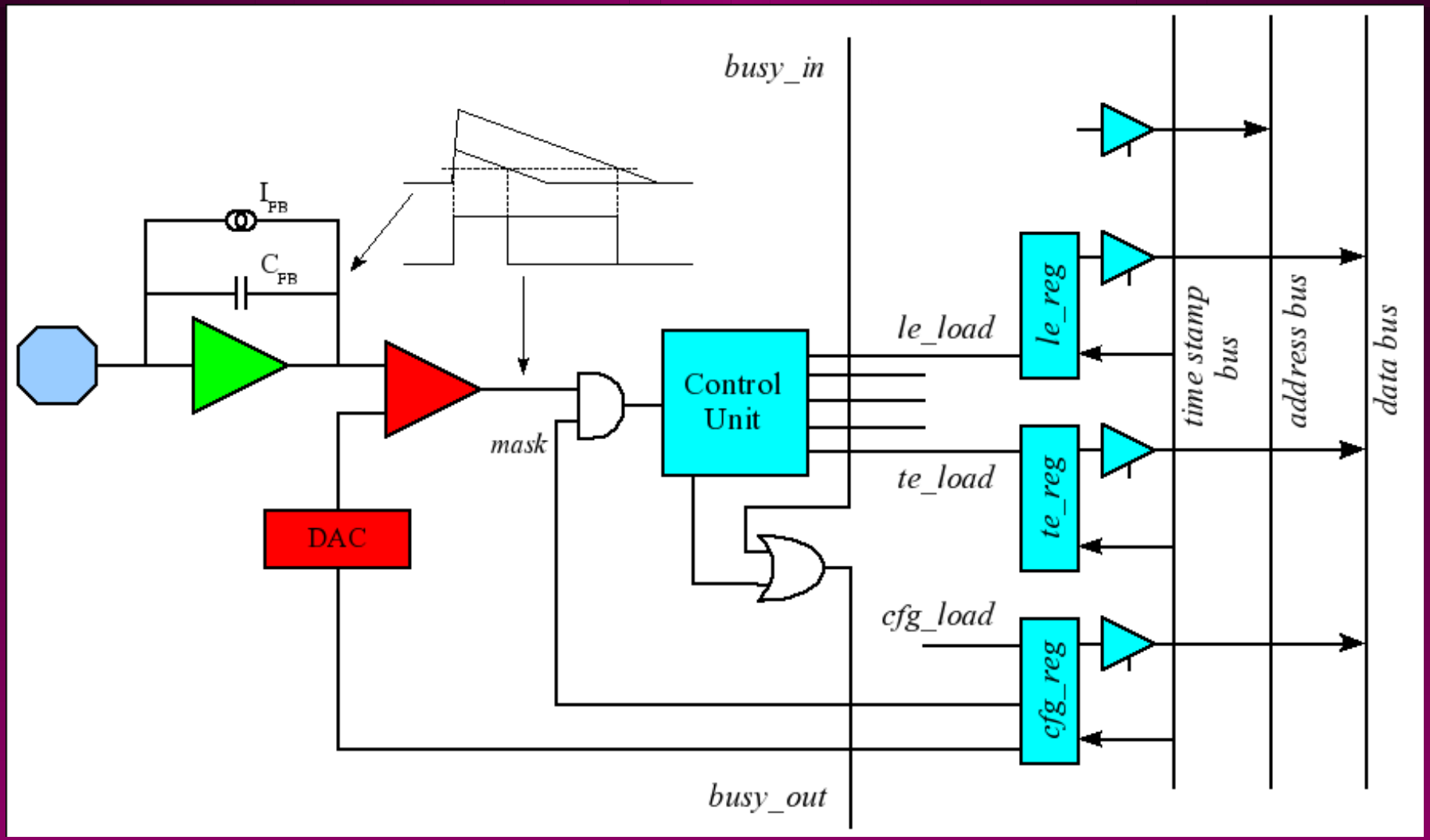
ToPiX ASIC

Sezione di Torino

- Custom development for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Each event has a 12 bits time reference
- Double rate serial readout
- Radiation tolerant
- Data corresponding to a 12 bits counter cycle (26.21 μs) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)

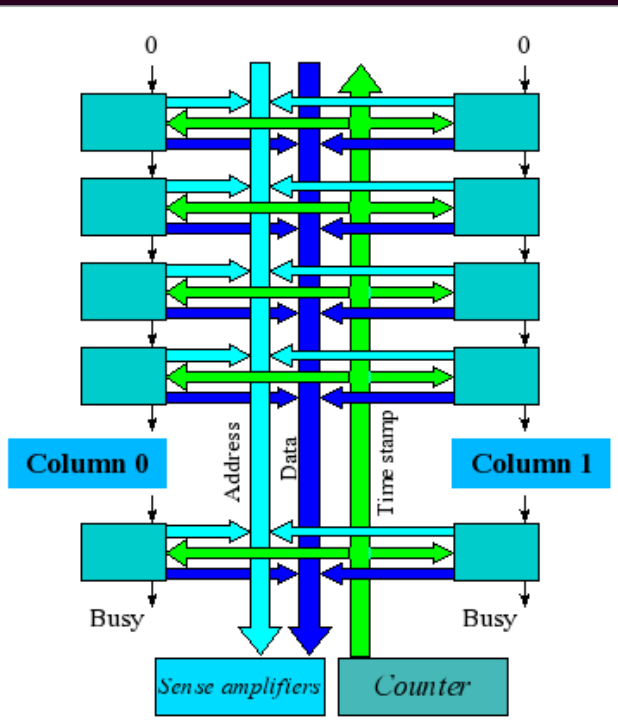
Pixel cell

Sezione di Torino



ToPiX block diagram

Sezione di Torino

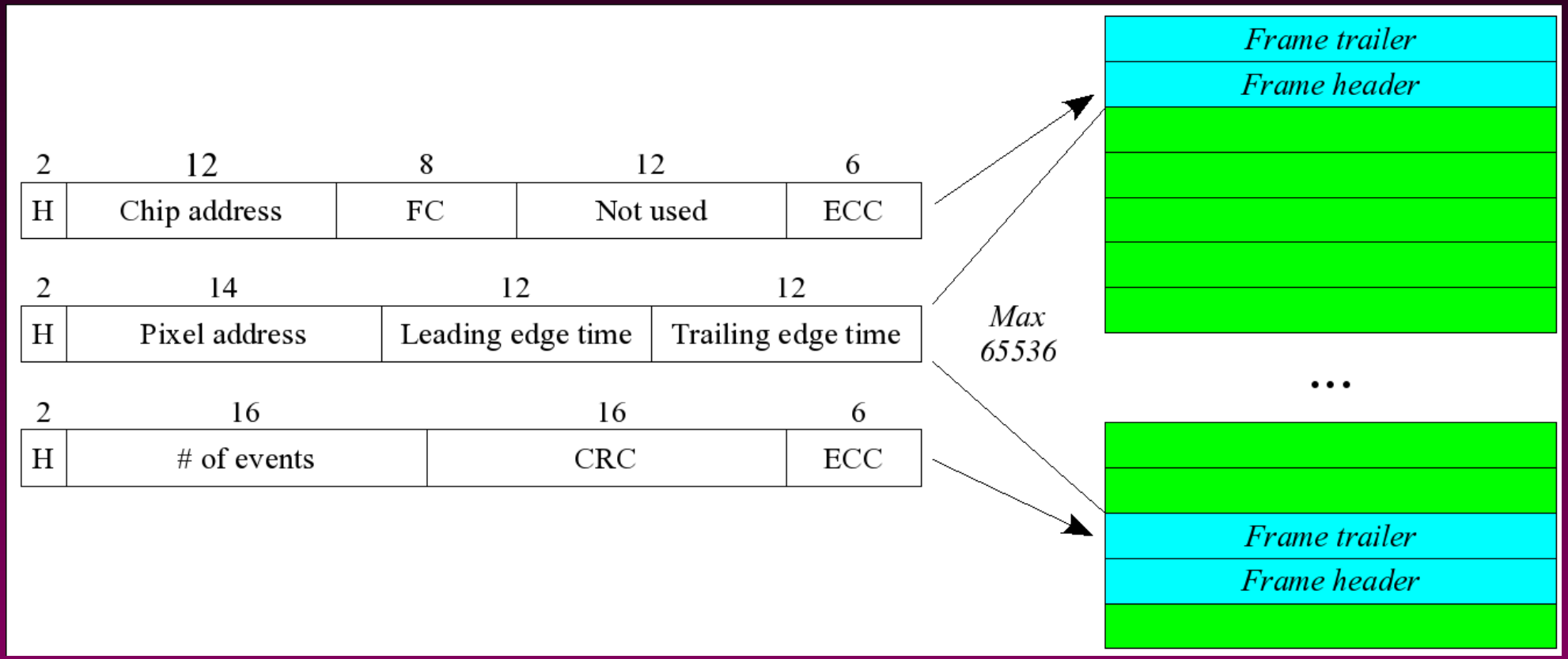


Double column structure
Common time reference
Readout data :
- Address
- Leading edge time
- Trailing edge time

End of column buffering
Serial data out

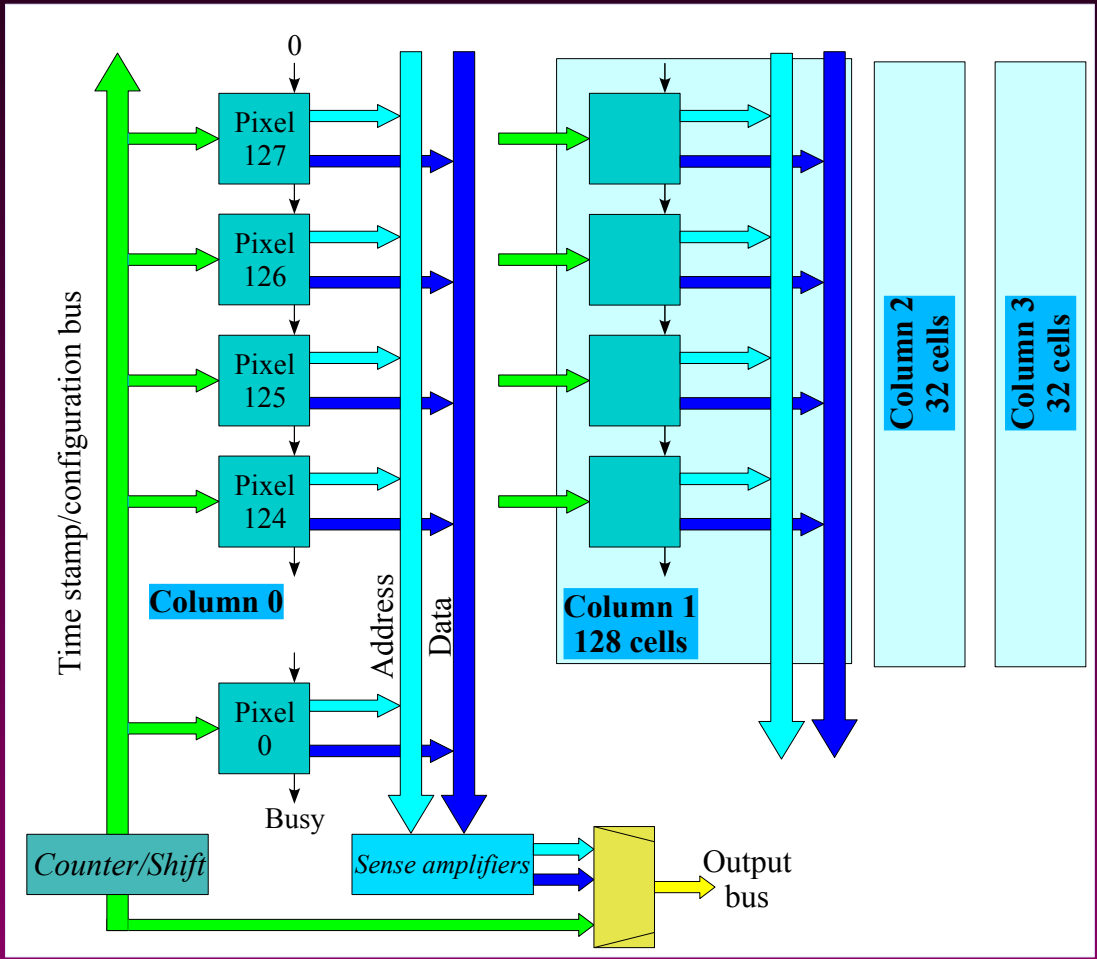
Data format

Sezione di Torino



ToPiX v2 architecture

Sezione di Torino



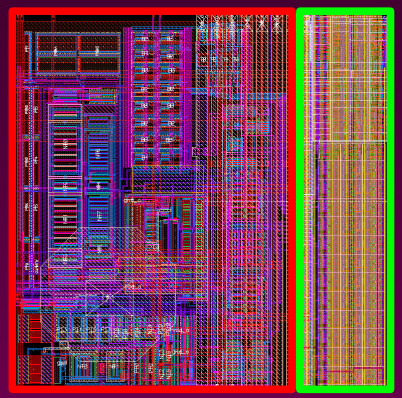
- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 µm technology
- SEU tolerant logic (based on the DICE cell)

ToPiX v2

Sezione di Torino

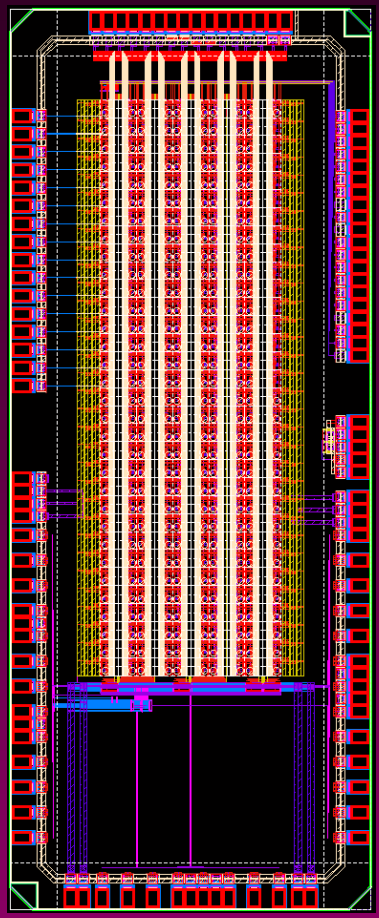
Pixel cell

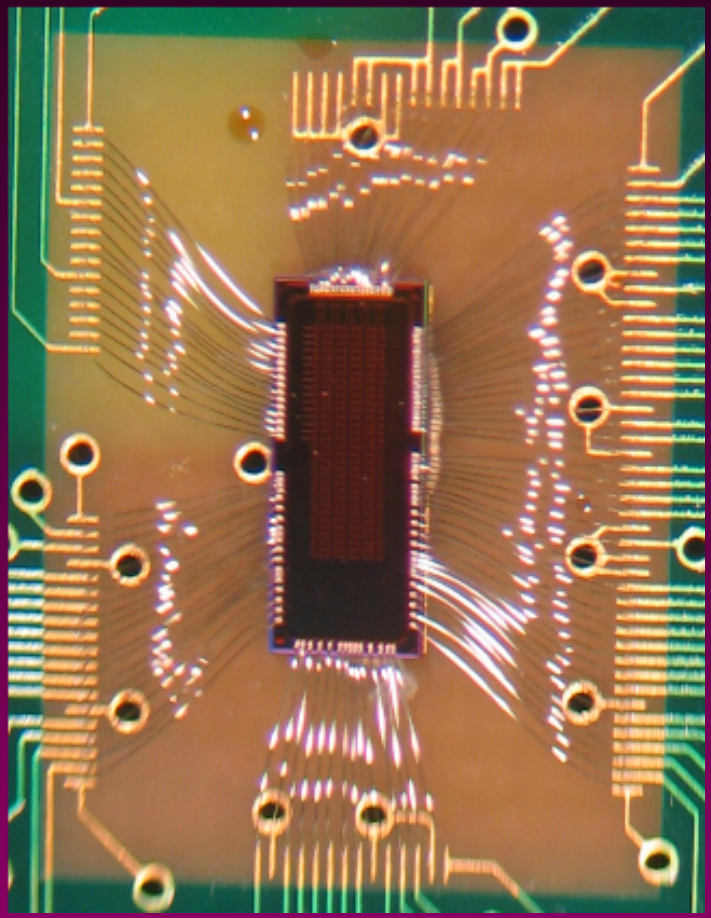
100 µm × 100 µm



Analog *Digital*

ToPiX prototype 5 mm × 2 mm





ToPiX v2

Sezione di Torino

Tests :

- electrical
- connected to a detector via wire bonding
- TID tests
- SEU tests

References :

D. Calvo et al, *A Silicon Pixel Readout ASIC in CMOS 0.13 µm for the PANDA MicroVertex Detector* , Nuclear Science Symposium Conference Record, 2008 IEEE, 19-25 Oct. 2008 Page(s): 2934 – 2939

D. Calvo et al., *The silicon pixel system for the Micro Vertex Detector of the PANDA experiment* – doi:10.1016/j.nima.2009.09.043

T. Kugathasan, et al., *Front end electronics for pixel detector of the PANDA MVD* - Proceedings of the Topical Workshop on Electronics for Particle Physics 21-25 Sep 2009 - Paris, France - CERN 2009-006, pag. 52-56

ToPiX v3

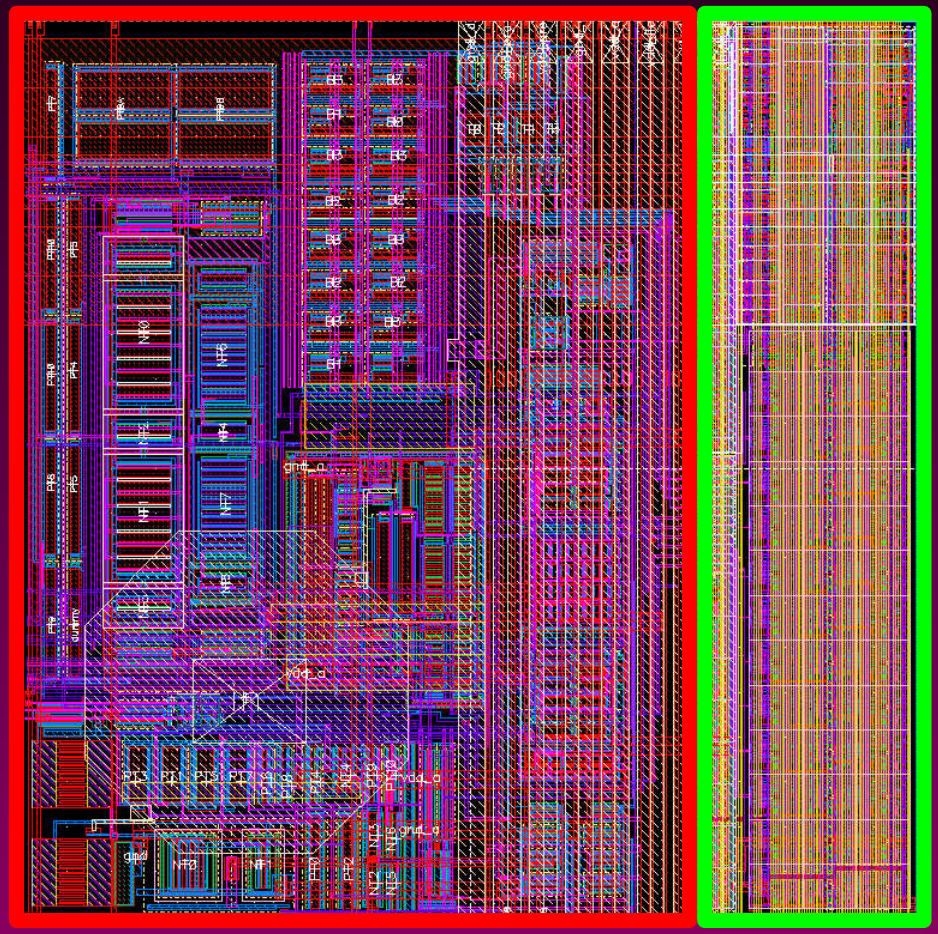
Sezione di Torino

- Layout submitted on February 7th – *just received*
- 4.5x4 mm^2 die area
- CMOS 0.13 μm DM technology
  - LM → 6 thin, 2 thick metal layers
  - DM → 3 thin, 2 thick, 3 RF metal layers
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding

Cell layout

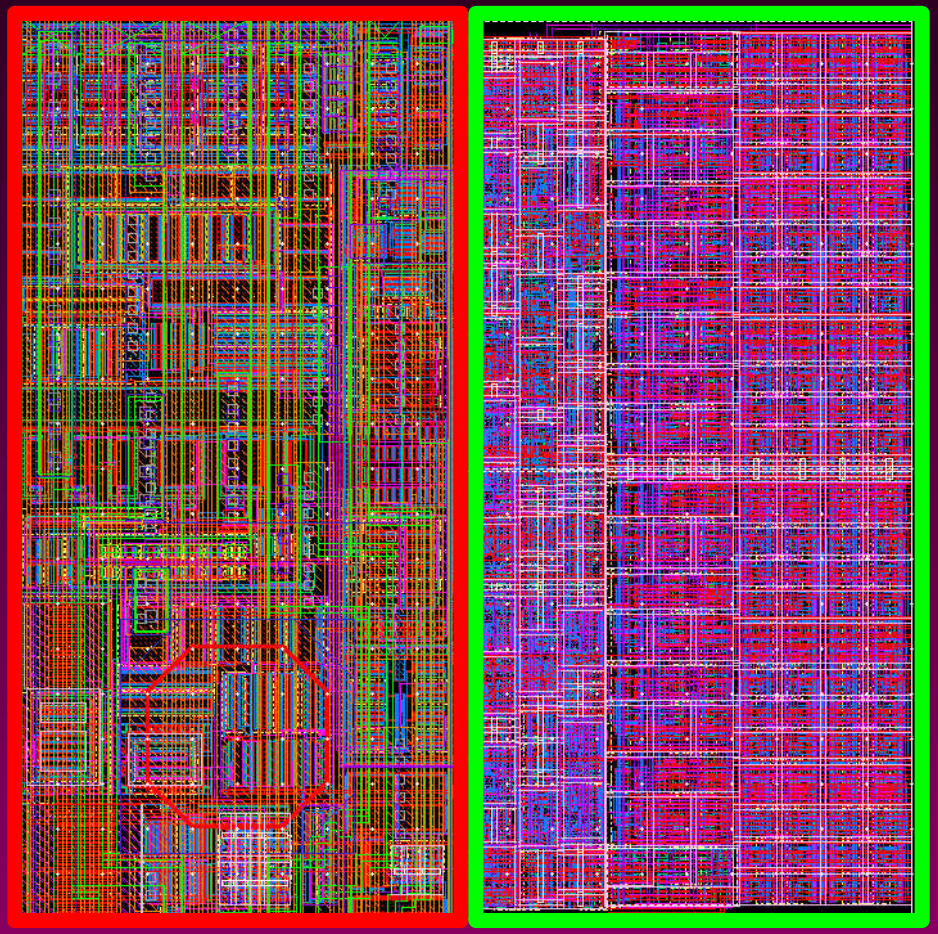
Sezione di Torino

ToPiX v2



Analogue *Digital*

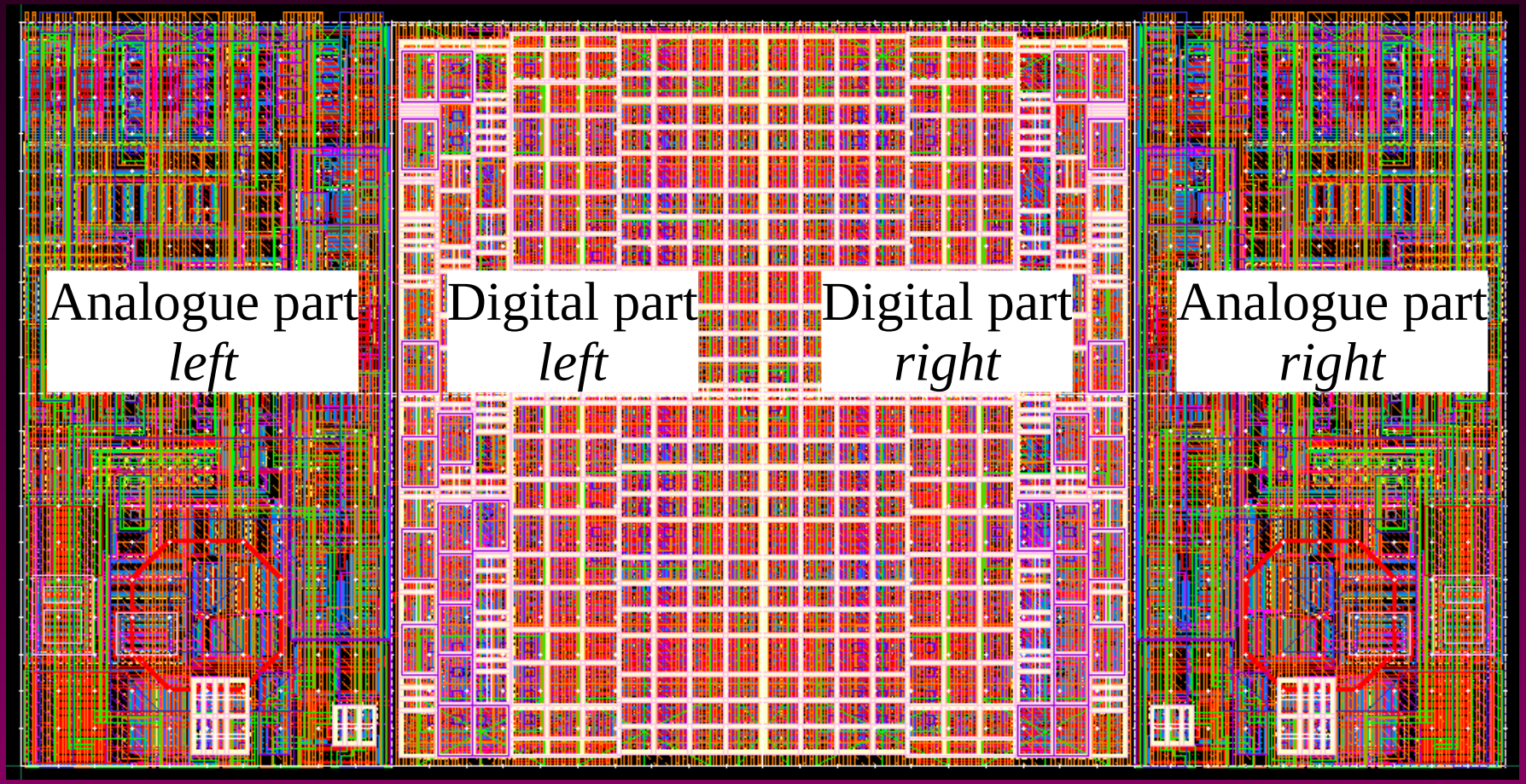
ToPiX v3



Analogue *Digital*

Double cell

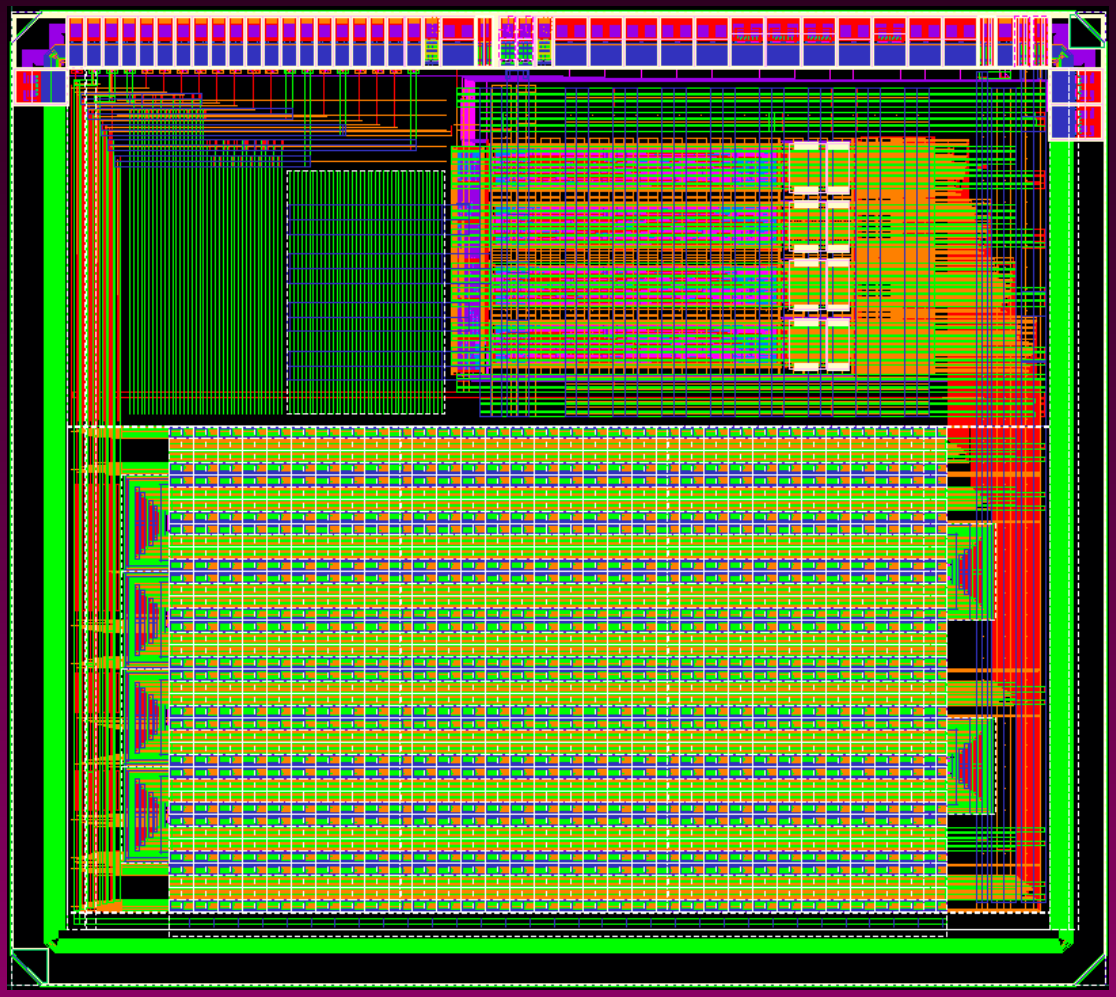
Sezione di Torino



Common bus

ToPiX v3 layout

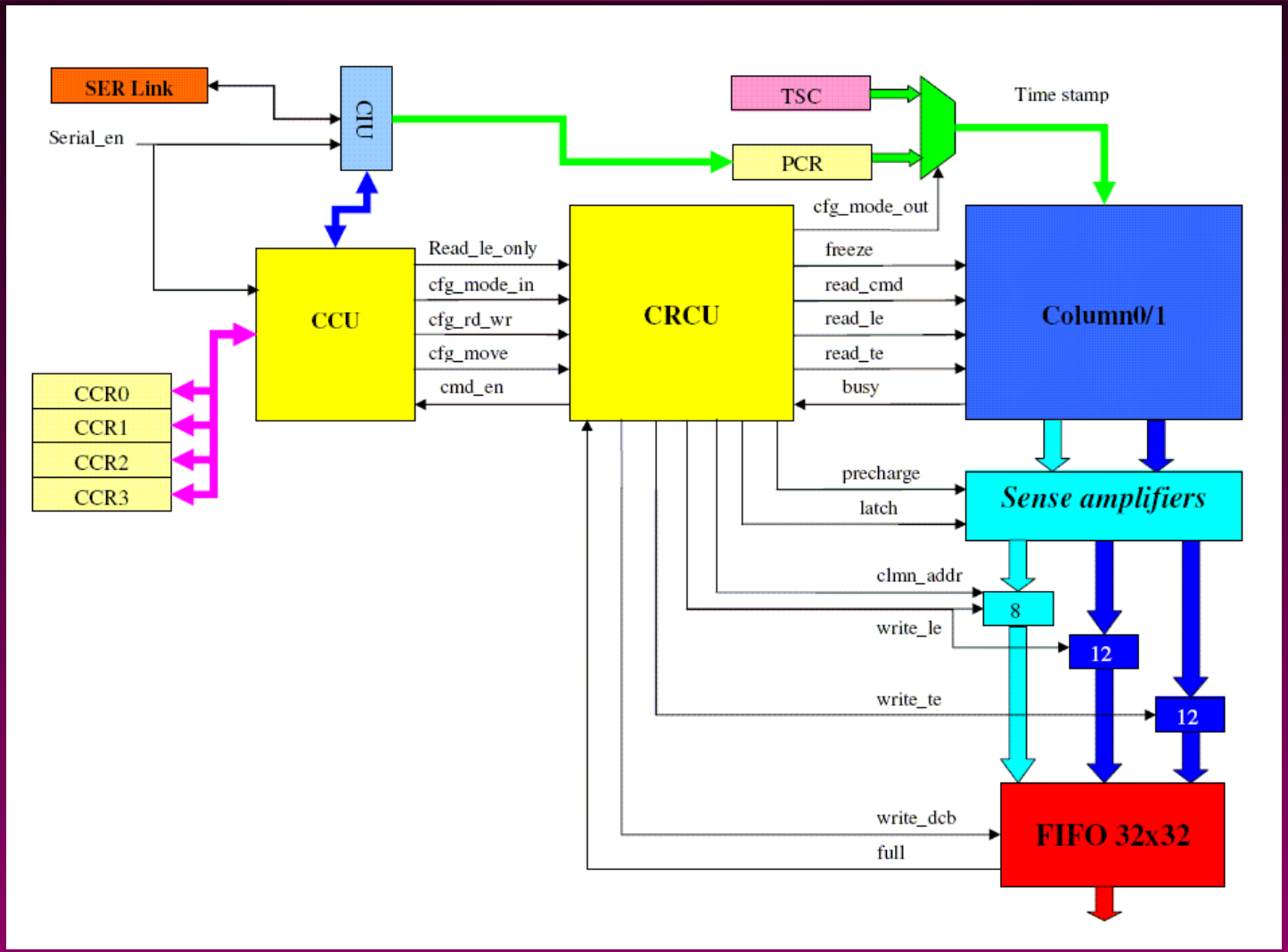
Sezione di Torino



- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

End of column

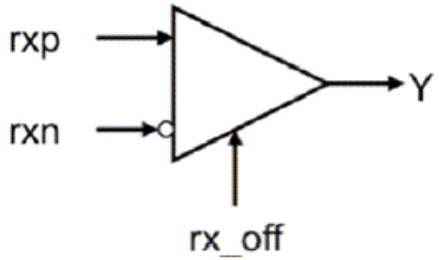
Sezione di Torino



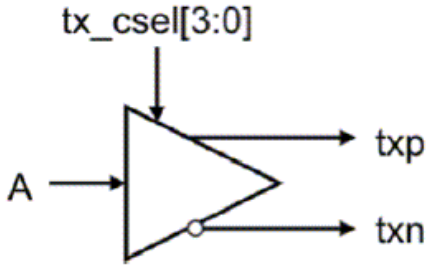
SLVS

Sezione di Torino

- Receiver
  - *Power Supply: 1.2V to 1.5V*
  - *Power Dissipation:*
    - *150uW @ 320Mbs, 1.2V supply*
    - *<1uW @ power down*



- Driver
  - *Power Supply: 1.2V to 1.5 V*
  - *Power Dissipation:*
    - *3.1mW @ 320Mbs, 1.2 V supply*
    - *<10uW @ power down*



- Engineer
  - Sandro Bonacini – CERN, Switzerland

Electrical Specifications

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_{OD}	Differential output voltage		110	200	320	mV
ΔV_{OD}	Differential output voltage change	(fig.1)	0	14	20	mV
V_{OS}	Driver offset voltage		100	200	350	mV
I_{SCO}	Output short-circuit current	V_{OS}=0, V_{OD}=0		-25	-60	mA
I_{SCOD}	Differential output short-circuit current	V_{OD}=0		-3	-5	mA
I_{DD}	Supply current			2.5	4.0	mA

Programmable Output Current

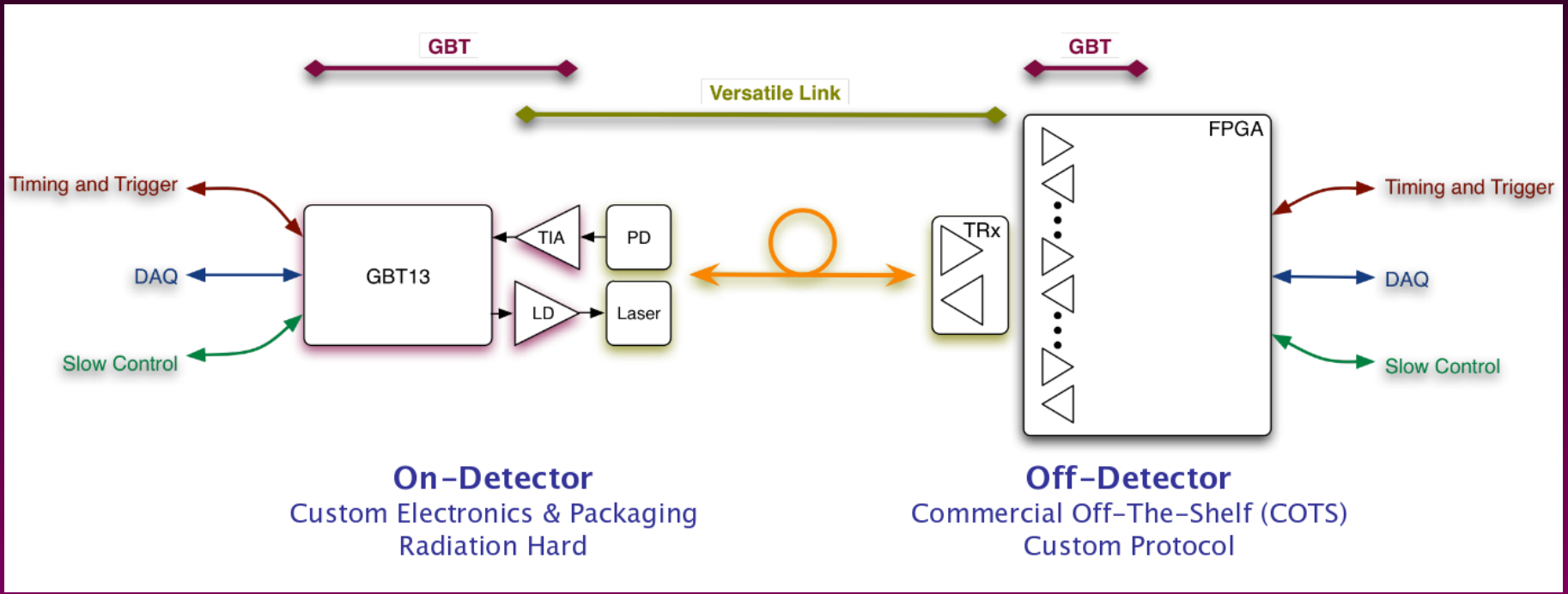
csel[3:0]	Output current [mA]	Driver power dissipation [mW]
8	2.0	3.0
4	1.3	2.1
2	0.8	1.4
1	0.5	1.0
(sleep) 0	0	<.01

Note: All values are given at 1.2V power supply voltage, typical conditions.

CERN development (*S. Bonacini*)
SLVS Driver test with Al cables ongoing

GBT

Sezione di Torino



GBT chipset

Sezione di Torino

Radiation tolerant chipset :

- GBTIA : Transimpedance optical receiver
- GBLD : Laser driver
- GBTx : Data and Timing Transceiver
- GBT-SCA : Slow control ASIC

Target Applications :

- Data readout
- TTC
- Slow control and monitoring links

Supports :

- Bidirectional data transmission
- Bandwidth :
  - → Line rate : 4.8 Gb/s
  - → Effective : 3.36 Gb/s

Radiation Tolerance :

- Total dose
- Single Event Upset

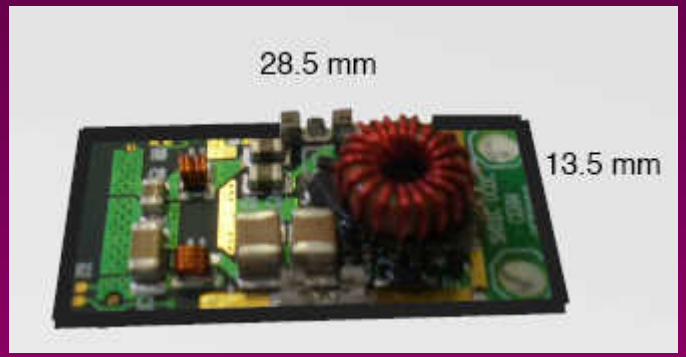
Power regulator

Sezione di Torino

- ToPiX power supply 1.2 V – I_{DC} ~ 500 mA (estimated)

  → voltage drop on cables is not negligible
- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.8÷3.3 V, I_{OUT} < 3 A
- V_{OUT}=1.2 V seems feasible
- Board position t.b.d.

  → *ToPiX internal regulator t.b.d.*



Conclusions

Sezione di Torino

- A pixel readout architecture has been defined – waits for more detailed rate simulations to be finalized.
- F/E ASIC with full pixel cells and columns has been designed and tested – a new prototype, with full end of column logic has been submitted to foundry.
- A GBT-based interface to the DAQ system is under evaluation. Contacts with the CERN GBT group ongoing.
- Started discussion with a CERN group for radiation tolerant DC-DC converter. A solution based on the AMIS ASIC is under evaluation.

Next steps

Sezione di Torino

- Test of ToPiX v3 *(G. Mazza, M. Mignone, A. Rivetti, R. Wheadon)*
- Simulations of the ToPiX updated architecture with the data ← input from simulations *(L. Zotti)*
- ToPiX more accurate power estimation (from v3 tests) → input to cooling design *(S. Coli)*
- 1st approximation definition of the data trasmission board and the power regulator board → input to mechanical design *(G. Giraudo)*
- New aluminium cables testing with SLVS drivers *(P. De Remigis)*
- Bump bonding with detector, test beam preparation *(D. Calvo, M. Mignone, R. Wheadon)*