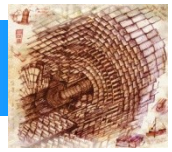
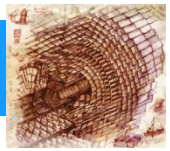


Pixel Upgrade plan and INFN proposed contributions

G.M. Bilei

Pixel Upgrade motivations and requirements

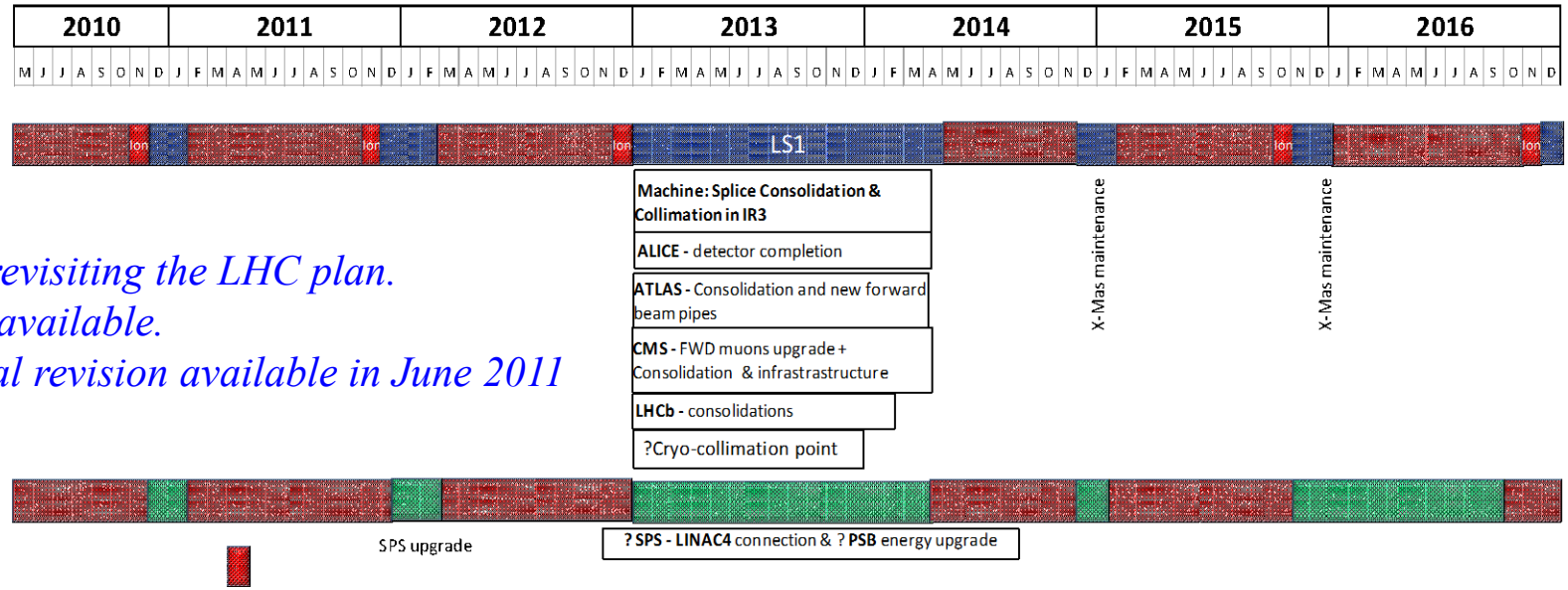


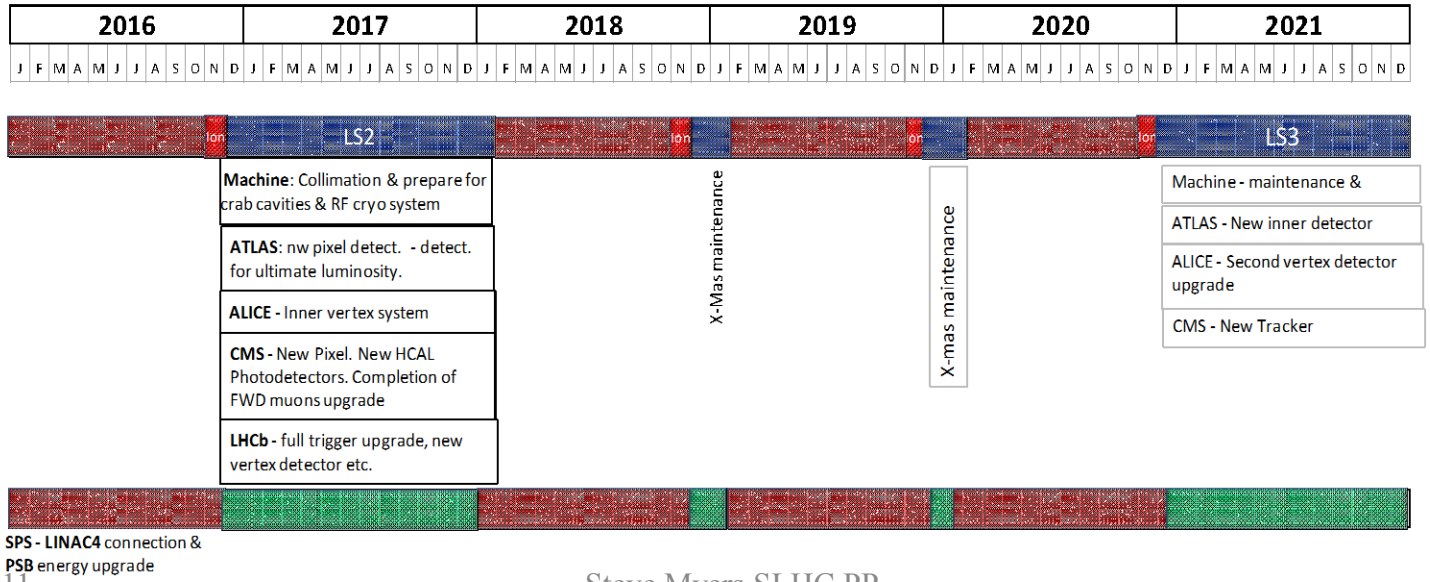
- The present Pixel detector is working very well and was designed 10 years ago and built to operate up to a maximum luminosity of ~ $1x10^{34}$ cm^{-2} s^{-1}
- Some limitations (4-5% data losses in inner region) in the Readout Chip will start becoming evident already at ~ $1x10^{34}$ cm^{-2} s^{-1}
- LHC is planning to increase luminosity in the years 2018-2020 up to 2 - 2.5 $x10^{34}$ cm^{-2} s^{-1} after 1 year shutdown in 2017.
- After $1x10^{34}$ cm^{-2} s^{-1} data losses of the present ROC would deteriorate to un unacceptable level (~ 15%) at $2x10^{34}$ cm^{-2} s^{-1} (or 50% !! if the machine will run with 50 ns bunch spacing and higher current /bunch) leading to a major degradation of Tracking performance.

  Under these conditions, the ability of CMS to continue to deliver Physics and benefiting of higher luminosity will be seriously compromised.
- The main goal of upgrading the pixel detector in 2017 is thus to maintain high level of Tracking performances until the end of Phase I e.g. up to 2 – 2.5 $x10^{34}$ cm^{-2} s^{-1}
- The necessity of replacing the Pixel detector will allow us to design and built a new system fully benefiting of the technological advances that took place in the past 10 years enabling the construction of an overall more performing system.

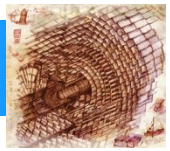
New Draft 10 year plan

CERN is revisiting the LHC plan.
A draft is available.
The official revision available in June 2011





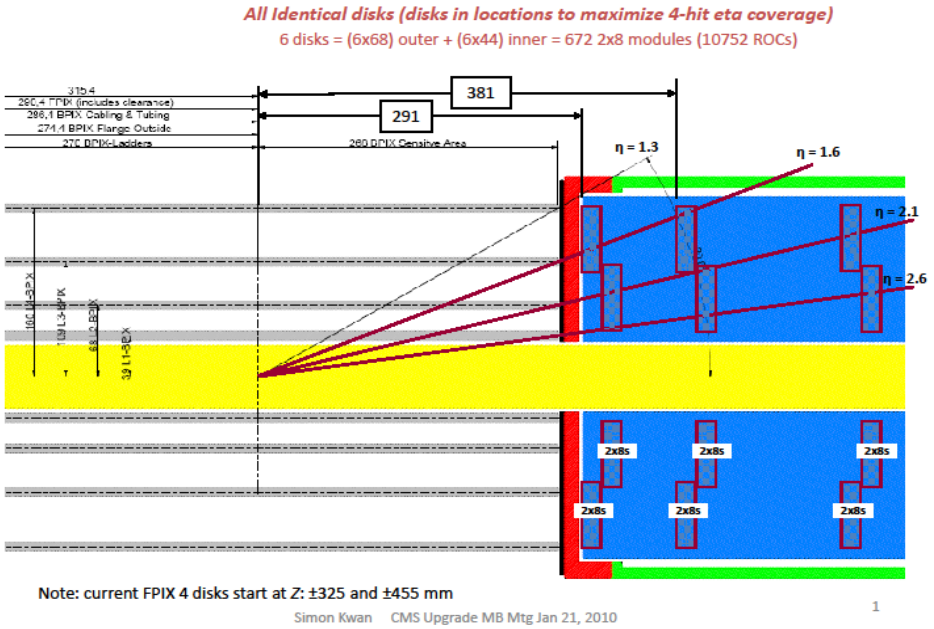
Main features under discussion

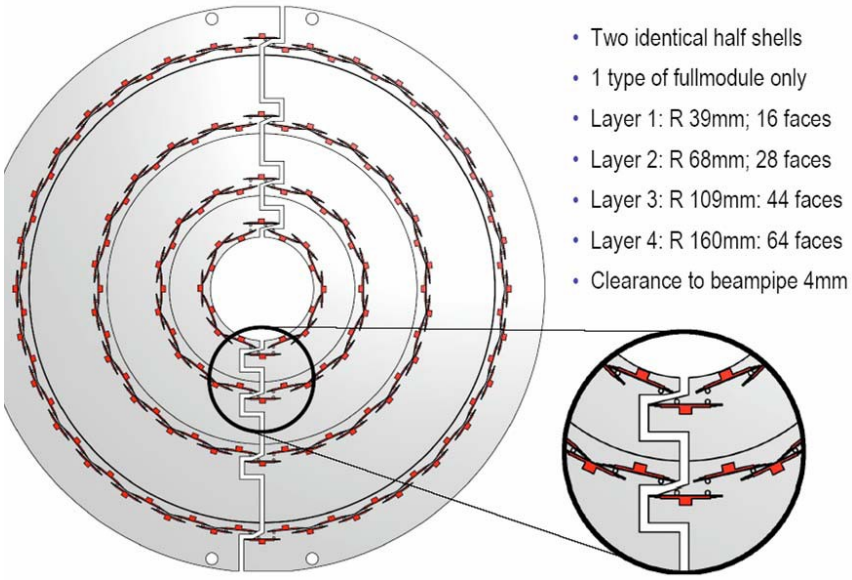


New Layout 4 layers / 3 Disks per side

- Reduce Read-Out inefficiency of present ROC – that has been designed for $\mathcal{L} \sim 1x10^{34}$ cm^{-2} s^{-1}
  - -New Readout chip to much improve Read-Out efficiency up to $2x10^{34}$ cm^{-2} s^{-1}
- Reduce aggressively (50-60%) the Material Budget
  - - Decrease the amount of multiple scattering, photon conversions and nuclear interactions.
    - Improve Impact Parameter Resolution and Tracking efficiency
- Add a 4th Layer (radius 160 mm) much closer to the TIB w.r.t. present 3rd Layer (106 mm)
  - - Improve track seeding efficiency and hermetic 4 hit coverage
    - Improved Tracking and HLT performance (pixel tracks can be found quickly)
    - Increase redundancy and robustness of pattern recognition
    - Improved Tracking performance in core of high pt jets
    - Cope better with possible problems of inner layer of outer Tracker
- Reduce Inner Layer Radius from 44 mm to ~ 39 mm (possibly 30mm) with a new beam pipe 25 mm radius (22.5 mm under consideration)
  - - Improve b-jet tagging (aim 20% improvement)
  - - Reduce dependence on charge sharing and maintain resolution with radiation
  - - Improve seed efficiency and quality in very dense environment
    - Improved Tracking performance in core of High Pt jets, increased robustness

Pixel Upgrade Layout





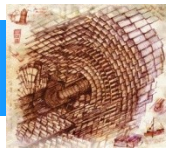
Total

Number of Pixel modules: 1.888

Number of Pixel: 124 M

Sensor Area: 2 m^2 of Pixel detector

Broad brush description Pixel Upgrade - Systems



- **New PSI46dig ROC:**
  - Reduce data losses at high luminosity
  - Robust digital readout link for higher data rate transmission
  - Protection mechanism against large clusters induced by beam background **(observed in present Pixel)**

- **New Cooling System: CO_2 Cooling**
  - Higher refrigeration capability, smaller pipes, lower mass fluid, reduce contribution to MB etc.

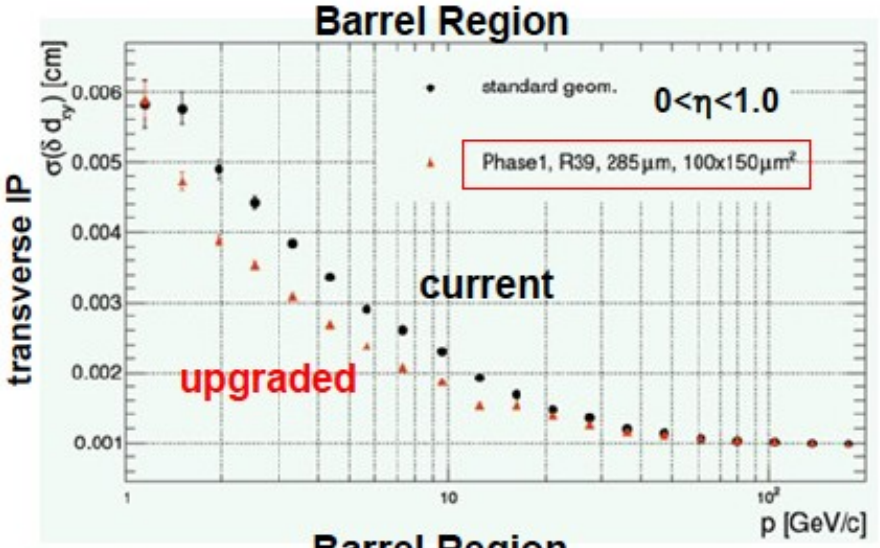
- **New Power System: DC-DC conversion Power System**
  - Lower currents, lighter internal cables, reduce contribution MB

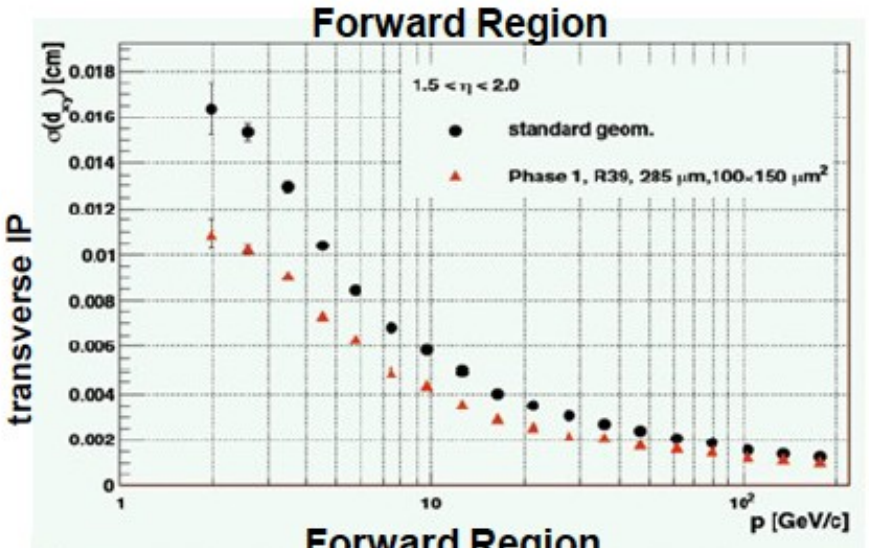
- **New Optical Readout link System: 320 MHz digital optical link**
  - Replace obsolete analog link with more robust digital link, with new lasers, new opto-hybrids and new opto-receivers

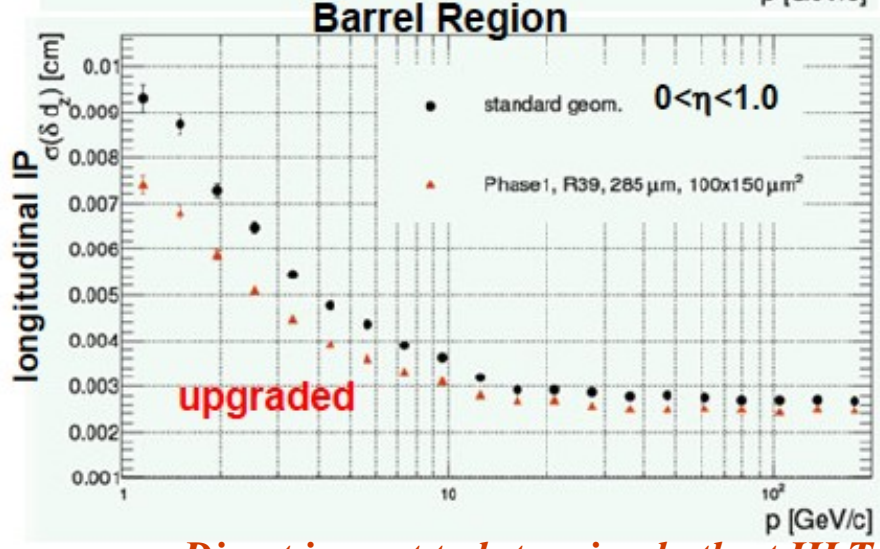
- **Modified DAQ and Control Systems**
  - Preserve present TTC, PxFEC
  - Modify PxFED to adapt to digital 320 MHz Readout
  - Fall forward Inner Layers option compatible with these read-out and controls systems

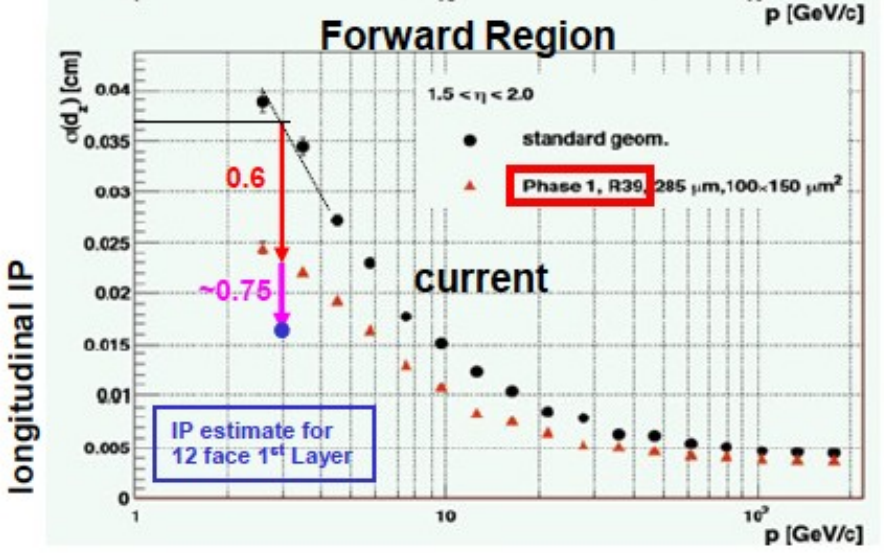
Impact parameter resolution

25-40% improvement in impact parameter resolution in both directions





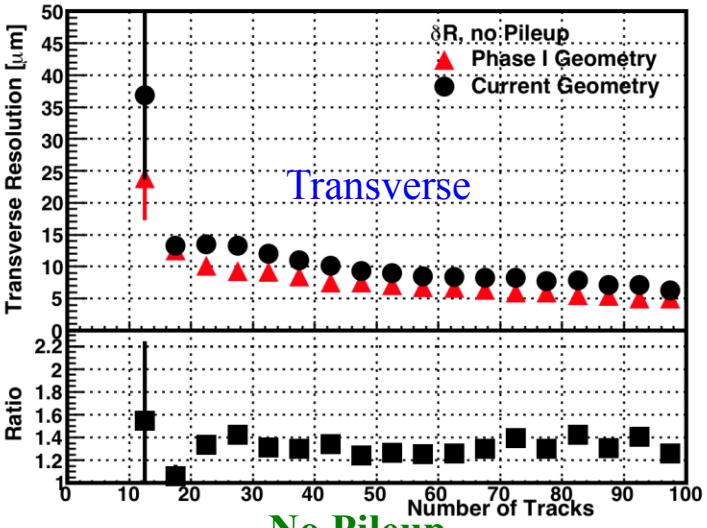




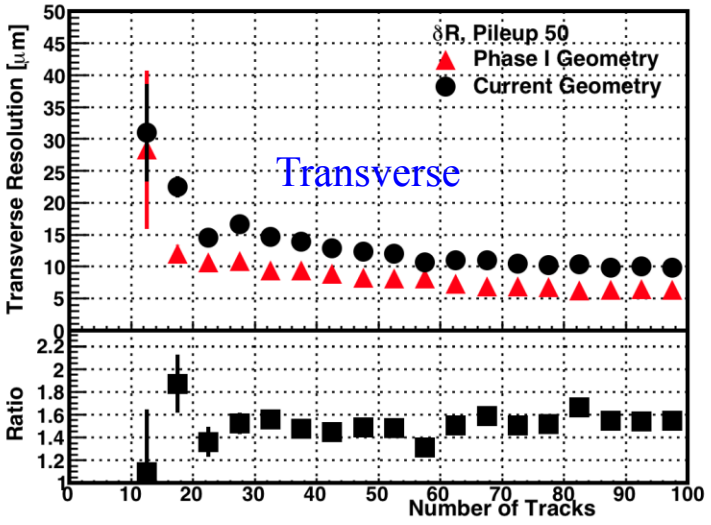
Direct impact to b-tagging both at HLT and offline!

Primary Vertex Resolution

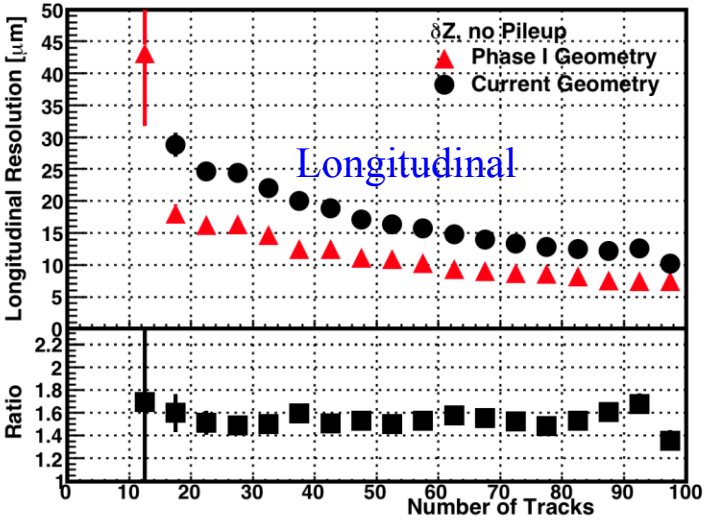
Ratio Resolution (μm)

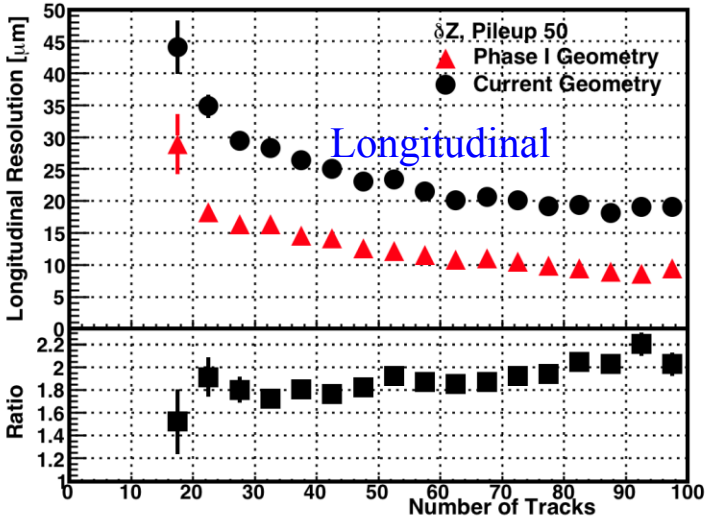


No Pileup

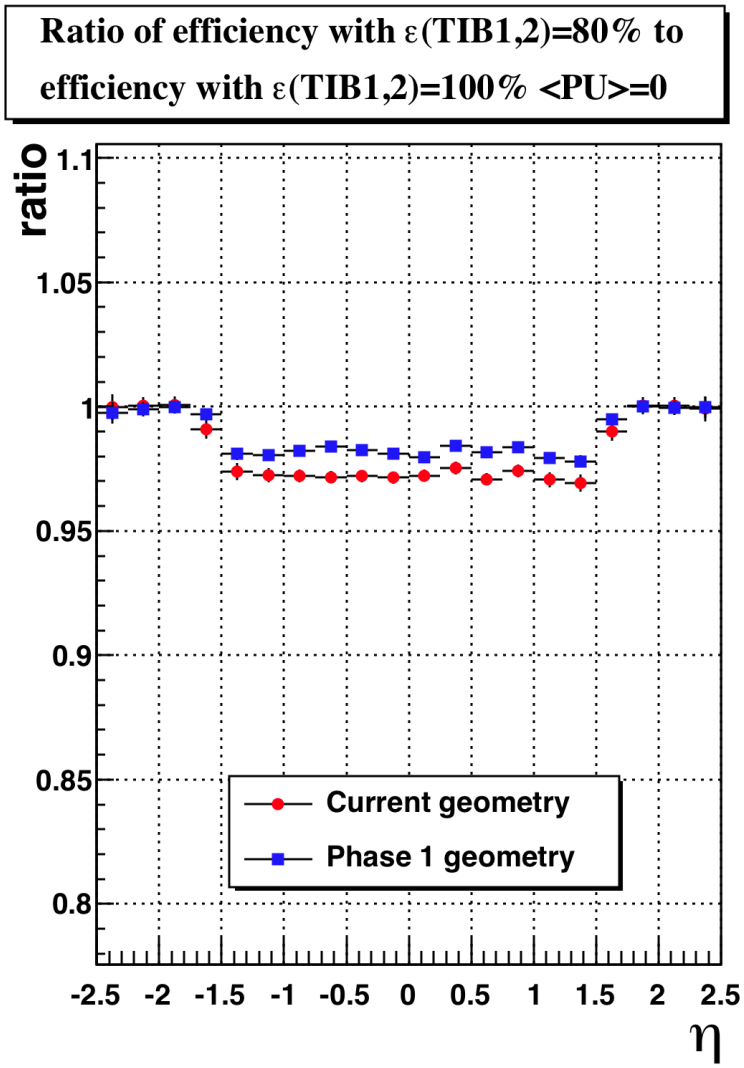


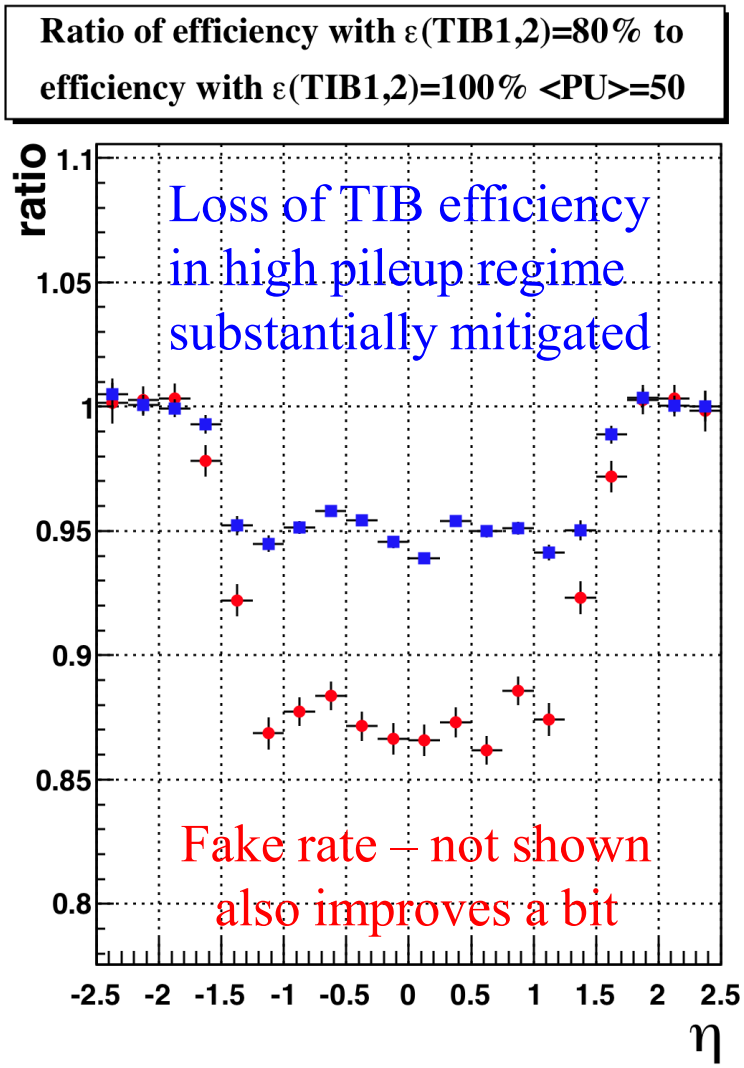
Pileup = 50





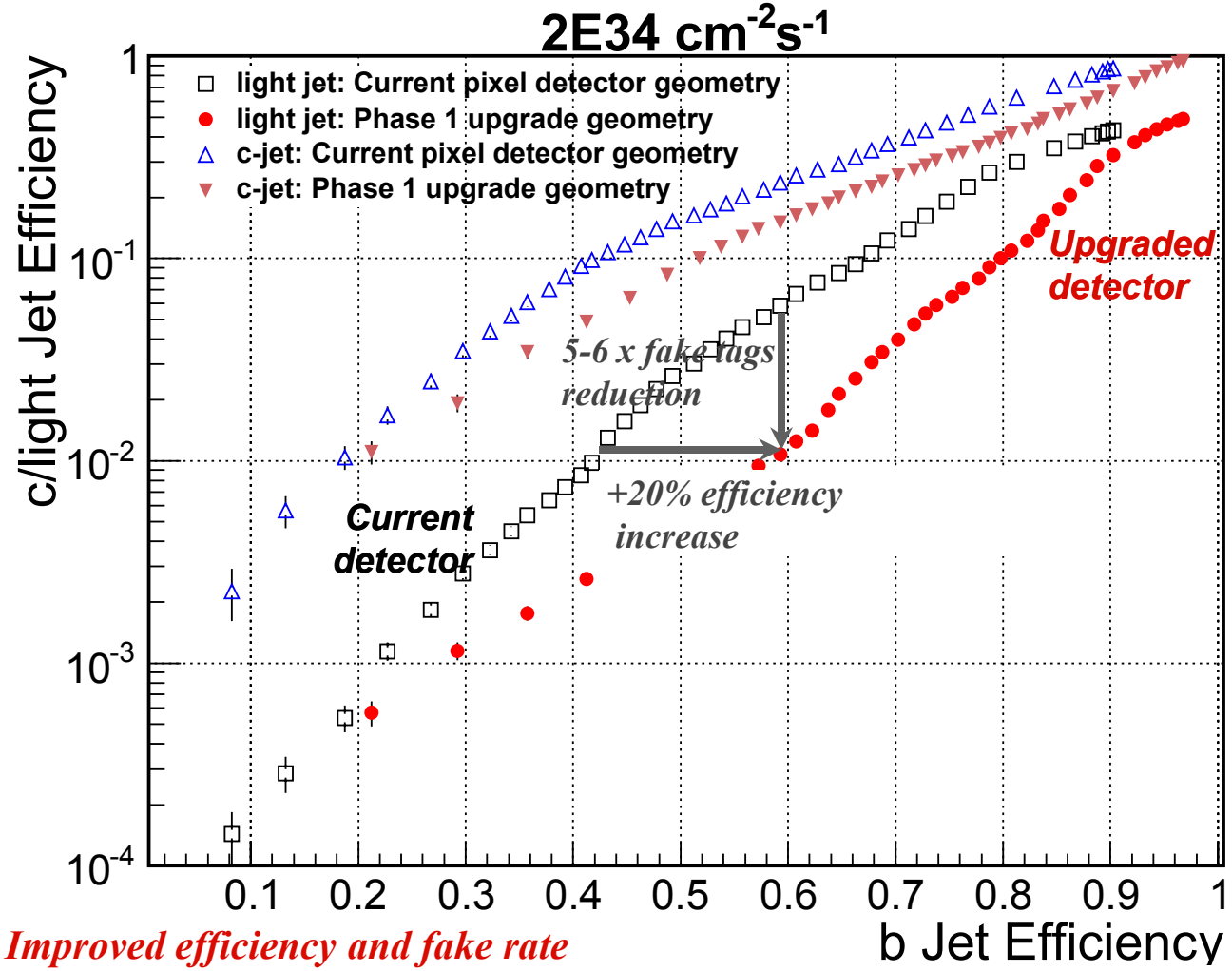
Pixels mitigate TIB losses





If Tracker Inner Barrel layers degrade prematurely, pixel upgrade recover losses

B-tagging performance

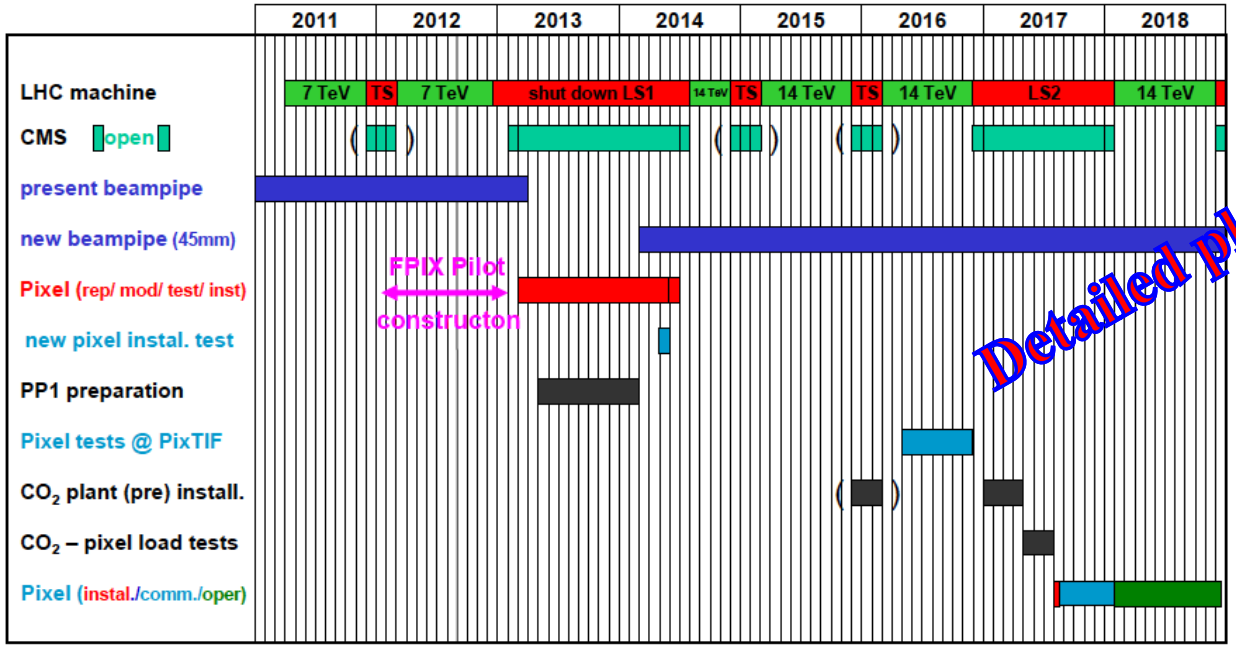


Improved efficiency and fake rate contributing exponentially with the number of b-tagged jets (e.g. Top, Susy, etc.)

QCD 80<p_t<120 GeV
Combined Secondary Vertex tagger

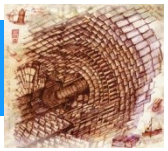
Draft timeline of INFN activities

Develop and produce assembly tools	start 2011
Develop assembly and testing procedures	start 2011-12
Participate to qualification of ROC chip and TBM	2012
Bump bonding tests and qualification of Selex	2012
Assembly and test procedures established	2012
Full qualification of pre-production modules	2012-13
Module assembly and calibration (~ 12 months construction)	2013-14
Participate to integration at CERN	2015
Participate to commissioning, full system test at CERN	2016
Ready for installation in CMS	mid 2017



Detailed plan under discussion

Fall forward option Pixel Upgrade: Inner Layers



- LHC is planning to deliver ~ 300 fb^{-1} by the end of Phase 1.
- The inner layer will have to be replaced once due to radiation damage.
- This replacement presents a further opportunity to improve detector performance and test newer technologies for later stage (in view of HL LHC era).

- Evaluating Performance, Physics gains in increasing the hit resolution in the inner layer – ring (reducing the pixel pitch and sensors thickness)

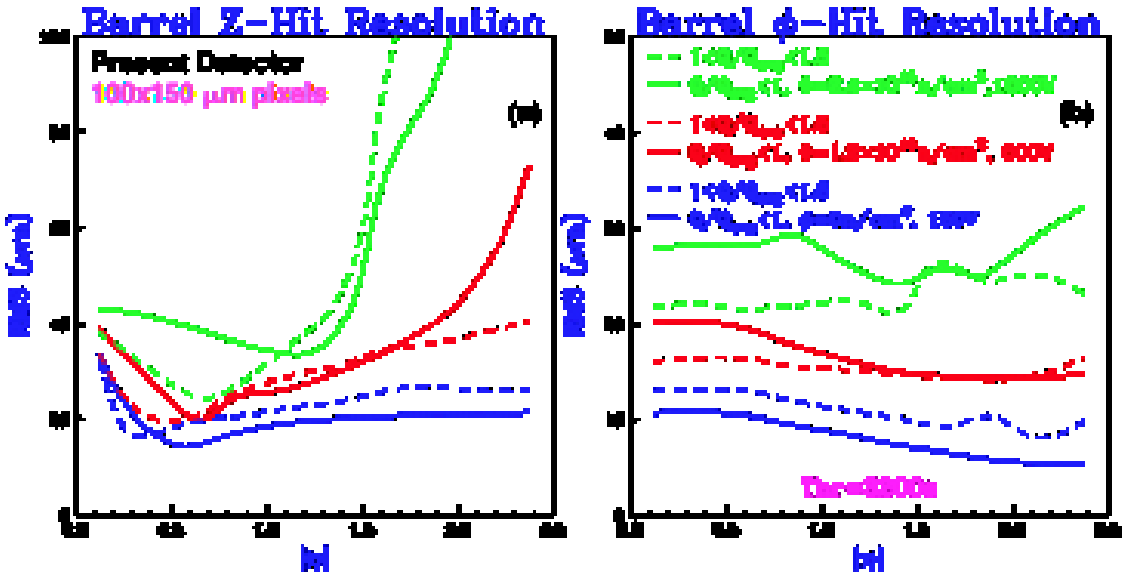
  • **Sensors design: n-on-n with reduced thickness and 50% pixel area.**

  -Fall forward option: Develop thinner n-on-n sensors (~ 220 μm thick), ~ 50% smaller pixel area (~ 75x100 μm^2) and evaluate possible alternatives (diamond).
  Improving single hit resolution (gain in term of radiation tolerance and reduction of material)

  • **Evolve Readout Chip**: **ROC chip design optimized for lower thresholds and 50% pixel area.**

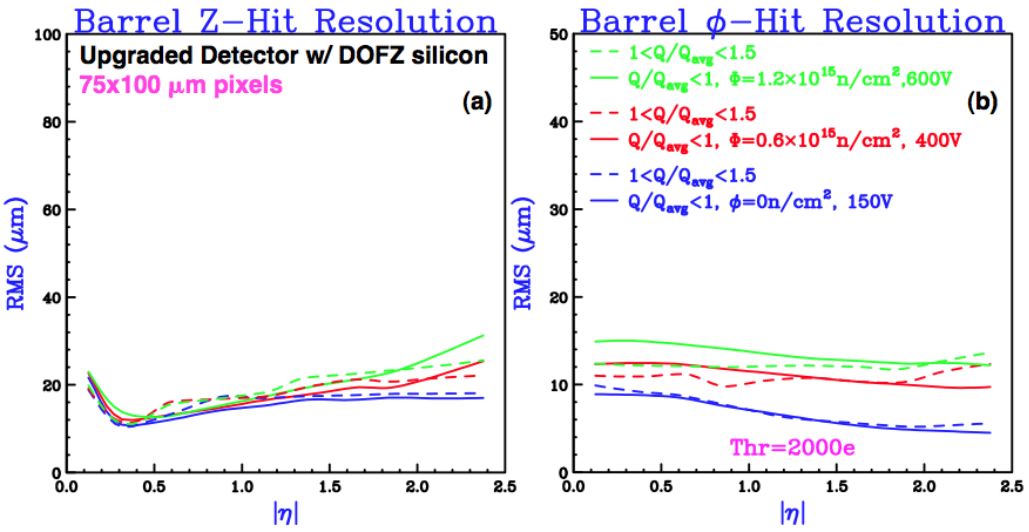
  - Fall forward option: evolve ROC chip, compatible with DAQ and controls.
    - Optimized design for lower operational thresholds to 'extend' lifetime of the inner layers.
    - Reduce readout cell size (~ 75x100 μm^2) to match reduced pixel area.
      This can be reached thanks to 130 nm (or lower) technologies and to a careful optimization of the chip layout design.
    - Possibly able to digest higher rate with reduced dead time

First layer lifetime



- Current sensor technology will have sizable resolution deterioration at end of Phase 1 lifetime
  - Radiation fluence expected to exceed 10^{15} n_{eq}/ cm^2 in Layer 1
  - Roughly twice as worse resolution and >3% hit inefficiency due to charge trapping
- Requires replacement of innermost layer once during Phase 1 (after having integrated ~ 200 fb^{-1})

Layer 1 replacement

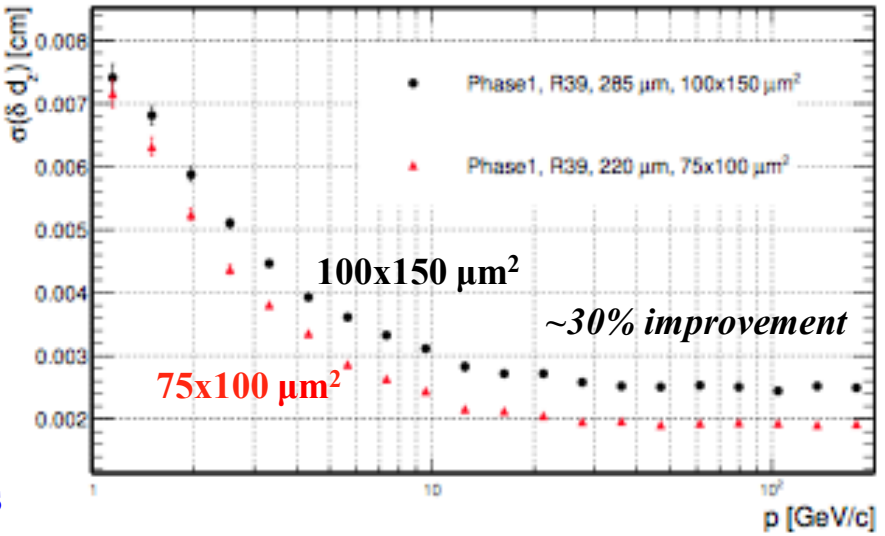


Replacement of layer 1 opens door for attractive opportunities

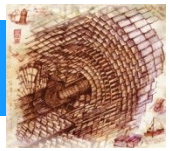
- New chip based on 130nm or smaller CMOS technology
- Can implement smaller pixel cells
- Aim at lower readout threshold

- Smaller pixels with lower readout thresholds can better preserve **position resolution** after irradiation.
- Improve **impact parameter** resolution.
- Add resolving power for **high pt jets** and boosted objects (b, tau, top).
- Better **vertex resolution** in a high pile-up environment and improved **lifetime measurements**

Longitudinal IP resolution



Fall Forward Option development



Design of new readout chip in 130 nm CMOS technology with objectives:

1)Readout architecture able to sustain very high data flow:

concept: keep data inside the matrix until a request arrives.
"**Regional**" approach (**size 2x2, 2x4..**), pixels share memory buffers, logic block and possibly an ADC. Experience exists (ViPix, SuperB..).

2) **Pixel size reduction**:

improvement in impact parameter resolution, occupancy reduction and sensitivity to radiation damage (sensor leakage current).
Pixel size of **100x75 μm^2 or even smaller** appears feasible.
Experience exists for smaller pixels (ViPix, SuperB..).

3) **Increase of clock frequency and output data bit rate**:

In 130 nm experience exists (ViPix) with logic blocks operated @~1GHz.
Good safety margin for a digital design at frequencies of **few hundreds MHz**.
Dead time reduction and readout efficiency optimization.
Logic blocks inside the pixel matrix can operate at lower frequencies.

Possible Work plan

As a first step, these three concepts could be tested in a small-scale device (just as an example, 32x32 pixels), with a size large enough to give meaningful results especially for the readout architecture solutions.

• In the preliminary stages of the project, single blocks (e.g. ADC or other critical analog circuits) could be submitted in a test chip.

• After the basic concepts are proven, a couple of iterations with a full scale device should lead to the final version of the readout chip, ready for production.

• As usual, an accurate contingency evaluation has to be carried out in terms of both schedule and funding.

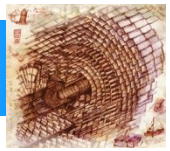
New Pixchip

- Project structured in 3 stages (~12-16 months each) total time 4-5 years.
  - Design, submission of Test structures (FE, ADC, pixel-level logic), 1 or more chips (estimate cost 250 KCHF)
  - Design, submission and test of a small scale version of readout chip (~ 150 KCHF)
  - Design, submission and test of a full scale version of the readout chip (~250 KCHF)
  - Production run (~ 400 CHF)
- Interest and experience in INFN and some other Institutes (FNAL).

  INFN : To, Pi, Pg, PD, Fi

  - Solid experience in Torino with 250 nm, 130 nm and even 90 nm technologies (chips FE Alice Si-drift, FE Panda Pixel, Dacel CMS GBIT laser driver).
  - Proven experience in Perugia and Pisa Electronics Departments 180, 130, 90 nm chip design (GR5 activities ->MAPS chips, VPix chip design, TO_asic, FF-LYNX)
  - Solid experience in PD for Rad-Hard qualification and SEU measurements of front-end chips (APV25)
- Resources (from INFN):
  - 2.5 FTE design
  - 2.5 FTE test & characterization
- Funding: possible sharing 50-50 INFN - USA (~ 500KCHF each)

Rad hard sensors



Replacement of layer 1 at later stage of Phase 1 provides an opportunity to adopt sensors with greater radiation hardness (diamond could be an option).

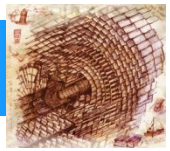
Milano group interested to assess possibility of using diamond sensors.

Solid interest and experience and several (past and ongoing R&D) GR5 activities.

- Milano: Diapix
- Catania: RD42
- Firenze/Perugia: Rapsodia/Chipsodia

- Funding for a batch thin n+on n /diamond sensors with fine pitch 75x100 μm^2 possible sharing 50-50 INFN - USA (~ 100 KCHF each)

Executive Summary



Technical Proposal for Phase I completed. Discussing timeline for TDR (~ end of 2011)

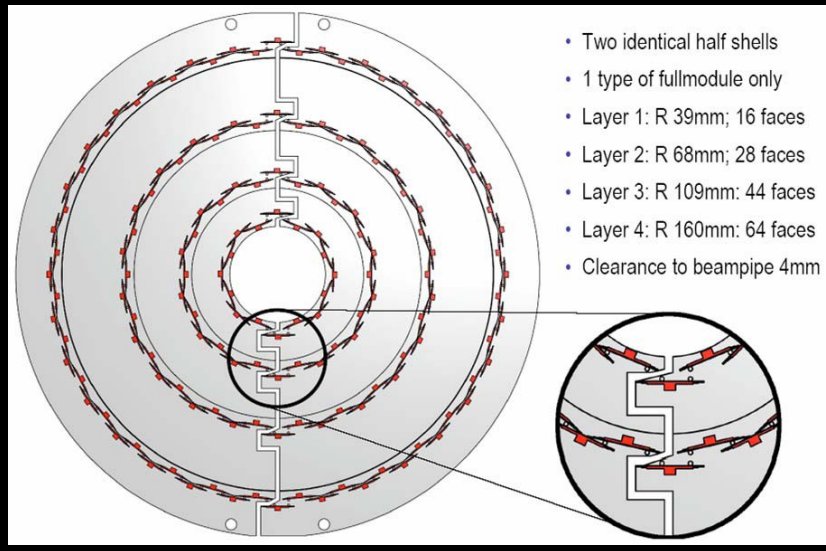
- Present detector was designed to operate up to ~$1x10^{34}cm^{-2}$ s^{-1}
  Strong evidence that current detector needs to be replaced for running at luminosities above $1x10^{34}cm^{-2}$ s^{-1}
- The main goal of upgrading the pixel detector in 2016-17 is to maintain high level of Tracking performances until the end of Phase I e.g. up to $2x10^{34}$ cm^{-2} s^{-1}
- Radiation effects will grow as luminosity increase requiring once the replacement of inner layer before the end of phase I

Proposing to contribute to:

1. Development, construction, integration and commissioning of part of Bpix to be installed in 2016-17.
2. Development of a new Read-out chip with more advance technology employing a smaller Pixel size.
   - This second development has to be seen as important intermediate step toward identification of new Pixel readout architectures and sensor technology for the Higher Luminosity LHC.
   - It will strategically strengthen our INFN community and CMS community in a critical area as that of readout chip design.

CMS: pixels ½ L3

- Costruzione ½ layer 3:
  - Partecipazione "importante" in termini di visibilita' della componente italiana
  - Interessante apertura del gruppo del tracker ad una nuova tecnologia
  - Riutilizzo di molte infrastrutture di sezione predisposte per il tracker
    - Transizione verso futuri upgrades piu' importanti
  - Proposta dimensionata in modo appropriato sia in termini di costi che di necessita' di risorse nelle varie sedi



CMS: pixels ½ L3

- Richieste:
  - Materials, sensors and bonding 850 kCHF ➔ 650 k€
  - Setup: 150 kCHF ➔ 120 k€
  - Totali: 1000 kCHF ➔ 770 k€
- Proposta referees:
  - Si autorizza CMS ad impegnarsi fino 750 k€
  - Si prevedono inoltre 150 k€ di contingenza che la CSN1 puo' assegnare, anche parzialmente, a fronte di motivate richieste
  - Massima assegnazione multiennale per questo progetto:
    - 900 k€
  - Assegnazione 2011:
    - 50 k€ per iniziare setup laboratori (a scalare dai 900)

CMS: pixels e alta luminosita'

- Il nuovo pixel detector necessitera' di sostituire il layer piu' interno nel corso del suo periodo di funzionamento
- Sviluppo di componenti dei futuri layer interni, pur rimanendo all'interno degli sviluppi per fase 1, pone le basi tecnologiche per gli upgrades di fase 2

- Interessi italiani:
  - Partecipazione con FNAL allo sviluppo di un nuovo chip per i pixels con tecnologia 0.13 μm
  - Partecipazione allo sviluppo di rivelatori a diamante

CMS: pixel – chip

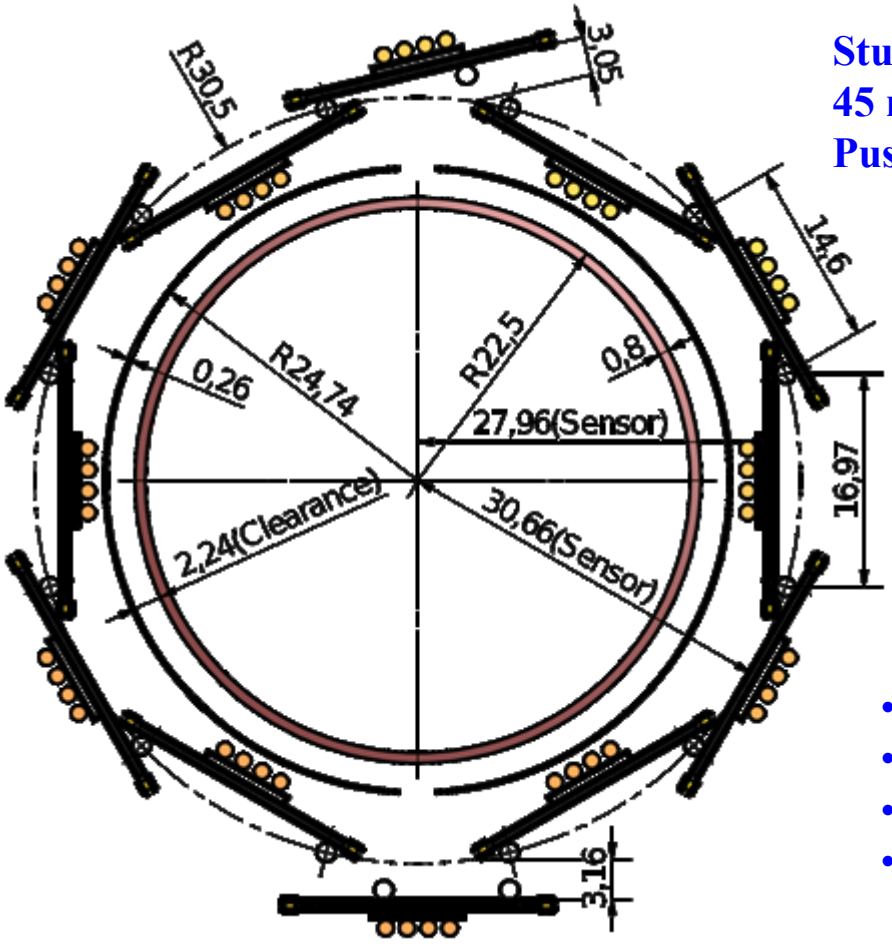
- Richieste:
  - 600 kCHF ➔ 460 k€
    - Di cui 200 kCHF (160 k€) per il run di produzione
- Proposta referees:
  - S'incoraggia l'attivita' che pero' non ha ancora trovato una sua chiara definizione. I partecipanti sono invitati a creare un piano che coinvolga un'importante contributo italiano alla progettazione del nuovo chip.
  - L'approvazione del finanziamento si articola in due stadi:
    - fino a 50 kE per le prime produzioni e test di parti del circuito, dopo verifica della definizione del programma di lavoro e di collaborazione
    - fino a 150 kE per successive produzioni di prototipi e test, dopo verifica dello stato del progetto dopo il completamento del punto precedente.
    - NON si finanzia il costo di produzione. Eventuali contributi vanno presi dalla contingenza residua sulla costruzione del Layer 3.

CMS: pixels - diamanti

- Richieste:
  - 38 k€ produzione prototipi sensori
  - 40 k€ bump-bonding degli stessi
  - 15 k€/yr consumi
- Proposta referees:
  - I referees supportano questo interessante sviluppo che deve pero' essere meglio integrato in CMS ed RD42
  - Si allocano fino a 40 k€ per la produzione dei sensori
  - Invito a negoziare il bump-bonding con la ditta che fara' quello del L3 dei pixels → costo finale da contingenza pixels
  - Consumi da finanziamento ordinario CMS

Back up slides

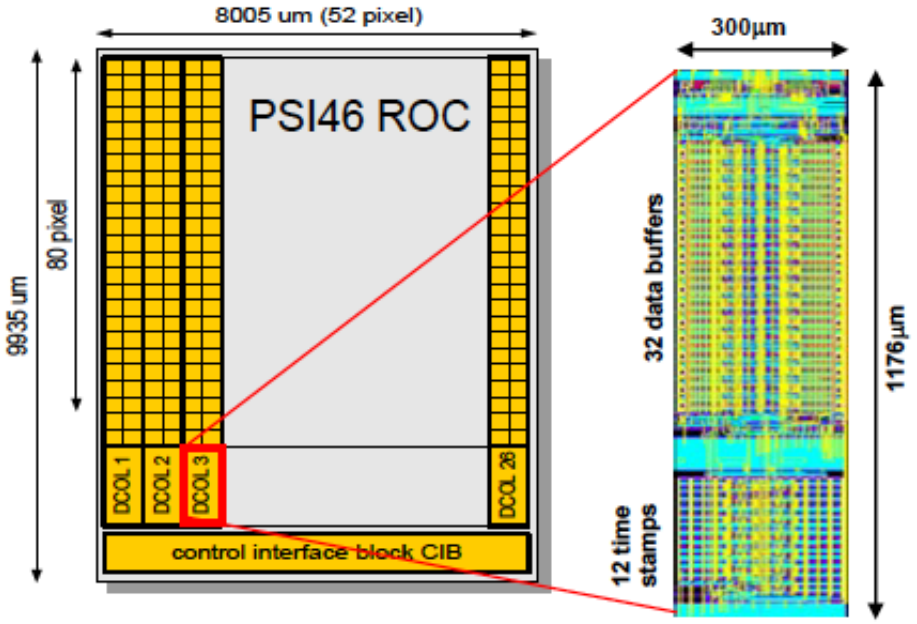
Beam pipe radius



Studies are ongoing to asses safe beam pipe radius.
45 mm diameter seems doable.
Pushing for Beam Pipe installation in LS1 2013

- **mean 1st layer Si- radius = 29.8 mm from 44**
- **need 2 mm clearance to beam pipe**
- **need adjustable closing mechanism**
- **Beam pipe diameter 45 mm from 58**

Upgraded PSI ROC Chip



Present ROC for 1st Layer:

Luminosity	bx-spacing	Data Loss
$1x10^{34}cm^{-2}s^{-1}$	25nsec	4%
	50nsec	16%
$2x10^{34}cm^{-2}s^{-1}$	25nsec	15%
	50nsec	~50%

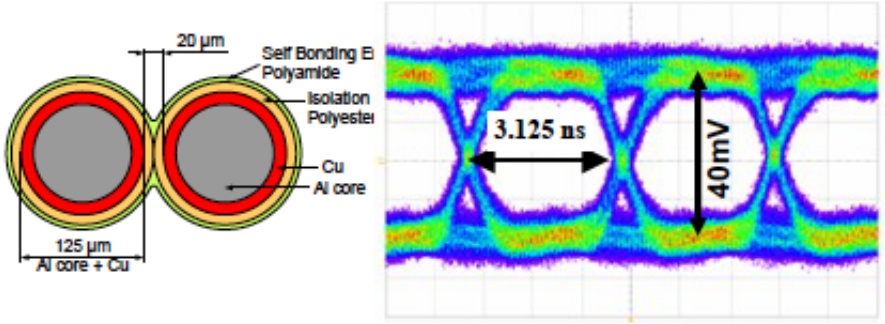
50nsec operation of LHC was not planned in original ROC architecture in 1998.

Data losses removed by ROC changes:

	Status
1) increase depth of	
- data buffer 32 → 80	done
- timestamps 12 → 24	done
2) add readout buffer	done
3) 160Mbit/sec serial binary data out	now
4) deal with PKAM events → DAQ resync	

µ-twisted CCA pair (Copper-Cladded Aluminum)

- 1m long low mass link at 320MHz , chips done !

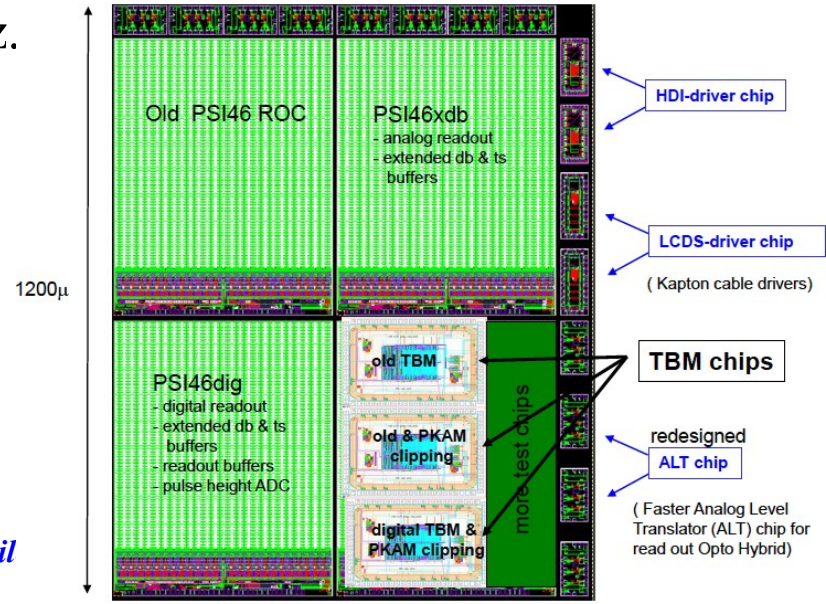


Upgraded PSI ROC Chip

- The current ROC was designed for 1E34cm^{-2} s^{-1}
- There is a ~4% dynamic data loss in the innermost BPIX layer at this lumi (readout-related losses 3%, column-drain time 0.8%)
- This increases gradually to ~16% for 2E34 cm^{-2} s^{-1}
- For 50 ns bunch spacing at 2E34 cm^{-2} s^{-1}, the data loss would be ~50%

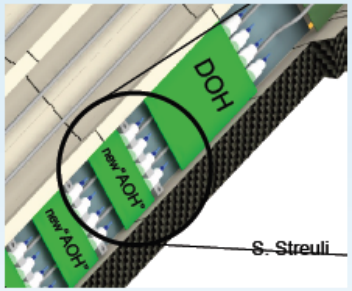
- Current ROC needs to be replaced for running above 1E34 cm^{-2} s^{-1}
- Double buffer space to reduce readout-related dead time
- All digital readout clocked out at 160 MHz from ROC to new digital Token Bit Manager (TBM). Multiplex multiple rings with TBM at 320 MHz. Allows reduction in number of cables and therefore mass and power.

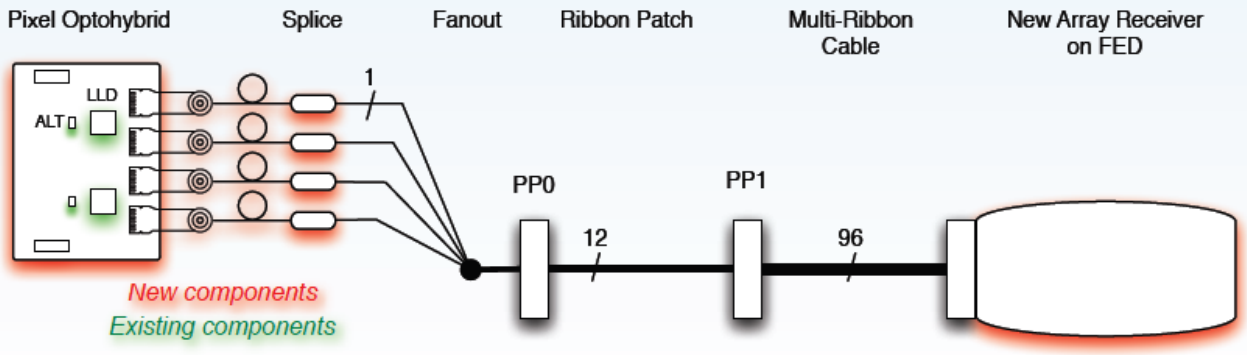
Submission foreseen for Sep. 2011

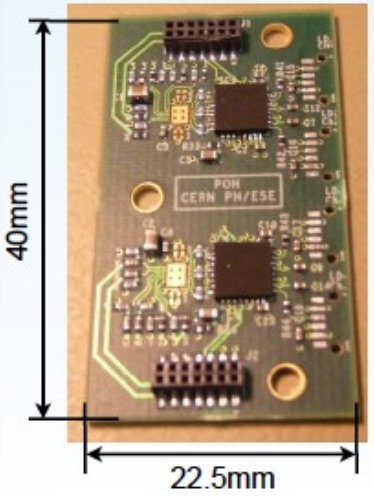


New Optical Link

- New pixel system aims at reducing material within the CMS detector acceptance
  - New supply tube
  - Electronics re-design with digital readout at 320 Mb/s
- Basic concept for the link is to keep the installed fibre system and replace the front-end and back-end components with ones compatible with 320 Mb/s digital operation

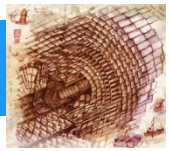






Activity advancing well at CERN. First Pixel Opto Hybrid (POH) prototypes with new laser available for evaluation

CO_2 Cooling System



Current cooling system for Tracker uses C6F14, which has density of 1.7 x water

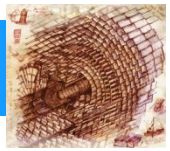
- Biphase CO2 successfully used in HEP, e.g. LHCb "Velo"
- Small channel (~2mm ID) biphase CO2 system would have good thermodynamic properties (low dT/dP, low mass, low viscosity, high latent heat, high heat transfer coefficient). Also rad hard

- Factor of ~2 lower density in liquid phase compared to C6F14

- High heat transfer means smaller area of thermal contact. High latent heat means more heat load per channel. Smaller pipes, less manifolding and less material.

R&D ongoing since ~ 2 years and well advanced at CERN/USA

DC - DC Power Supply System



- Assume that we will reuse same cable plant (very difficult to change)
- New pixel detector has factor of ~2 more readout chips.
- Will need more power To limit resistive losses, propose to bring in high V along long cables (50m) and use DC-DC switched mode converter ("buck") near the detector
- Needs to be rad hard and magnetically tolerant
- R&D ongoing in Germany/CERN since ~ 3 years. Prototypes underway