

REQUIREMENTS FOR A NEW PIXEL CHIP

Layout of the presentation

1. Present and Upgraded ROC (CMS Pixel chip)
2. Atlas Chip(s)
 1. A New chip for CMS Pixel

Requirements for the new ROC

Present ROC has been design for a max luminosity of $L = 10^{34} \text{cm}^{-2} \text{ Hz}$

- at inner radius $R=4.3\text{cm}$ correspond to a particle flux of 40 MHz cm^{-2}

□ Main features:

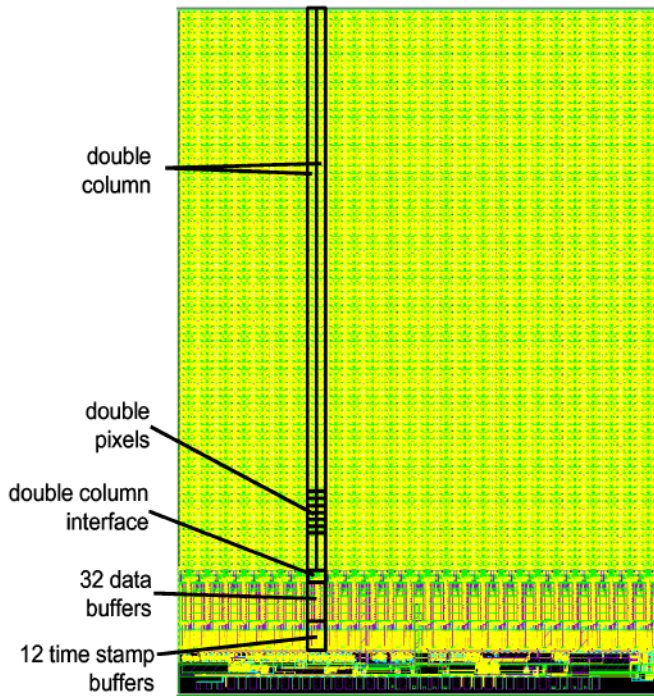
- Pixel cell $100\mu\text{m} \times 150\mu\text{m}$
- analog readout, threshold of 3500 e-
- End of Column Drain architecture
- Technology $0.25 \mu\text{m}$
- Readout serial 40 MHz

New ROC should maintain performance of present ROC at max luminosity of $L = 2 \cdot 10^{34} \text{cm}^{-2} \text{ Hz}$

- At inner radius $R=3.9\text{cm}$ correspond to a particle flux of 120 MHz cm^{-2}

□ Strategy:

- Maintain the heart of the pixel chip
 - pixel cell (PUC)
 - DoC architecture
- Lower threshold (1600e^- ?) ?? To be proved
- Digitize after DoC
- Change of periphery
- Maintain the technology
- Readout serial 160 MHz



- **ReadOut Chip (ROC) bump bonded sensor pixels.**

- **Pixel CELL (PUC): 100 μ m x 150 μ m**

- **52 \times 80 = 4160 pixels per ROC**

- **15,840 ROCs = 66 million pixels**

- **zero-suppressed output**

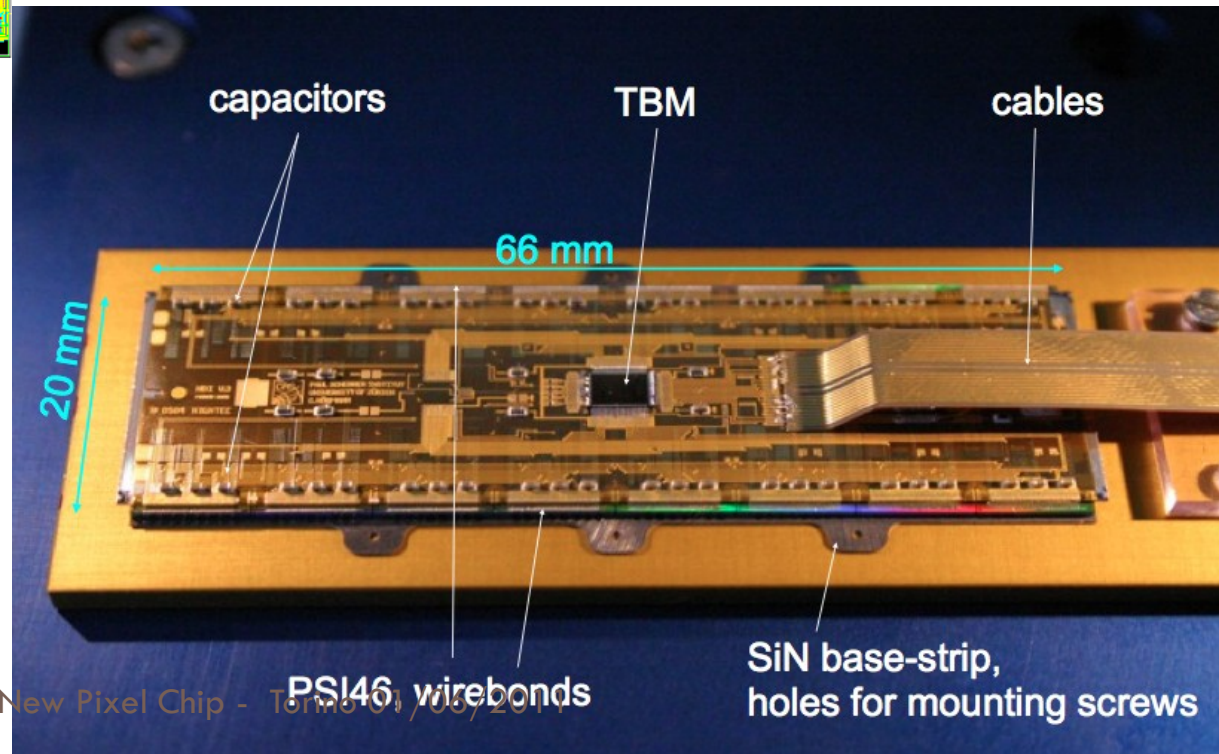
- **Each ROC can be tuned (DAC)**

- **Each pixel has a programmable threshold (adjusting this is called *trimming*)**

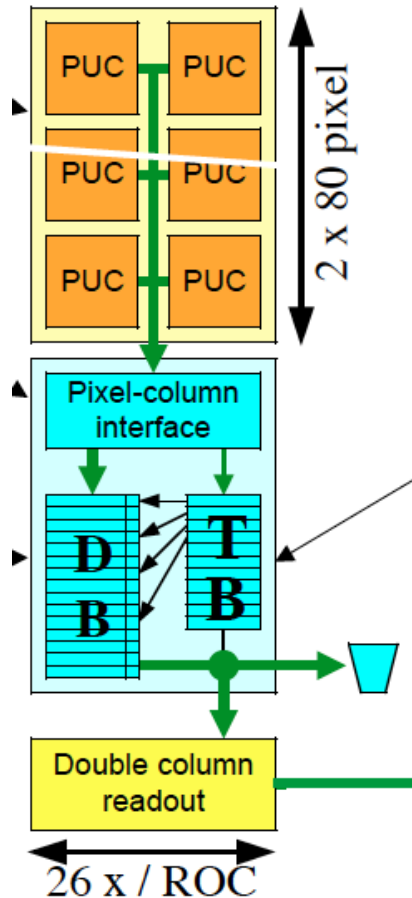
- On receiving a L1 trigger, the **Token Bit Manager (TBM)** initiates a Chinese-whisper of “token bits” that instruct each ROC to send its hit data to the TBM

- The signal from the TBM is electrical and analog. It encodes the ROC #, row and column and charge collected of each pixel hit

- The electrical signal from the TBM is converted to optical by the Analog-Optical Hybrid (AOH)



EoC drain architecture

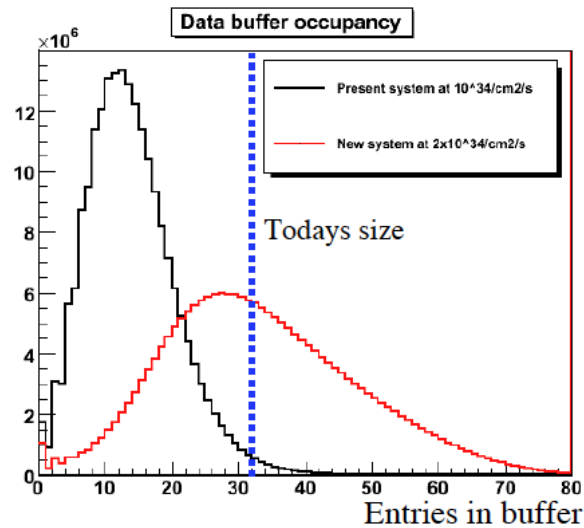
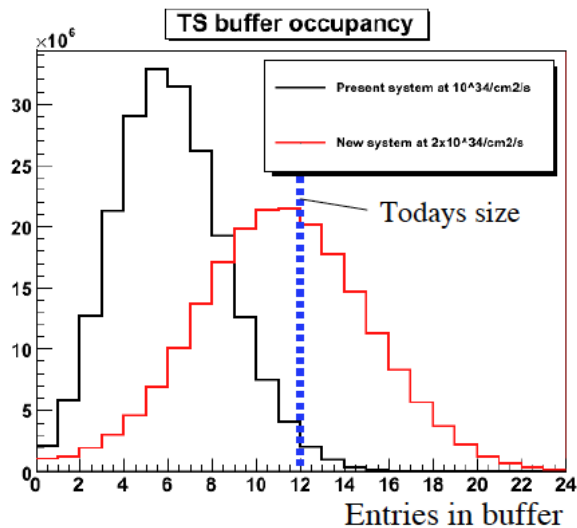


- No buffering at pixel level
 - Pixel can go in busy (waiting to be readout) but it is continuously readout
 - All data go to End of Double Column
- Huge buffer at End of Column (EoC)
 - ▣ Lot of (analog) data transfer to EoC: signal outside trigger are sent to EoC → linear with pixel fluence
 - Column can go in Busy
 - ▣ Trigger time stamp at EoC
 - Time Stamp buffer linear with: PixFluence; Trigger Latency (and also with trigger frequency)
- Readout Double Column & reset of DC data buffer
 - Dead-time depends on: $\text{PixFlu} * \text{BX-time}(25/50\text{ns})$; trigger frequency

DoC occupancy at trigger latency:
19-38 (Phase 1); 58 (Phase 2)

New ROC maintain same architecture of DoC but increase buffering

1. Increased buffering at EoC (from 12 to 80)
2. Increase Time Stamp Buffer (12 to 24)
3. Introduced ReadOut Buffer (0 to 80)
4. Increased ROC readout clock (ROC at 160 MHz, TBM to 320 MHz)



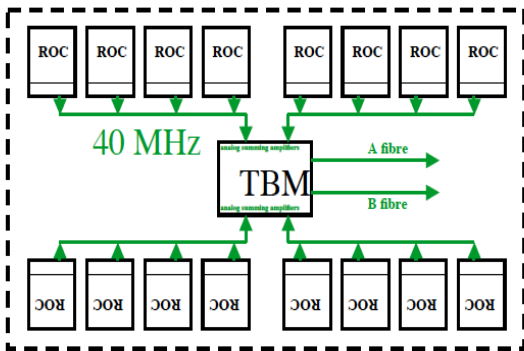
--> New buffer sizes:

Timestamp buffer: 24 (now 12)

Data buffer: 80 (now 32)

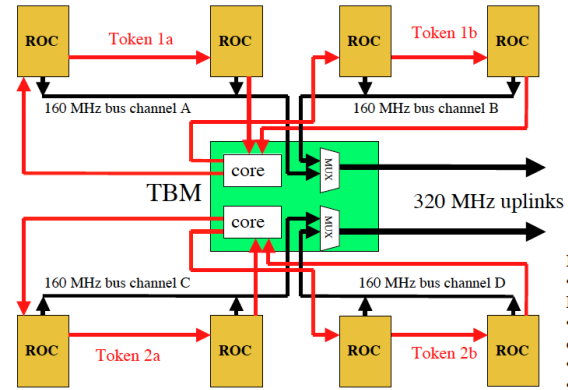
Readout of Old and New ROC

ROC → TBM (module controller) : 40 MHz analog readout
 TBM → pxFED (off detector DAQ): 40 MHz analog readout
 8 or 16 ROCs are daisy chained



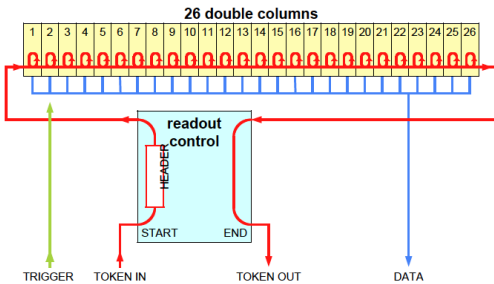
Layer 1 & 2 → 2 fibres A & B
 Layer 3 → 1 fibre A

Basic Idea of digital module layer 1

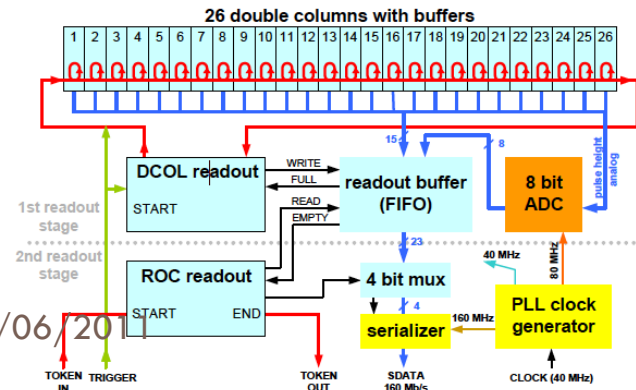


New is:
 • 4 token rings à 4 ROCs
 • TBM core takes AND of 2 tokens
 • 4 readout buses
 • 2x320 MHz uplinks

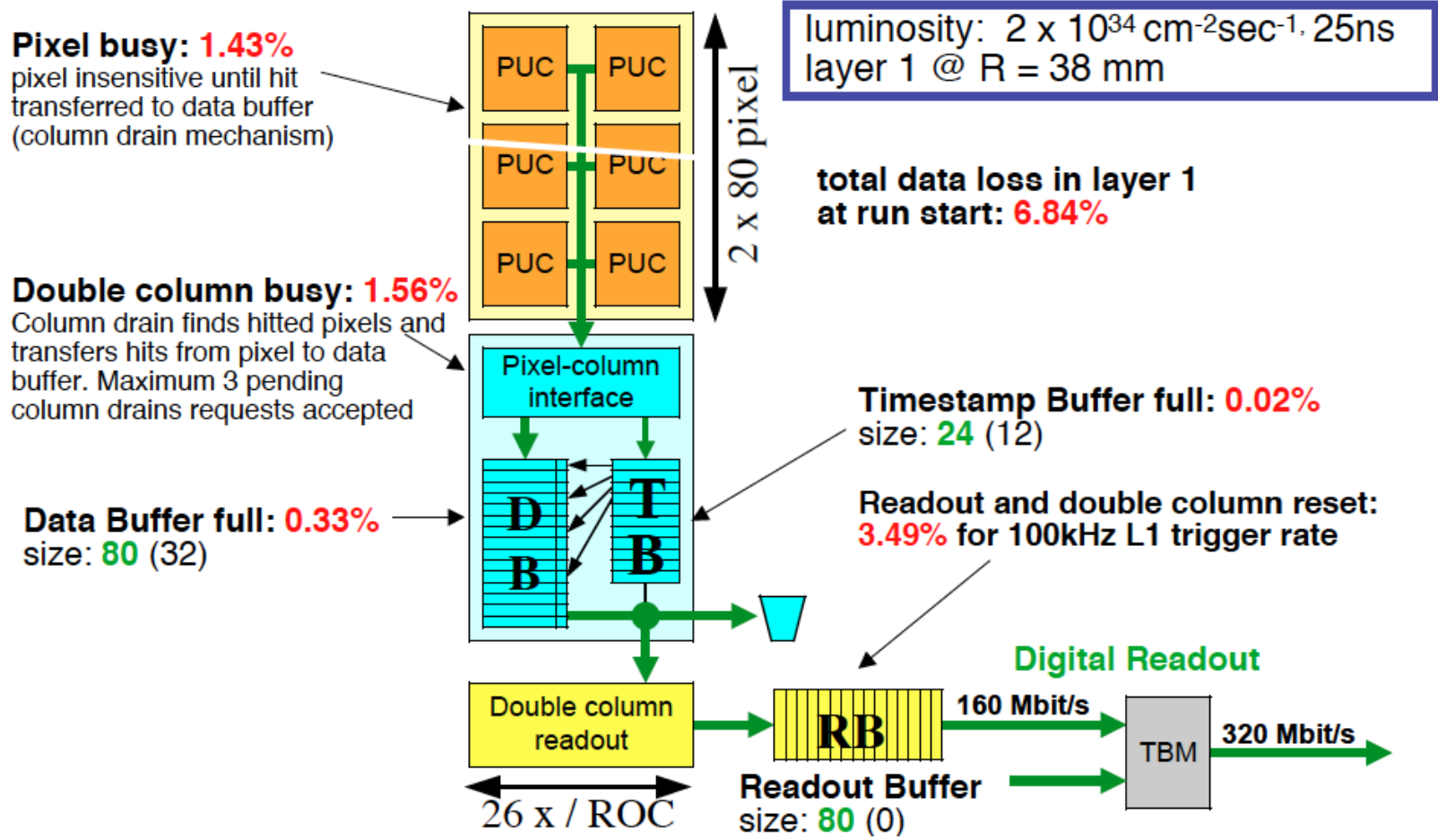
Readout Token Passing – Existing ROC



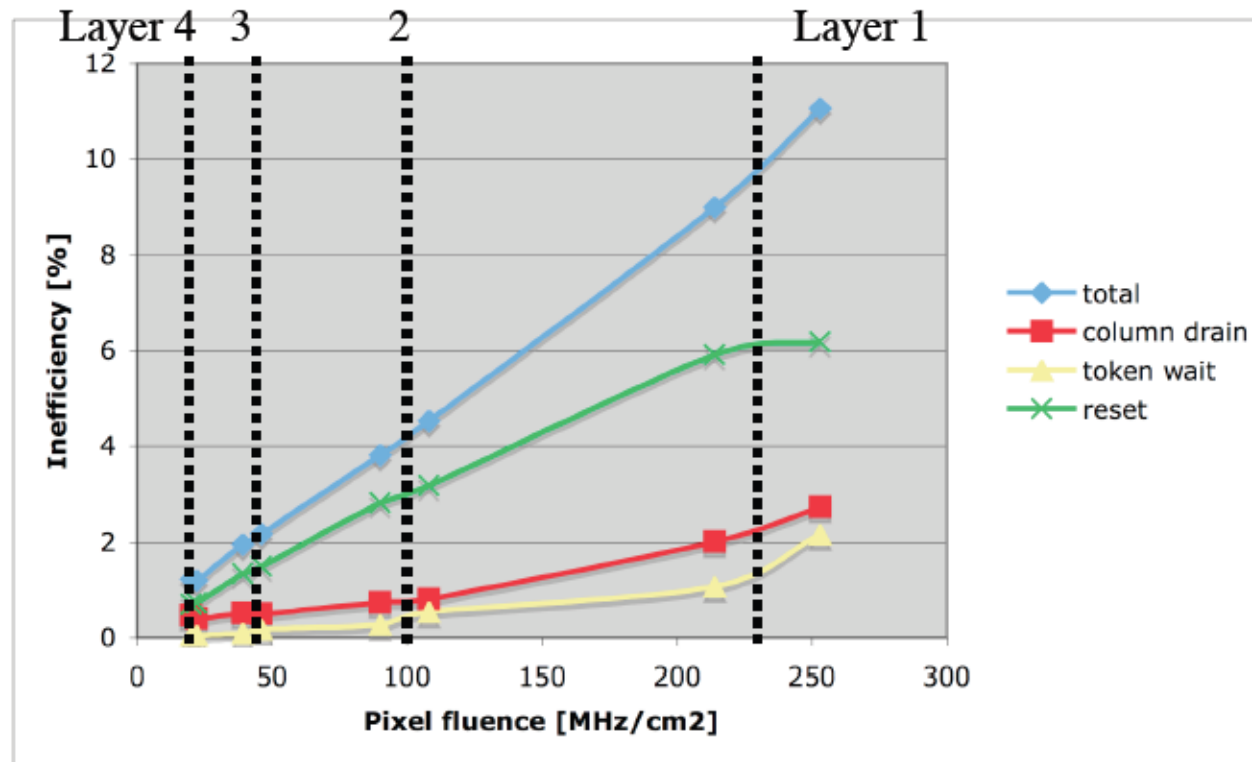
Readout Token Passing – New Digital ROC



Remaining Losses on New ROC for Layer 1, $R=3.9\text{cm}$, $L=2 \cdot 10^{34} \text{ cm}^{-2} \text{ Hz}$



Inefficiency vs fluence - status



Vertical lines indicate 2×10^{34} and 50 ns bunch structure, 100kHz trigger rate

At maximum peak luminosity, inefficiency still high

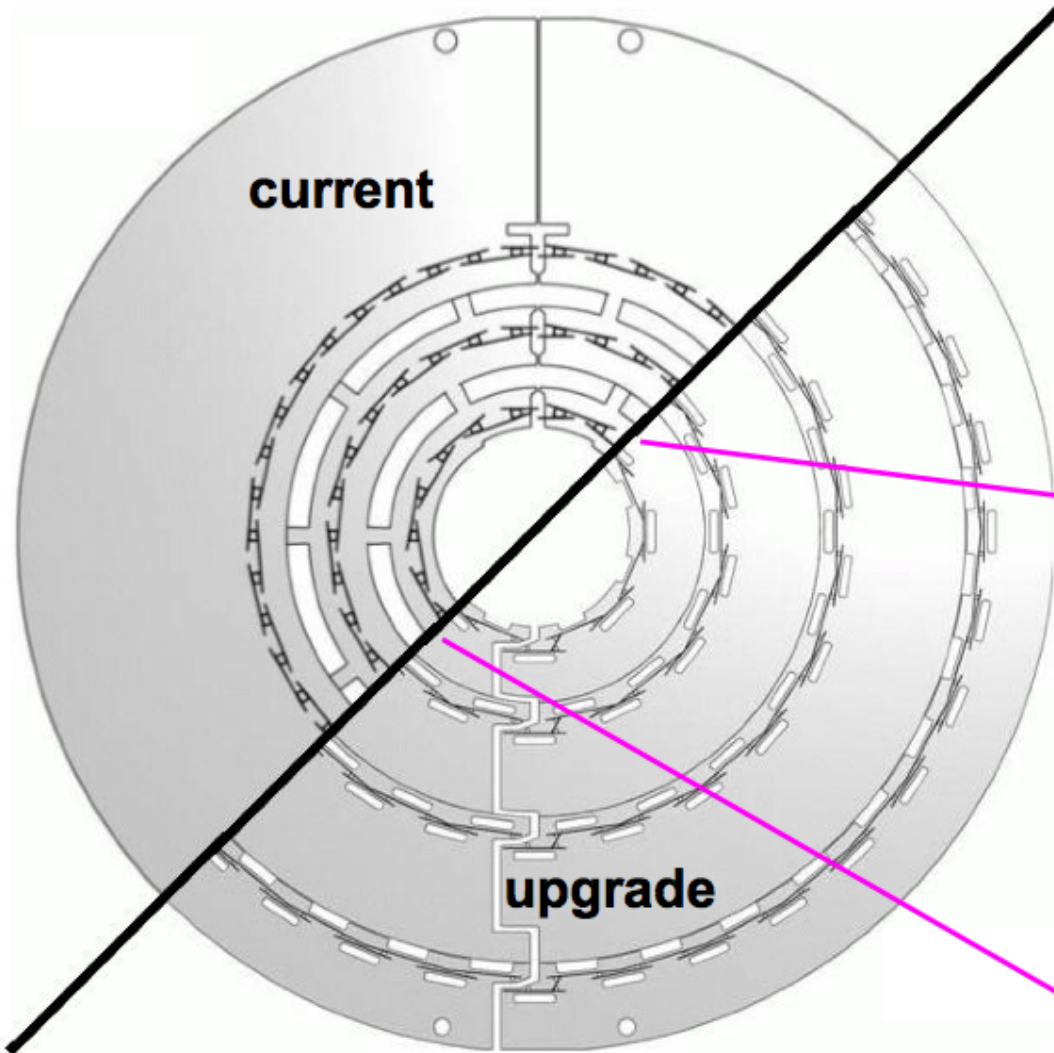
Dominated by resets after readout. There is a handle on this, but...

... It needs time to implement.

Final strategy has to be agreed on **when CMS wants what**.

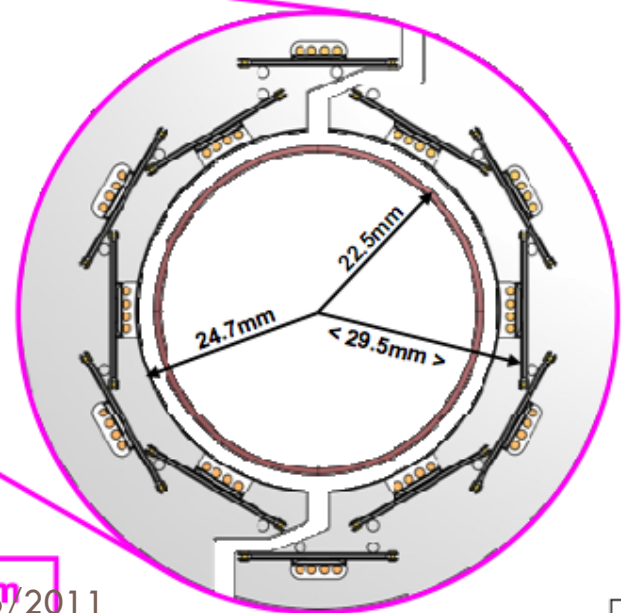
BPIX Upgrade Mechanics

→ 1216 modules → 81M pixel
(1.6 x present BPIX)



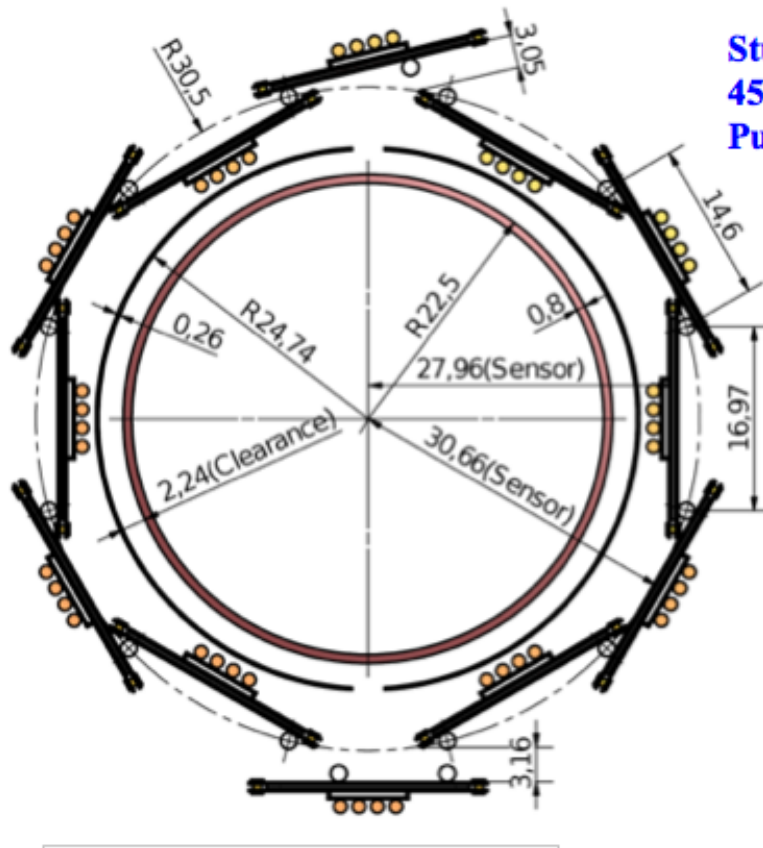
- Full module type only
- | |
|----------------------------|
| Layer 1: R 39mm; 16 faces |
| Layer 2: R 68mm; 28 faces |
| Layer 3: R 109mm; 44 faces |
| Layer 4: R 160mm; 64 faces |
- Clearance to beam pipe 4mm
(present)

baseline



If beam pipe $r < 22.5\text{mm}$ → 1st Layer: 12 faces $\langle R \rangle = 29.5\text{mm}$

Project for new beam pipe



Studies are ongoing to assess safe beam pipe radius.
45 mm diameter seems doable.

Pushing for Beam Pipe installation in LS1 2013

- mean 1st layer Si- radius = 29.8 mm from 44
- need 2 mm clearance to beam pipe
- need adjustable closing mechanism
- Beam pipe diameter 45 mm from 58

How is the Pixel Flux with the new beam pipe ?

Estimation of fluxes with an Analytical Calculation – $L=2E34$

TECH. PROPOSAL WITH $R=3.9$ cm
(L1)

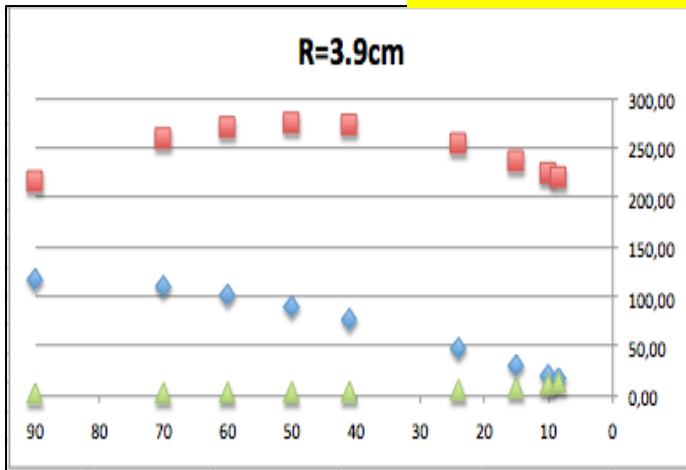
PSI Estimation

Data Rate Estimations, 25ns

- Full 4 layer phase I geometry
- Assuming 24 bits per hit, 100kHz L1A
- Peak lumi= $2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, $\sigma_{\text{tot}}=80 \text{mb}$, $\sigma_{\text{signal}}=1.5 \text{mb}$
- Data rate includes headers/trailers
- Bandwidth of present analog links $\approx 100 \text{ Mbit/sec peak}$

Layer	1	2	3	4
Pixel fluence [MHz/cm^2]	251	108	48	27
Hits / trigger / module	70	35	16	8.4
MBit/link/sec	204	107	61	40.0
# links	128	224	352	512

My Estimation



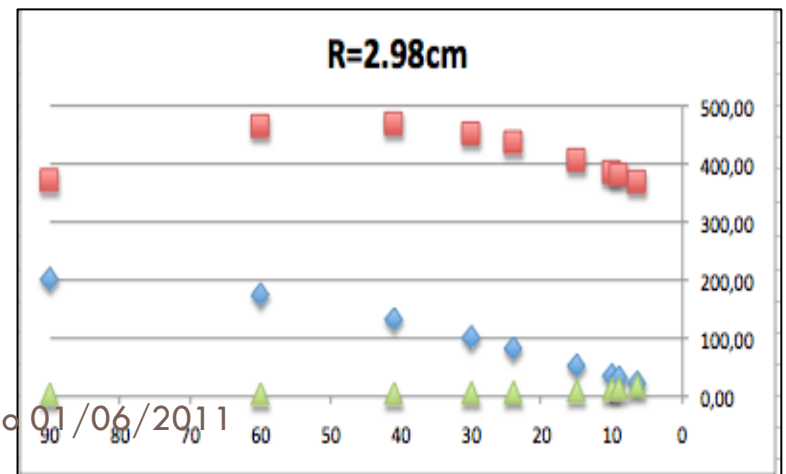
Pixel rate vs Theta

Pixel Upgrade ROC

9. March 2011

5

**NOW NEW PROJECT FOR BEAM PIPE
REDUCED Radius $R=2.98$ cm
RATE goes to $\sim 500 \text{ MHz}/\text{cm}^2$**



Uma Demora - New Pixel Chip - Torino 01/06/2011

September 2011: Engineering run with 3 ROC versions

- 1) Existing ROC (PSI46)
- 2) Existing ROC + enlarged data buffer 32 → 80 (PSI46xdb)
- 3) Same as 2) + Readout buffer and digital readout (PSI46dig)
- 4) Test Structures, TBM

2012: PSI46dig + Data buffer skip mechanism in double column to remove dc-reset loss (PSI46digx)

My comment:

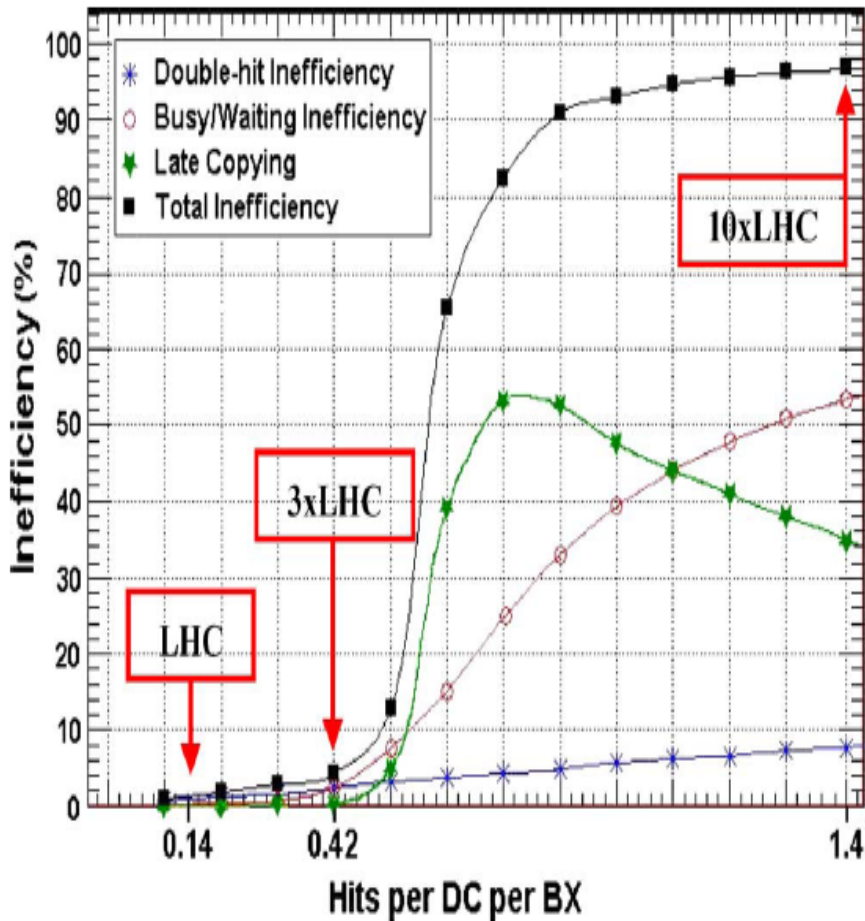
- Layer 2,3 and 4 are clearly OK
- Layer 1 has to be understood better

Simulation Studies for the smaller beam pipe yet to be done. It will be interesting to see what are the consequences on the buffering at EoC and on the overall deadtime.

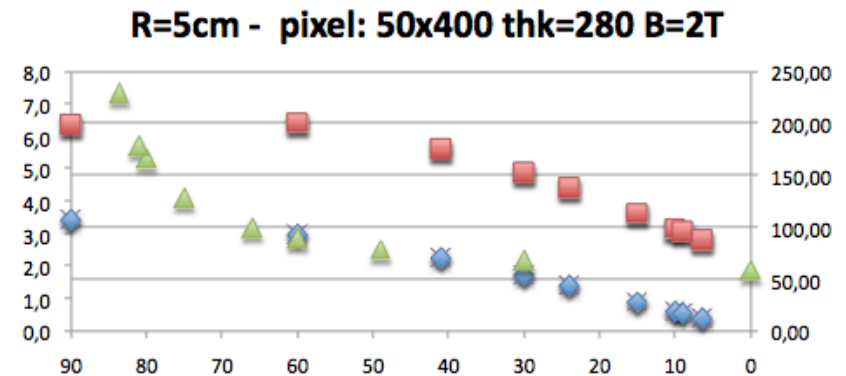
What is Atlas Doing ?

Present Atlas CHIP

FEI3: drain architecture, ToT, 0.25 μm

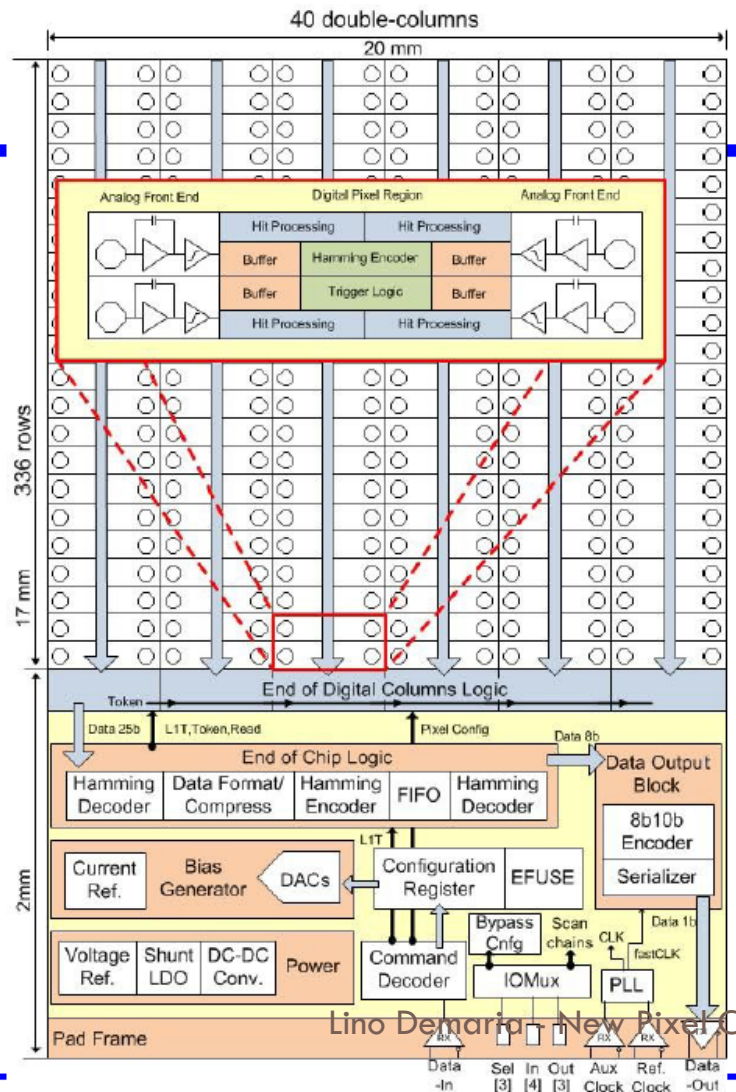


For Atlas chip, at 5cm radius, $L=3 \cdot 10^{24}$ the chip reach saturation



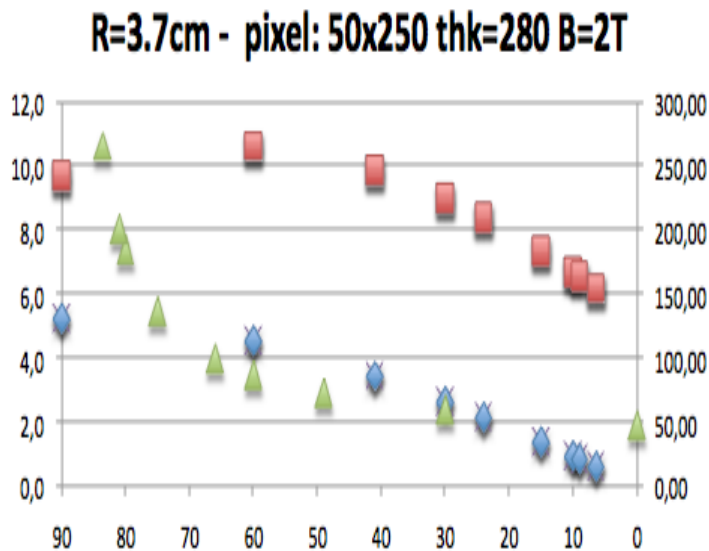
THIS IS the estimate of Pixel flux for $L=3E34$ with FEI3 geometry

FEI4: new chip in 130nm



- Regional architecture,
 - ▣ data memorized in Region of 4 PUCs
 - ▣ N-buffer to store data
- Data are canceled at $\sim 99.75\%$ after trigger latency
- ToT is used for signal amplitude
- Only good data go to EoC at each trigger

Pixel flux conditions for FEI4 chip @ L=2E34



Interesting to see that in the end the pixel flux is \sim same as for CMS phase 1.

The smaller pitch is balanced by a smaller magnetic field (cvd)

How many buffers ?

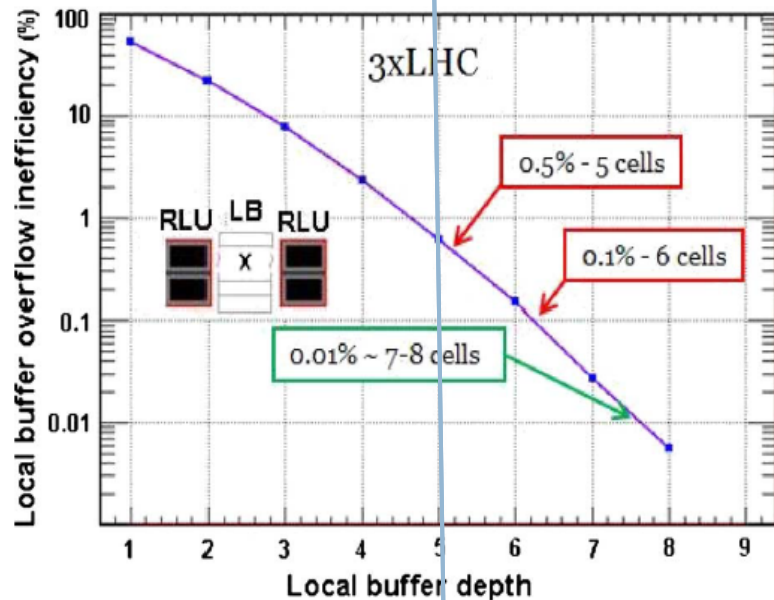


Fig. 7. Full simulation result. LB overflow inefficiency as a function of LB depth for the IBL. The structure used here consists of two RLUs of two pixels each sharing a single LB.

TABLE I
LB OVERFLOW INEFFICIENCY, POWER AND AREA ESTIMATE FOR 2 DIFFERENT
RLU IMPLEMENTATIONS AT $\tau = 3.7 \text{ cm}$

	1RLU \times 4pix (6 memories)		2RLU \times 2pix (6 memories)	
Luminosity	3x LHC	10x LHC	3x LHC	10x LHC
LB overflow inefficiency[%]	0.01	0.65	0.11	3.29
4-pixel region area [μm^2]	100 \times 156		100 \times 128	
Power/pixel[μW]	2.75	5.19	2.72	5.12

For IBL 5 buffers have been chosen

Trigger Latency is important

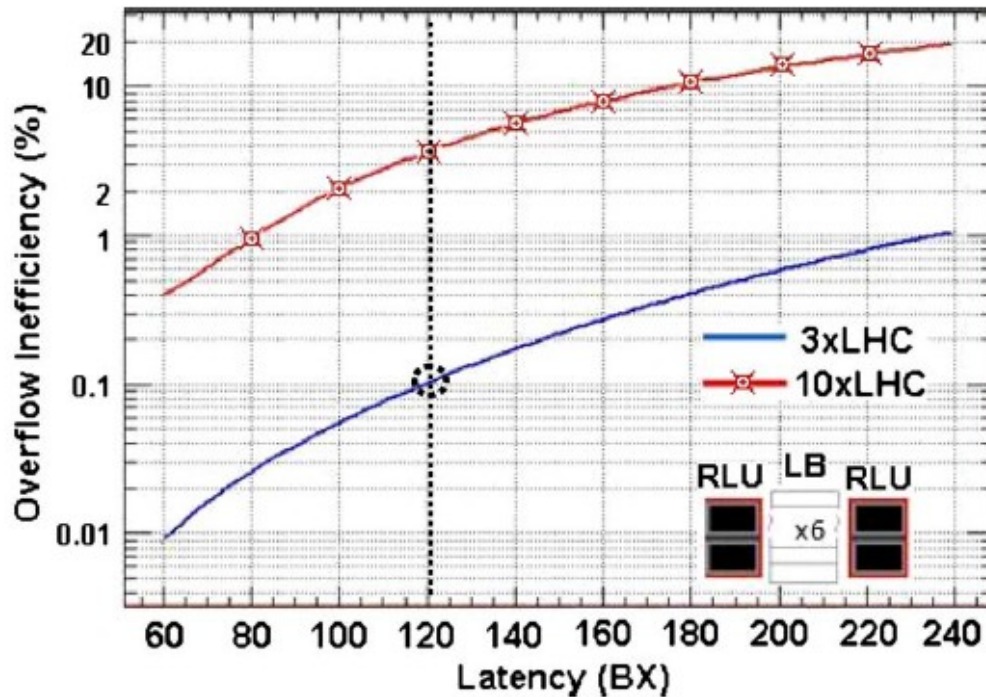


Fig. 6. LB overflow (in percent) calculated analytically as a function of L1T latency (in bunch-crossings), for a 3.7 cm radius layer, with 2 RLU's of 2 pixels each tied to a single 6-memory cell LB.

ToT is important

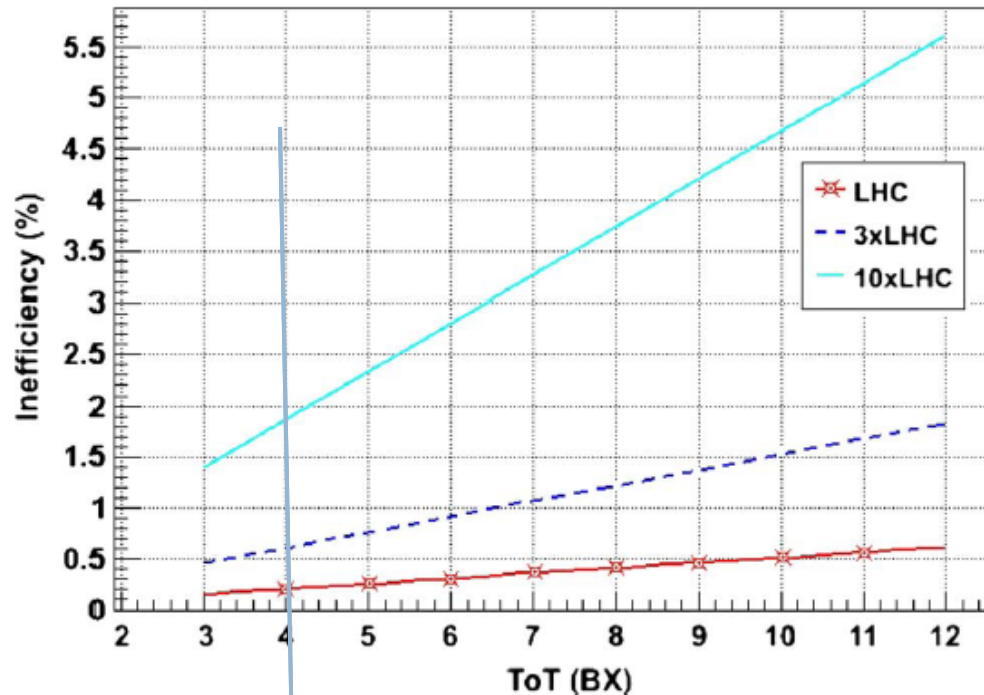
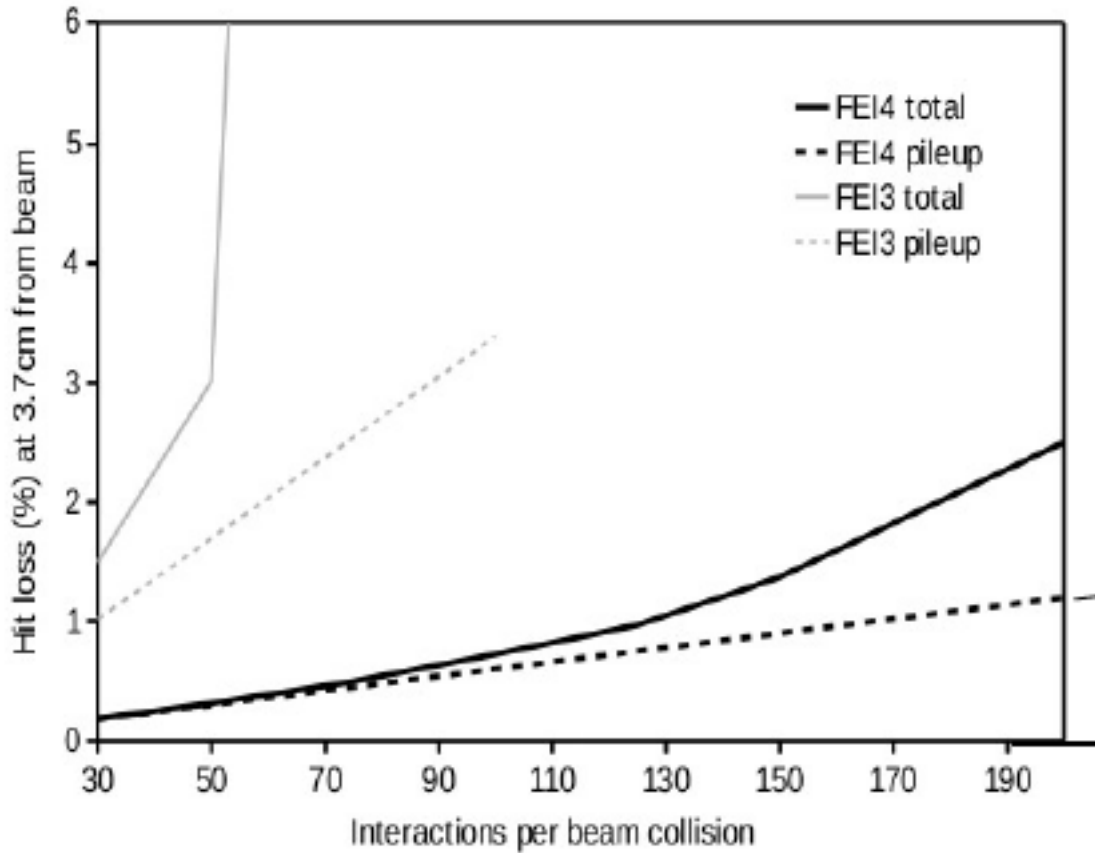


Fig. 4. Single pixel pile-up inefficiency (in percent) as a function of the mean ToT (in unit of bunch-crossings) as calculated analytically for a 3.7 cm layer for the new pixel size of $50 \times 250 \mu\text{m}^2$.

4 BX chosen for IBL at 3.7cm

FEI4 estimated overall inefficiency



This was shown at ACES: not completely clear to me if this plot is compatible with previous plots...

BTW:
we need to remember Atlas still has to do HIGH rate tests to certify the performances



..... NOW ...

→ We should ask ourself

- Why not using FEI4 ?
 - ▣ Change pixel geometry from 100x150 to 50x250 μm^2
- or an adapted FEI4 to the CMS pixel geometry ?
 - ▣ Work with FEI4 team ?
- Or we make a new chip ?
 - ▣ Take in mind FEI4 in Atlas is for:
 - IBL phase 1
 - Layer (2),3,4 for phase 2
 - ▣ We should make a chip that ANSWER to the request of Phase 1 (2007-2008), but with a target in mind of a L1 in phase 2 where there will be new sensor technology

Technical specs: main ingredients for the Loss Mechanisms in Pixel Cell

- How many signal have to be stored every BX: Pixel Flux. Determined by Particle and by Pixel cluster size, important:
 - Pixel size in Rphi
 - charge sharing due to Lorentz angle
 - Pixel size in Z
 - Sensor thickness
- Trigger Latency
- Pixel Dead Time
 - ToT

Sizes comparisons

- Choice of Rphi
 - Should give same resolution as today
 - Deterioration from high irradiation
 - Dealing with digitalized information
 - Still profiting from $B=3.8T$, should result larger than Atlas
- Choice of Rz
 - Resolution should remain superior than Atlas, we aim to remain as good as now
 - Balance among dimension and area in the pixel
 - I would not go below the present $150\ \mu\text{m}$
 - I would investigate if larger could be better
- Practical aspects are important too
 - We should be compatible with existing sensor material if we want to bond chip and sensor
 - Rphi: 50 (several); 80
 - Z: 150

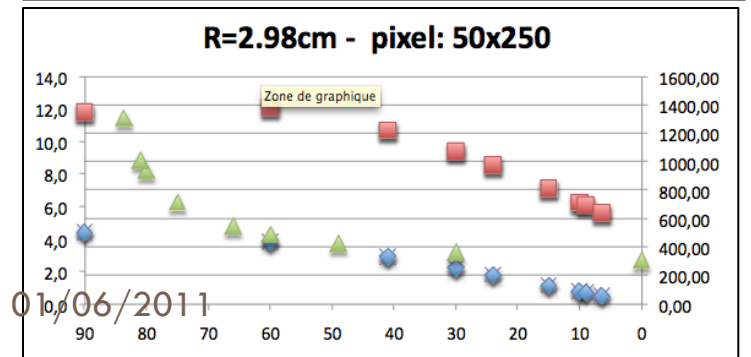
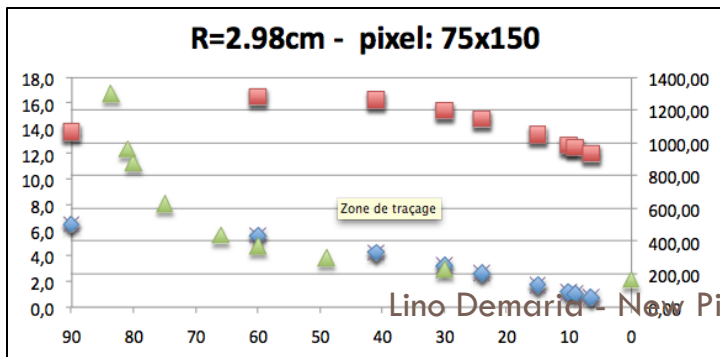
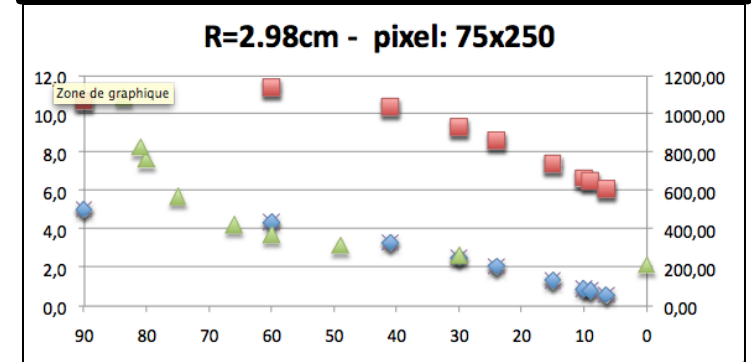
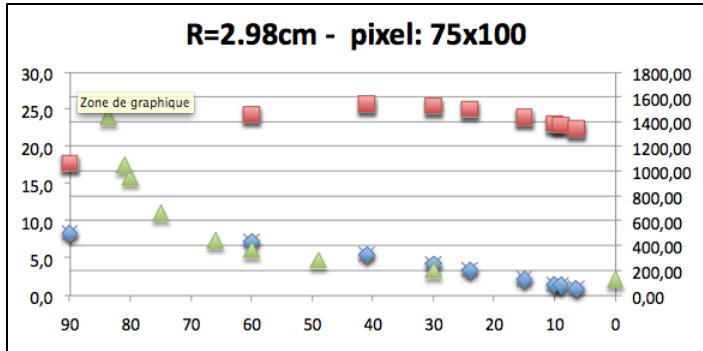
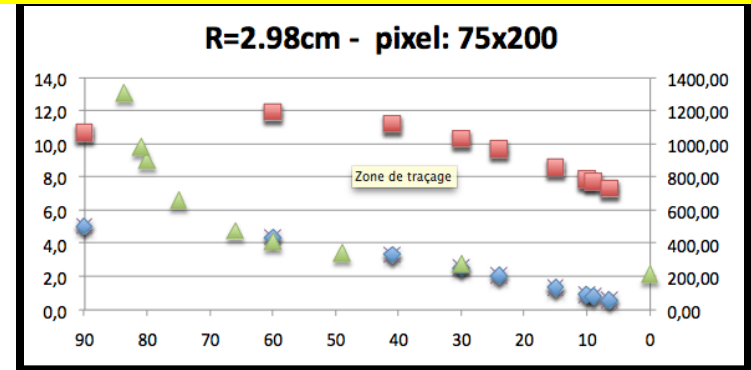
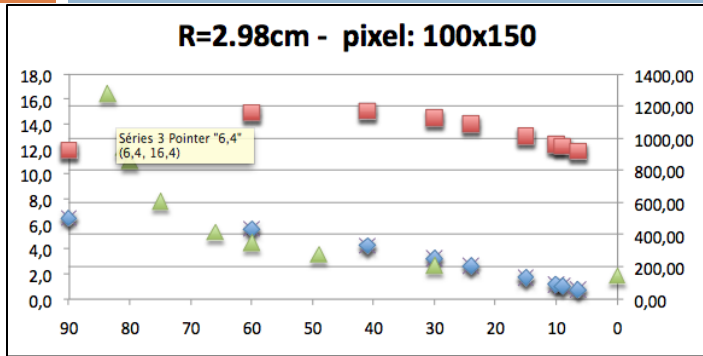
Choosing pixel size

	Rphi	Z	binary res-rp	binary res-z	binary 1/2 pitch rp	binary 1/2 pitch z	AREA pixel	real res-rp	real res-z
CMS NOW	100	150	28.87	43.3	14.43	21.65	15000	8	25
Atlas NOW	50	500	14.43	144.3	7.217	72.17	25000		
Atlas IBL	50	250	14.43	72.17	7.217	36.08	12500		
Panda	100	100	28.87	28.87	14.43	14.43	10000		
Fall Forward	75	100	21.65	28.87	10.83	14.43	7500		
1 optim.rphi	75	150	21.65	43.3	10.83	21.65	11250		
2 optm.rphi+enl.z 1	75	200	21.65	57.74	10.83	28.87	15000		
3 optm.rphi+enl.z 2	75	250	21.65	72.17	10.83	36.08	18750		

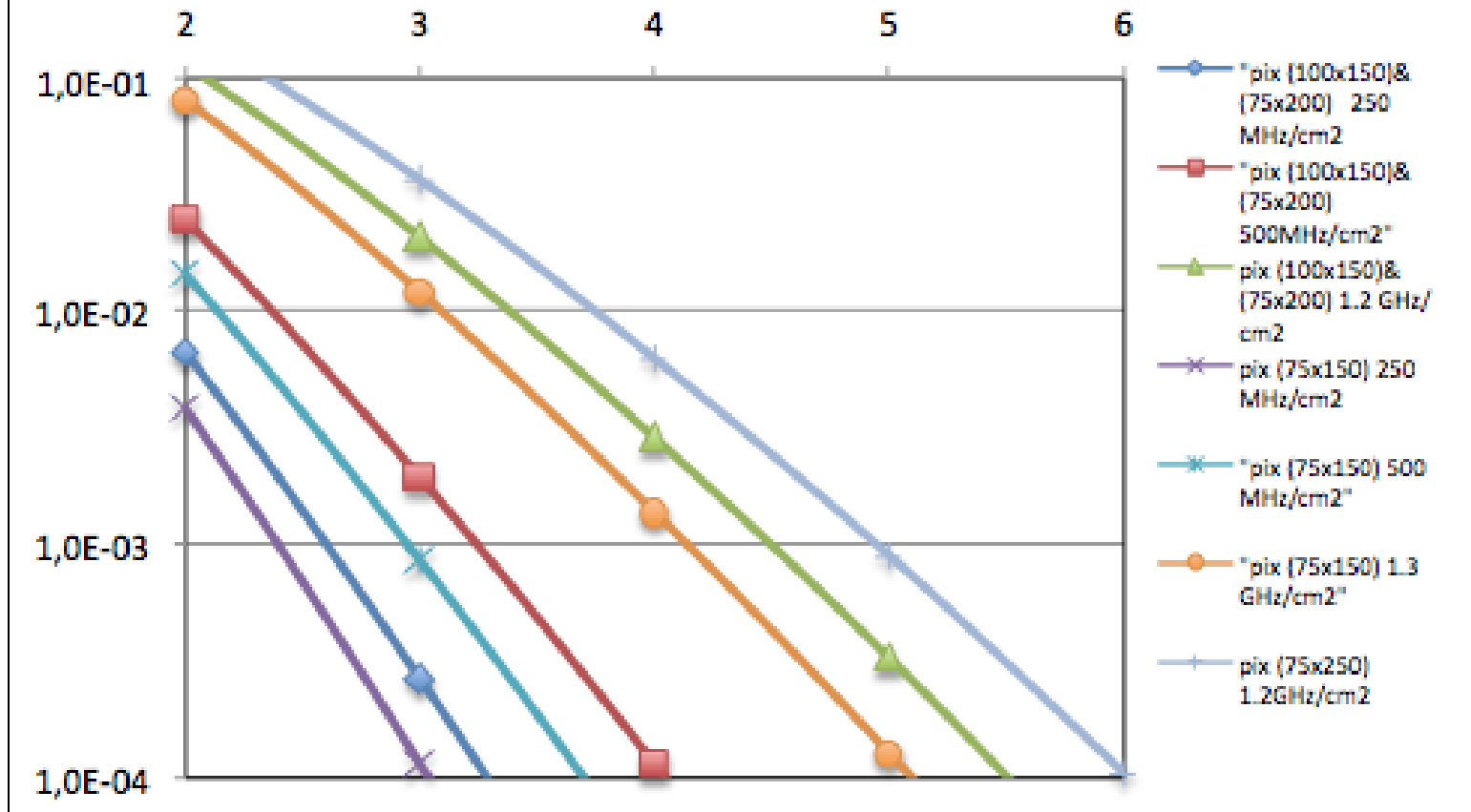
1. **Fall Forward** solution is un-necessarily small in Z (→huge clusters)
2. Solution **75x150** should be at least **equivalent to present** one but more robust in term of R-phi resolution
3. Solution **75x200** should be evaluated. Rphi should be at least as good as Atlas (magnetic field 3.8T) and Z resolution is **still better than ATLAS but has more space in PUC**
4. Solution 75x250 should be still as good as Atlas in term of resolution on both directions. Area available for electronics on pixel is 50% larger → more electronics on pixel is possible

Pixel rate @L=(5x10³⁴) for different pixel cells –thickness =280 micron

NB: green dots are the cluster size (theta is reversed)



PUC Inefficiency vs #Buffer (T-latency=3.2)

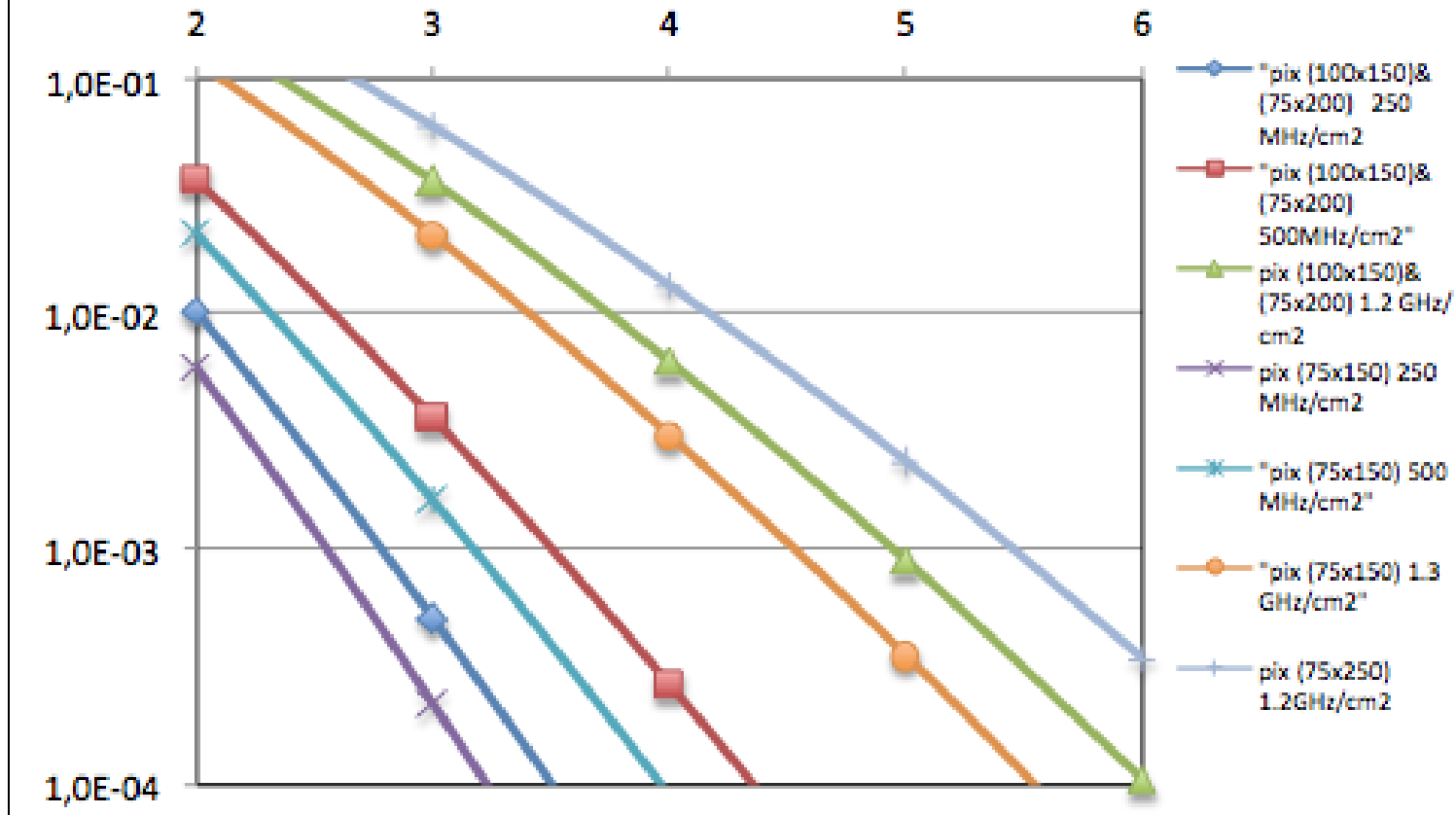


THIS graph applies to the solution of buffering in the PUC the signal until next trigger is arrived (trigger latency =3.2 microsec).

4 buffers allow to reach Phase 2 with $\ll 1\%$ losses;

5 buffers allow to reach Phase 2 with $\ll 0.1\%$ losses;

PUC Inefficiency vs #Buffer (T-latency=4.0)

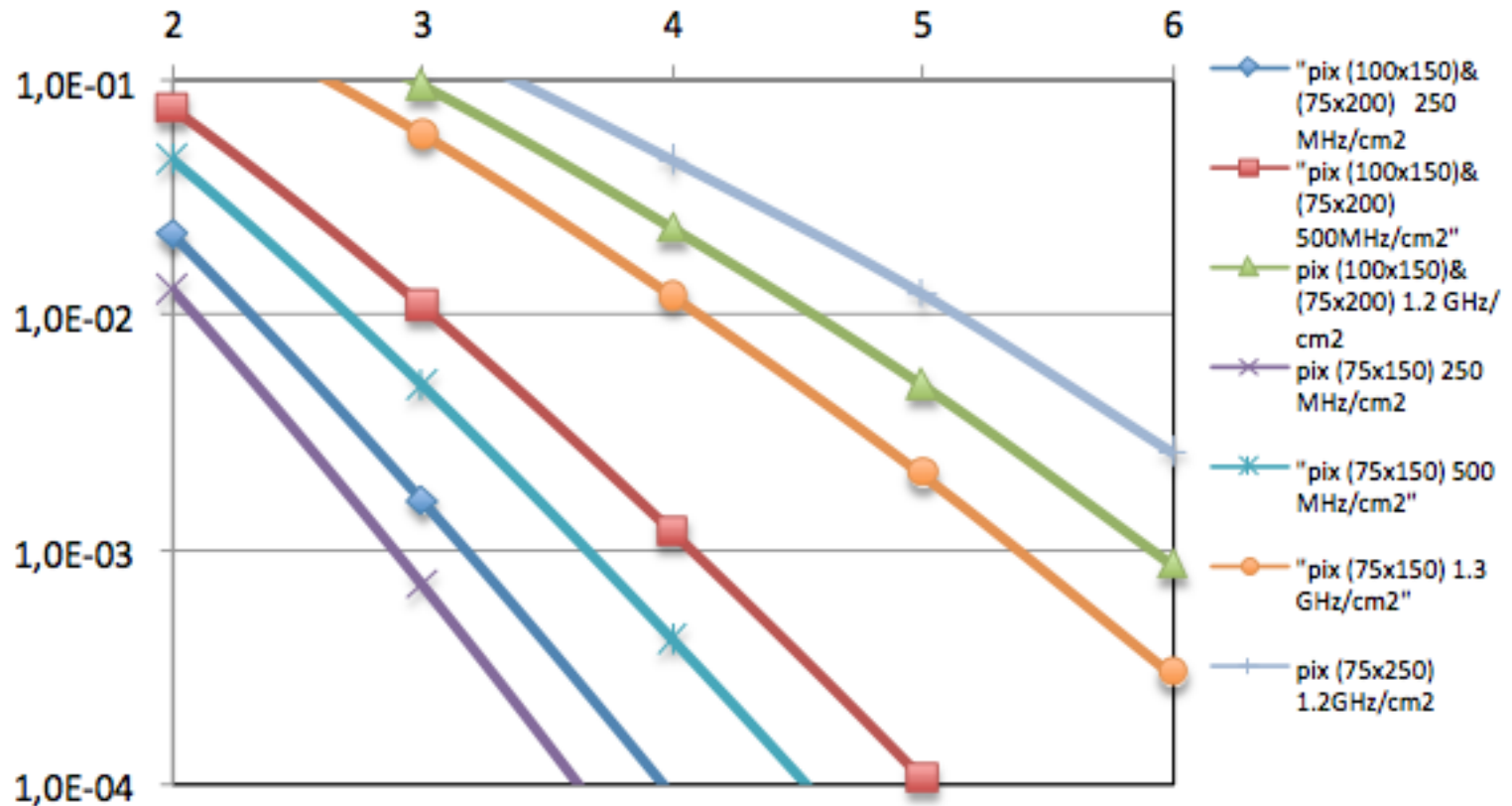


THIS graph applies to the solution of buffering in the PUC the signal until next trigger is arrived (trigger latency =4.0 microsec).

5 buffers allow to reach Phase2 with <1% losses;

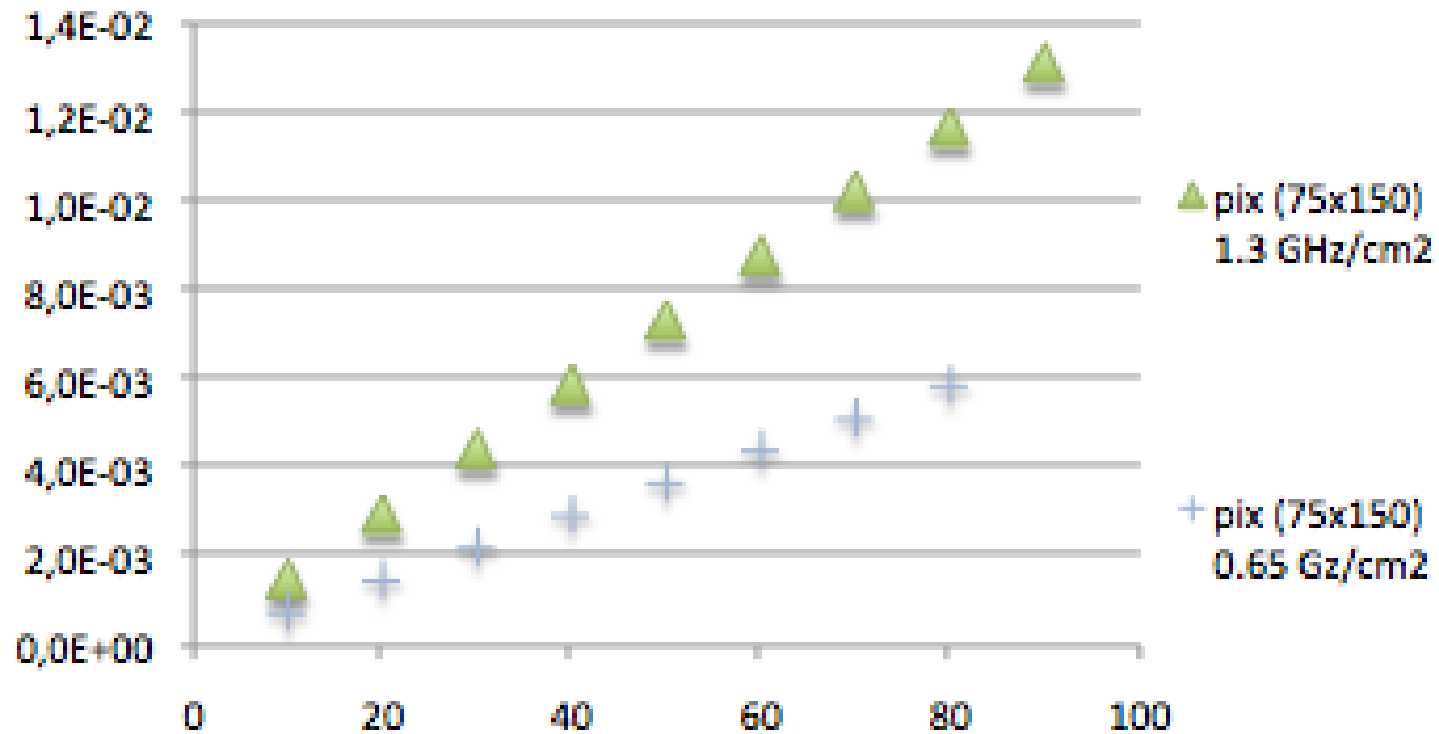
6 buffers allow to reach Phase2 with ~0.1% losses;

PUC Inefficiency vs #Buffer (T-latency=6.0)



Phase 2 is considering to have all sub-detectors supporting 6 micro-sec trigger latency (Tracking Trigger takes time...)

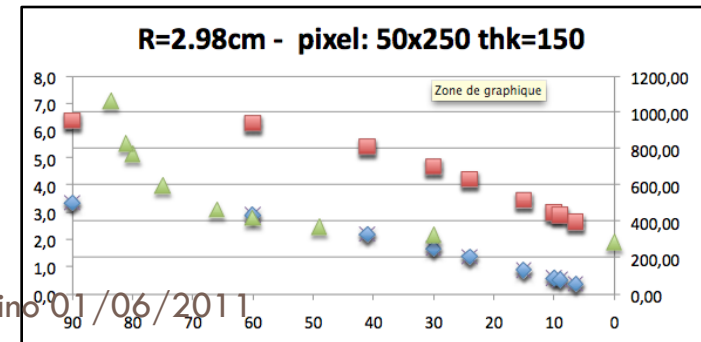
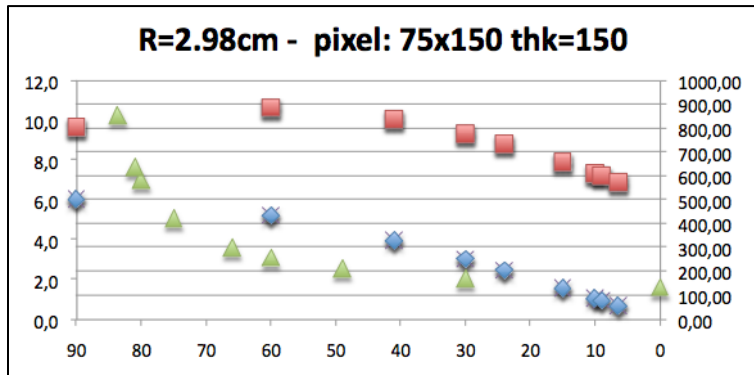
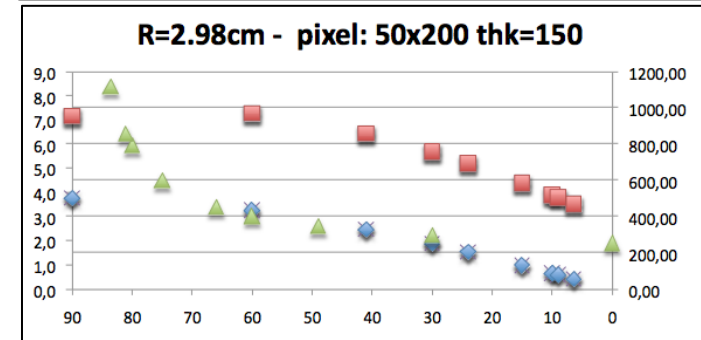
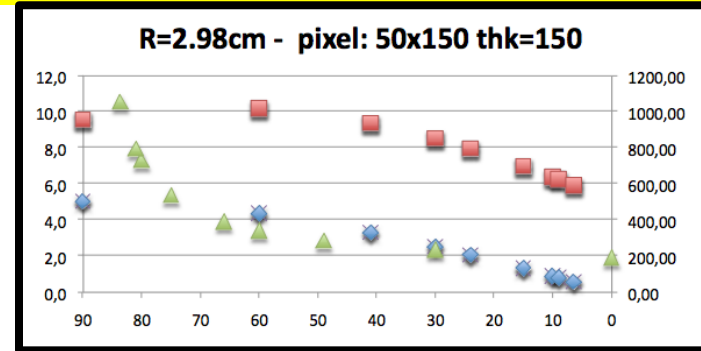
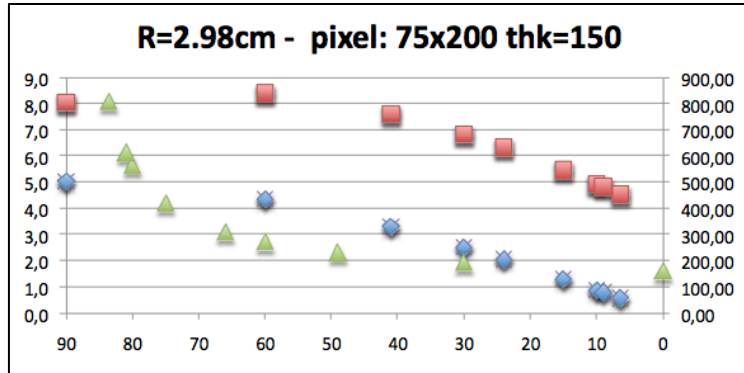
PUC Inefficiency vs ToT duration (nsec)



Sensor is important

Pixel rate @L=(5x10³⁴) for different pixel cells – thickness = 150 micron

NB: green dots are the cluster size (theta is reversed)



Conclusion

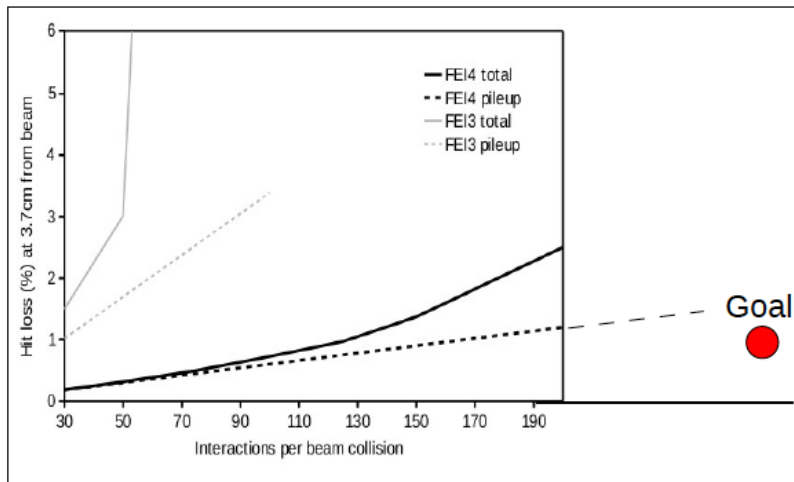
- New ROC is the main baseline for Phase 1
 - ▣ Good conservative approach but it limited precisely by that (250nm; PUC/architecture unchanged)
 - ▣ Problems foreseen for Layer 1 already with $R=3.9\text{cm}$; they will not improve at 2.98cm
- Good moment to start a project of a new chip: we should do it
 - ▣ We should set our technical specs above phase 1, studying phase 2 regime already
- We should profit from CMS case: same performance as Atlas (or better) with larger PUC
- Technology wise we should start with 130nm but in future we should not forget larger integration scale (90/60/35 nm)
- Sensor will be an important ingredient to be taken into account
 - ▣ Thickness could allow better segmentation or higher rates

BACKUP

Atlas looking to the future

Beyond FE-I4

- Still higher rate capability
- Need smaller, faster pixel
- Yet need more memory per pixel to buffer higher rate
- Two directions being explored: 3D and 65nm



FE-I3 pixel -- 3.2 bits

FE-I4 -- 25 bits

⋮

? ~35 bits