DRD3 - Solid State Detectors
- Research Proposal (Version 3.1) -

DRD3 Proposal Team

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1 Scope of the DRD3 collaboration

The DRD3 collaboration has the dual purpose of pursuing the realization of the strategic developments outlined by the Task Force 3 (TF3) in the ECFA road map [1] and promoting blue-sky R&D in the field of solid-state detectors.

2 Introduction

Solid State detectors (SSD) based on semiconductors, and in particular silicon detectors (planar pixels, planar strips, and 3D pixels), are used in almost all particle physics experiments. Since they can be easily segmented using standard photolithographic techniques, they can achieve superb position resolution and play a key role in measuring primary and secondary vertices and tracking charged particles. Silicon is also used as an active medium in particle flow calorimeters to associate showers with tracks from trackers and track showers as they develop in the calorimeter.

Revolutionary improvements of SSD performance are needed to match the requirements of future experiments. All-silicon trackers are required for future hadron colliders such as FCC-hh and are one of the most competitive options also for e^+e^- Higgs factories. There are commonalities in the possible SSD technological choices since both hadrons and e^+e^- colliders require low mass, low power, high-resolution trackers. Nonetheless, there are also differences since hadron colliders necessitate ultra-fast detectors, enabling 4D-tracking[1], to deal with multiple interactions occurring within a bunch crossing. Detectors at FCC-hh must also achieve unprecedented radiation hardness. The highest levels are reached in the forward calorimeters where the total ionizing dose and the 1-MeV equivalent neutron fluence rise to values of 5000 MGy and $5 \cdot 10^{18}$ n_{eq}/cm^2. Even in the innermost layer of the barrel vertex detectors, the fluences approach $1 \cdot 10^{18}$ n_{eq}/cm^2 after an integrated luminosity of $30\,ab^{-1}$.

After years of R&D, silicon sensors manufactured using mainstream CMOS imaging technologies are now being implemented in several high energy physics (HEP) experiments. CMOS MAPS (Monolithic Active Pixel Sensor) have now been installed in STAR and ALICE; they are planned for other experiments as CBM, LHCb tracker, and Mu3e. MAPS technologies are especially suited for applications requiring low-mass and excellent position resolution called for at electron machines.

Future flavour physics experiments will operate in a high-occupancy environment where event reconstruction will be very challenging. The physics program enabled by the LHCb Upgrade II relies on an efficient and precise vertex detector with real-time reconstruction of tracks from all LHC bunch crossings in the software trigger system, which would benefit from having 4D-tracking. The higher occupancy expected in future running will also demand increased detector granularity for the LHCb tracker.

Reduction of material in the region close to the interaction point leading to significant improvements in tracking precision and efficiency at low transverse momentum is criti-

[1]Reconstructing the trajectory of a charged particle in three spatial dimensions plus time as a fourth dimension

cal to achieving the physics goals of Heavy Ion experiments, such as ALICE, and those planned for the EIC and particularly at future e^+e^- colliders. Better position and timing resolution and lower power consumption would also benefit the upgrades of Belle and NA62, which will occur in this decade. Devices with $\mathcal{O}(10\,\mathrm{ps})$ timing resolution will be highly desirable for 4D-tracking reconstruction at the foreseen 1000 collisions pile-up of the FCC-hh.
One aspect common to most future facilities is the requirement for the front-end electronics to perform very complex tasks, such as those required for 4D-tracking or by the transfer off-chip of very large data volume. 3D-stacking is, therefore, a key technological development that needs to be included in the future high-performing trackers.

Following these needs, TF3 has identified the essential Detector R&D Themes (DRDT) that capture the most critical requirements.

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass, aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity, are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored as a complement to standard sensors fabricated in specialized clean room facilities towards hybrid, where the sensors are bonded to an independent ASIC circuit. Passive CMOS sensors are good candidates for calorimetry applications where position precision and lightness are not major constraints. State-of-the-art commercial CMOS imaging sensor (CIS) technology should be explored for suitability in tracking and vertex detectors.

DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry
Understanding the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research and developments to increase radiation tolerance and achieve 100% fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.
DRDT 3.3 - Extend capabilities of solid-state sensors to operate at extreme fluences
To evolve the design of solid-state sensors to cope with extreme fluences, it is essential to measure the properties of silicon and diamond sensors in the fluence range $1\cdot10^{16}\ \mathrm{n_{eq}/cm^2}$-$5\cdot10^{18}\ \mathrm{n_{eq}/cm^2}$ and to develop simulation models correspondingly including microscopic measurements of point and cluster defects. All technologies will need improved radiation tolerance for use at future hadron collider experiments. Exploration of alternative semiconductors and 2D materials should timely start having as target the proper functioning at the extreme fluences present in the innermost parts of the detectors. A specific concern to address is the associated activation of all the com-

ponents in the detector. Exploration of alternative semiconductors and 2D materials is desirable to push radiation tolerance further.

DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics
3D interconnection is commercially used, for instance, in imaging sensors, to use the most appropriate technology process for the different functionalities of the devices. This process would allow particle physics detectors to be more compact and lighter devices with minimal power consumption. This approach also provides an alternative to the use of deeper nodes to enable lower pitch and new digital features. An enhanced R&D effort in building a demonstrator as a starting cornerstone is highly desirable. A demonstrator program is to be established to develop suitable silicon sensors, cost-effective and reliable chip-to-wafer and/or wafer-to-wafer bonding technologies, and to use these to build a multi-layer prototype with vertically stacking layers of electronics interconnected by through-silicon vias and integrating silicon photonics capabilities.

Figure 1 shows the timeline of experiments that are already planned or at the proposal level. In the following, their needs are used to define the most important strategic R&D planned for the next few years.

Figure 1: Timeline of the near-term R&D

2.1 The DRD3 research structure

The DRD3 structure is based on a number of mainstream activities related to solid state detectors. At the moment, the following eight Work Groups (WG) are foreseen [2]:

1. WG1 Monolithic silicon technologies
2. WG2 Hybrid silicon technologies
3. WG3 Radiation damage characterization and sensor operation at extreme fluences
4. WG4 Simulations
5. WG5 Characterization techniques, facilities

6. WG6 Wide band-gap and innovative sensor materials
7. WG7 Interconnections and device fabrication
8. WG8 Dissemination and outreach

These working groups have an interplay with the Work Packages (WP) defined in the Solid State Detectors chapter of the 2021 ECFA Road-map. The Working Groups link together activities broadly focused on Research Goals (RGs). WGs aim at long term R&D activity linked to certain technology, purpose and application. They encompass R&D that can also reach outside the scope of DRDTs, but it is related to semiconductor detectors and is of benefit for the particle physics detector community.

The conveners of the WG will steer the research towards realization of RGs, monitor the work progress, strive to include new institutions in the research activities and coordinate activities across the WGs.

The Work Packages are meant to address the need of the strategic R&D objectives on short to mid term. These Work Packages are largely defined by the four strategic Detector R&D Themes (DRDT). Each DRDT defines a work package (WP), with associated deliverables and milestones.

1. WP1, DRDT 3.1, Monolithic CMOS sensors
2. WP2, DRDT 3.2, Sensors for 4D-tracking
3. WP3, DRDT 3.3, Sensors for extreme fluences
4. WP4, DRDT 3.4, 3D-integration & interconnections

The activities of four WGs map directly into WPs, while WP3 is also closely linked to WG6. Other WGs are transversal, and their activities benefit all WPs. It should be emphasized that these links are not exclusive and WPs should benefit from all WGs. These relationships are shown in Figure 2.

The four work packages are divided into specific tasks as summarized in Table 1, each task is focused on a given topic. The tasks will be realized through WP projects. These will focus on one or more tasks. The WP projects will be proposed by interested groups and will include resource loaded schedule with clear milestones and deliverables. These should be compatible with broader milestones and deliverables of the given WP.

The coordinators/leaders of the WP will shape the WP projects in a WP proposal, look for synergies between the projects, monitor progress and will be responsible for reporting. The WP leaders can also serve as conveners of directly mapped WGs. The number of conveners and their responsibilities will be decided by the elected DRD3 spokesperson (together with his management) in line with the rules of the collaboration.

Figure 3 summarizes the DRD3 research structure.

- Research and networking is organized in work groups (WG)
- Strategic R&D is organized into four work packages (WP) with associated broad milestones and deliverables.

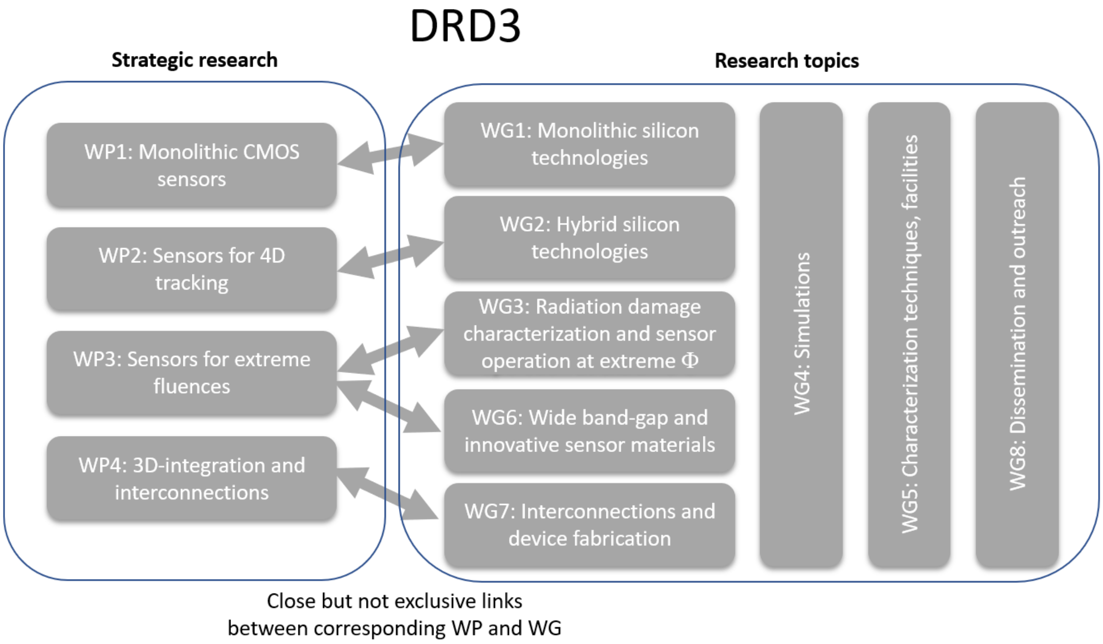

Figure 2: Relationship between Work Packages (WPs) and Work Groups (WGs)

- Blue-sky R&D is promoted via common projects (CP) and other forms of collaboration such as common test beams, equipment, schools, and personnel exchange.

2.2 Common R&D

One of the main goals of the DRD3 collaboration is to foster blue-sky research and collaboration among groups. The main tool to achieve these goals is creating a fund to finance selected common projects (CP). It is foreseen that each proposed CP finds 50% of the financing among the proponents, while DRD3 finances the other 50%. To access the DRD3 contribution, each CP has to be presented to the collaboration for evaluation. This research fund is financed by an annual fee of about 2,000 CHF, which each institute must pay.

2.3 Institutes participation to working groups and work packages

Figure 4 reports the number of institutes willing to contribute to each working group, while Figure 5 reports the same information for work package and task. In both figures, the institutes can show interest in more than one WG or Task. The figures show that the interest of the collaboration members is well distributed across WGs and WPs.

WP	Task	Title
1	1.1	MCMOS: spatial resolution
1	1.2	MCMOS: timing resolution
1	1.3	MCMOS: read-out architectures
1	1.4	MCMOS: radiation tolerance
2	2.1	4D tracking: 3D sensors
2	2.2	4D tracking: LGAD
3	3.1	Extreme fluence: wide band-gap materials (SiC, GaN)
3	3.2	Extreme fluence: diamond-based detectors
3	3.3	Extreme fluence: silicon detectors
4	4.1	3D Integration: fast and mask-less interconnect
4	4.2	3D Integration: in house post-processing for hybridization
4	4.3	3D Integration: advanced interconnection techniques for detectors
4	4.4	3D Integration: mechanics and cooling

Table 1: Tasks for each of the four work packages.

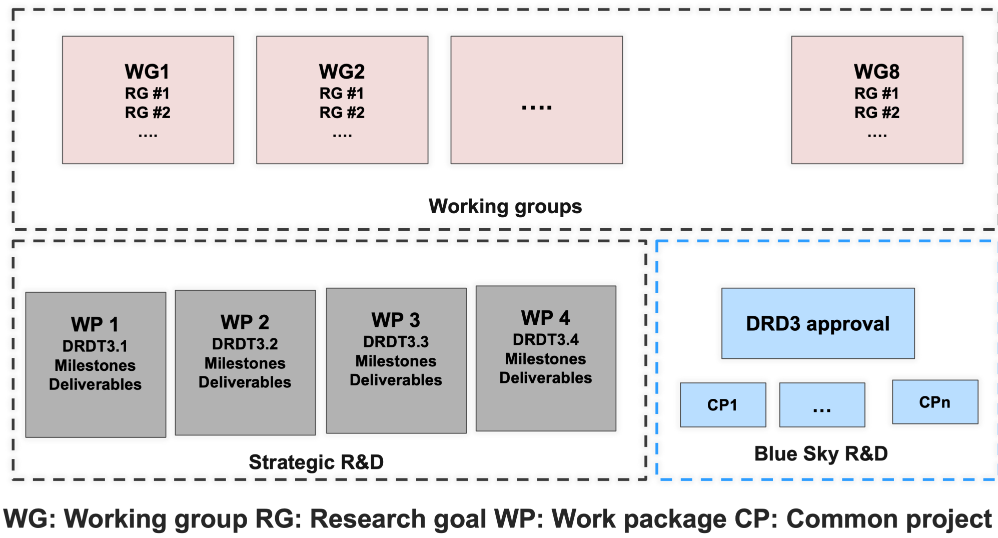

Figure 3: The research structure of the DRD3.

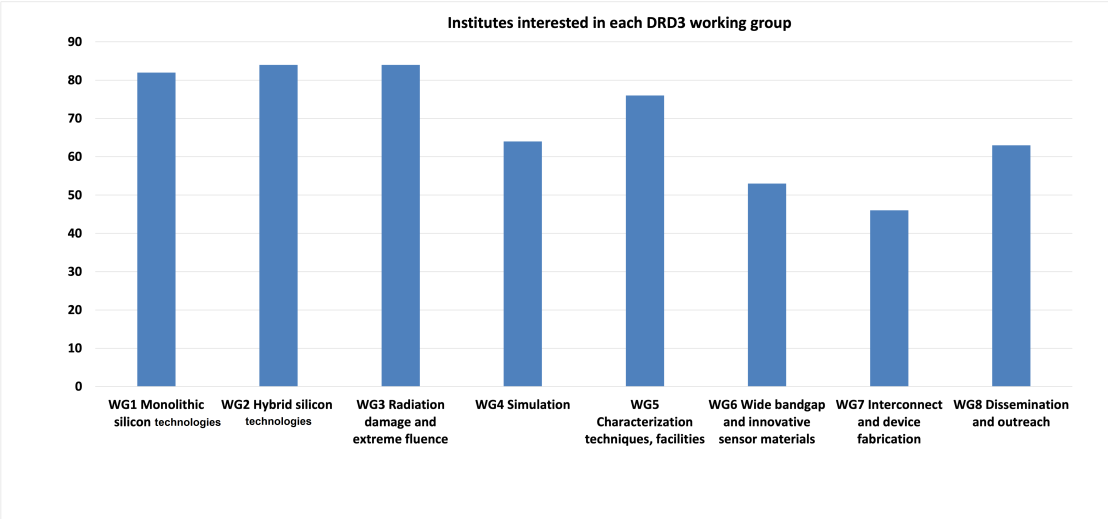

Figure 4: Number of institutions interested in each working group.

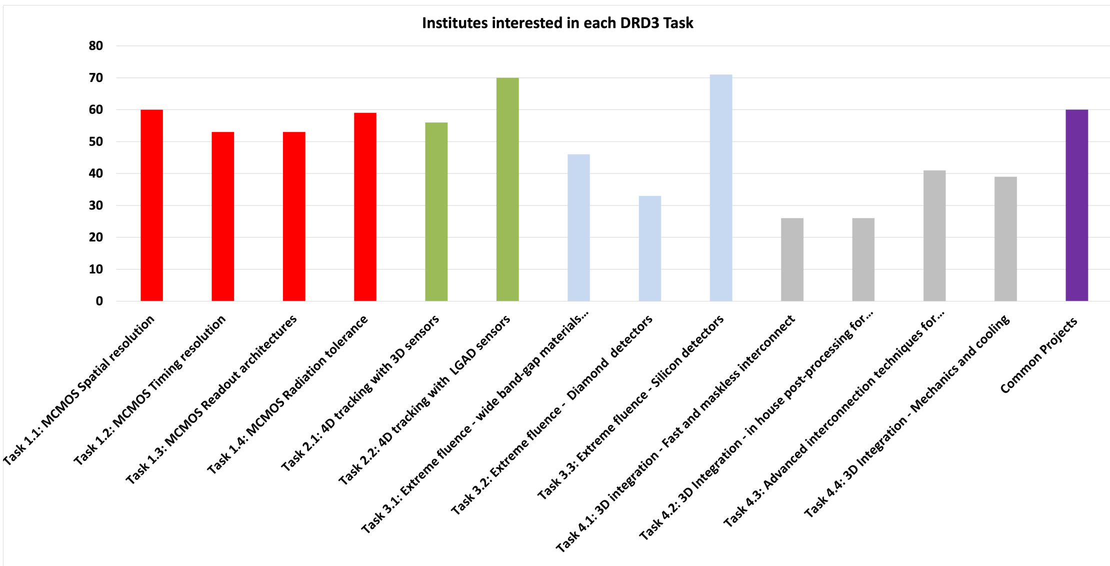

Figure 5: Number of institutions interested in each work package and task

Figure 6 details the number of institutes interested in each WG for each country.

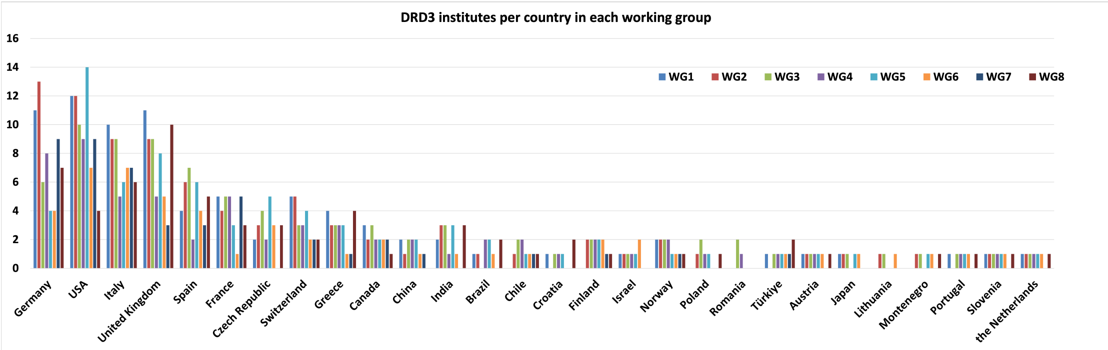

Figure 6: Number of institutes interested in each WG for each country.

2.4 Milestones and deliverables

Table 2, 3, 4, and 5 report the list of the milestones and deliverables for each work package. The complete list of 129 institutions participating in each work package and task is provided in Annex - III.

WP	Task	MS or D	Description	2024	2025	2026	2027-2029	> 2030
1	1.1	MS1.1	Establish position precision versus technology, channel configuration and readout mode (2026), handle technical solutions for several tracking applications (2027)			x	x	
1	1.2	MS1.2	Establish time precision versus technology, channel configuration (2026), handle technical solutions for timing applications (2027)			x	x	
1	1.3	MS1.3	Establish performance of readout variants for power consumption (2026), handle technical solutions for low power (2027)			x	x	

1	1.4, 3.3	MS1.4	Establish radiation tolerance, provide guidelines for choice of substrates (2026), handle technical solutions for tracking applications with high radiation tolerance (2027)			x	x	
1	1.1, 1.2, 1.3, 1.4	D1.1	Several MPW1.1 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2024, and TJ 65 nm in 2025)	x	x			
1	1.1, 1.2, 1.3, 1.4	D1.2	Several MPW1.2 submissions in the identified technology processes (TJ/TSI 180 nm, LF 110/150 nm and IHP 130 nm in 2026, and TJ 65 nm in 2027)			x	x	
1	1.1, 1.2, 1.3, 1.4	D1.3	Several MPW1.3 submissions in the identified technology processes (all identified technologies in 2028 and beyond)				x	

Table 2: Work package 1: tasks, milestones, and deliverables.

2	2.1	MS2.1	Reduction of the pixel cell size for 3D sensors		x			
2	2.1	MS2.2	Combination of a temporal resolution of about 50 ps and a pixel size of about 50 $\times$ 50 μm^2 in 3D sensors			x		
2	2.1	MS2.3	Improve 3D temporal resolution to around 10 ps				x	
2	2.2	MS2.4	Improve position resolution in LGAD toward about 10 micron maintaining a 30 ps temporal resolution		x			
2	2.2	MS2.5	Improve LGAD radiation resistance up to $5{\cdot}10^{15}$ n_{eq}/cm^2			x		
2	2.2	MS2.6	Improve LGAD temporal resolution to 10 ps				x	
2	2.2	MS2.7	Improve LGAD radiation resistance up to $1{\cdot}10^{16}$ n_{eq}/cm^2				x	

2	2.1	D2.1	Production of 3D sensors with reduced pixel size		x			
2	2.1	D2.2	Large matrix of 3D sensors with reduced pixel size to be coupled to read-out ASIC				x	
2	2.2	D2.3	Production of LGAD sensors with enhanced position resolution		x			
2	2.2, 3.3	D2.4	Production of LGAD with radiation resistance up to $1{\cdot}10^{16}$ $\mathrm{n_{eq}/cm^2}$				x	

Table 3: Work package 2: tasks, milestones, and deliverables.

3	3.2.	MS3.1	Evaluate the possibility of achieving CVD diamond wafers with CCD $>$ 500 μm and variation $<$ 2%				x	
3	3.2.	MS3.2	Study radiation hardness and fast timing ($<$ 30 ps) of diamond detectors at $1{\cdot}10^{16}$ $\mathrm{n_{eq}/cm^2}$ (2026), $0.5\cdot10^{17}$ $\mathrm{n_{eq}/cm^2}$ (2029), $1{\cdot}10^{17}$ $\mathrm{n_{eq}/cm^2}$ (>2030) in planar and 3D geometries			x	x	x
3	3.1.	MS3.3	Fabrication of SiC sensors with different geometries and epitaxial thicknesses (50 μm in 2024 and $>$ 100 μm in 2030).	x				x
3	3.1	MS3.4	Understanding timing performance and validate simulation models of SiC detectors, before irradiation (2024) and at $1{\cdot}10^{15}$ $\mathrm{n_{eq}/cm^2}$ (2030).			x		x
3	2.2, 3.1	MS3.5	SiC-LGAD (gain layer) proof of principle, simulation and first fabrication of devices with small areas ($<$ 1 $\mathrm{cm^2}$ in 2026) and in large areas (5 $\mathrm{cm^2}$ after 2030).			x		x
3	3.1	MS3.6	Assess GaN devices as high-rate, high timing precision devices			x		

3	3.3.	MS3.7	Fabrication and testing of different defect engineered Si sensors (enrichment with O, C and/or P) mimicking the gain layer in LGADs	x				
3	2.2, 3.3.	MS3.8	Understanding the effect of co-doping with O, C and/or P on the radiation hardness of gain layers in LGADs and develop defect engineered strategies for improving the radiation hardness (pin diodes 2026) and then segmented detectors (2029).			x	x	
3	2.1, 3.2	D3.1	Fabricate 3D diamond detectors with cages/interconnects and a base length < 25 μm.			x		
3	3.1	D3.2	Production of SiC large area detectors ($> 1\text{cm}^2$) with pixel and strip geometries in thick epitaxial wafers (> 100 μm).			x		
3	3.1	D3.3	Fabricate and validate Monolithically integrate HEMTs and Schottky diodes on GaN substrates			x		
3	3.3	D3.4	Report on microscopic and macroscopic investigations in irradiated defect engineered gain layers for Si based LGADs			x		
3	3.3	D3.5	Radiation damage studies on various silicon sensors up to $1{\cdot}10^{17}$ $\text{n}_{\text{eq}}/\text{cm}^2$ (2025) and up to $1{\cdot}10^{18}$ $\text{n}_{\text{eq}}/\text{cm}^2$ (2029)		x		x	

Table 4: Work package 3: tasks, milestones, and deliverables.

4	4.1.	MS4.1	Consolidate the connection yield necessary for tracking detectors applications		x			
4	4.1.	MS4.2	Finalise a process optimization that could satisfy pixel pitch of the order of 30 μm or below		x			

4	4.2.	MS4.3	Develop a maskless post-processing for common interconnection technologies	x				
4	4.2.	MS4.4	Export common interconnection technologies to specialized academic laboratories		x			
4	4.2.	MS4.5	Develop device-to-wafer interconnection techniques to support the multi project wafer (MPW) submissions			x		
4	4.3.	MS4.6	Develop wafer-to-wafer process in front-end to sensor connection		x			
4	4.3.	MS4.7	Develop the use of TSV to transfer power or data through sensors or front-end layers		x			
4	4.3.	MS4.8	Develop the interconnection capability for post-processed devices			x		
4	4.1	D4.1	Production of devices to test the radiation hardness of the interconnection			x		
4	4.1	D4.2	Production of devices to assert the reliability under specific thermal/mechanical conditions			x		
4	4.2	D4.3	Produce a demonstrator using a maskless technique for deposition in a bump-based interconnection technology		x			
4	4.2	D4.4	Demonstrate the capability of a non-industrial and non-RTO facility to provide interconnections based on an in-house method			x		
4	4.2	D4.5	Demonstrate the capability to connect individual dies from a MWP using a cost-affordable die-to-wafer technology			x		
4	4.3	D4.6	Demonstrate a cost and yield-affordable wafer-to-wafer interconnection process		x			
4	4.3	D4.6	Produce a sensitive device using interconnections to transfer power or data across tiers		x			

4	4.3	D4.7	Proof a cost-effective solution for post-process interconnection of dies			x		

Table 5: Work package 4: tasks, milestones, and deliverables.

2.5 The DRD3 proto-collaboration

The interest of the physics community in the DRD3 program has been evaluated via questionnaires.

Presently, the DRD3 proto-collaboration comprises 133 groups from 28 countries, for about 900 interested people (see Annex I, page 50). Figure 7 shows the geographical distribution of the DRD3 institutes: $\sim 70\%$ are from Europe, 15% from North America, 10% from Asia, 5% from South America.

2.6 Interlink with other DRDs

During the preparation of this document, the conveners of the DRD3 proposal had the opportunity to engage with the Executive board of the Solid State and Radiation Damage of the CPAD [3] initiative. One noteworthy point discussed was the status of the Solid State section, which is currently in the process of being organized in their collaboration. Consequently, we find ourselves in a situation where there is limited information available to be included in this document regarding the Solid State section.

Looking ahead, we are considering potential connections and collaborations with other DRDs.

DRD4 is interested on detectors with intrinsic charge multiplication or other fast-timing solid-state detectors, mainly SiPM, possible collaboration may arise from understanding mechanism to mitigate the radiation damage mechanism in the gain layers.

DRD5, which as part of their program also focuses on 2D materials, is presently in the nascent stages of defining and developing technology in this area. Consequently, the potential for collaboration with DRD5 is not clearly established yet. It's apparent that future discussions will be crucial to determine and create potential synergies between our collaboration and DRD5, setting the stage for productive partnerships in this advancing field.

A possible collaboration with the DRD6 may focus on interconnecting technologies used for calorimeters with silicon sensitive layers for the readout, such as silicon pixel high granularity calorimeters.

DRD7 shares several common topics with our collaboration. Sensor-frontend interconnections use technologies which are often inherited from electronics. As a general rule, a strategy has been discussed to mention these technologies in both DRDs but to keep as boundary the final goal of the application. If the developed devices are aimed to

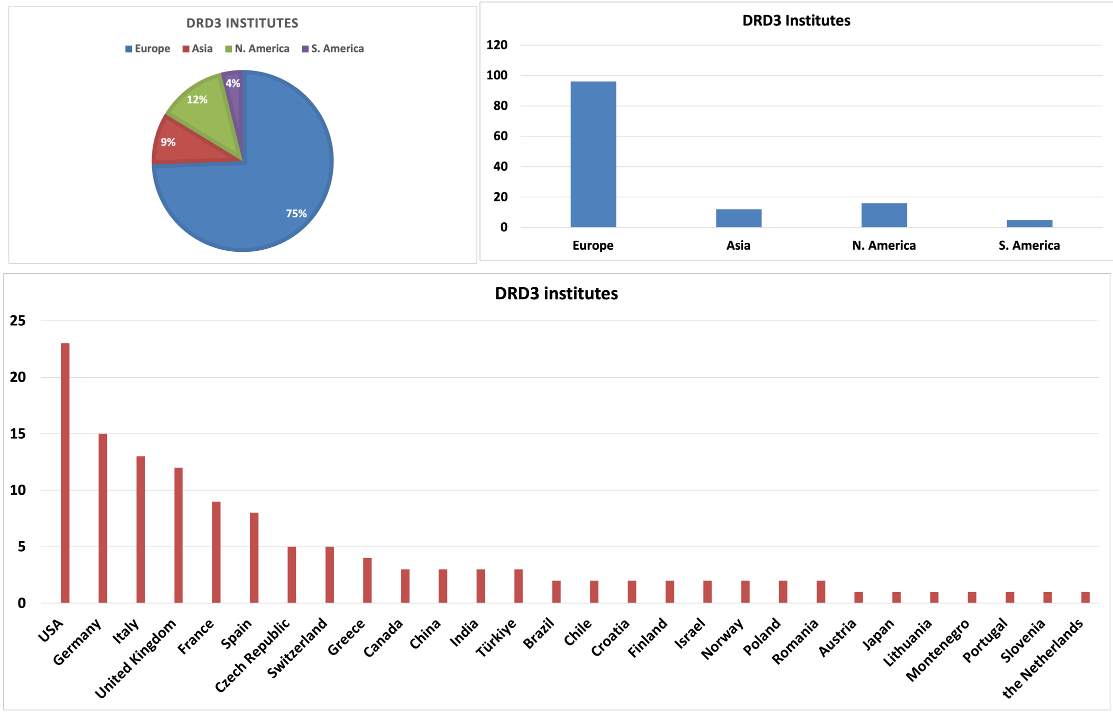

Figure 7: Top: Continent of origin of the DRD3 institutes. Bottom: number of DRD3 institutes per country

the development of sensors they will go to DRD3, while all developments more electronics oriented such as tier-to-tier interconnections for example are clearly more suitable to belong to DRD7. DRD3 will benefit from close collaboration with DRD7 especially for joint submissions, the development of complex readout architectures and the 3D integration of a sensitive CMOS chip with an independent digital chip.

3 WG1: Monolithic silicon sensors

WG1 aims to advance the performance of monolithic CMOS sensors for future tracking applications, tackling the challenges of very high spatial resolution, high data rate, and high radiation tolerance while maintaining low mass, covering very large areas, reducing power, and keeping an affordable cost. The combination of several and ultimately all of these challenges in one single sensor device is another very important aim of this WG, necessary to fulfill several strategic programs. WG1 will explore high-precision timing for applications such as Timing Layers and in full 4D tracking. It will also consider application in the electromagnetic section of a High Granularity Calorimeter. WG1 includes the design and experimental evaluation of fabricated sensors, and the development of suitable data acquisition systems. WG1 will benefit from synergies and common areas with other DRD3 WGs, and close collaboration with DRD7 for readout architectures and DRD8 for integration (DRD8 still to be formed).

3.1 WG1 Research Goals

The R&D program can be divided into three phases according to the timelines of the strategic programs: (i) the initial stepping stones developments of ALICE-3, LHCb-2, EIC, Belle-3, ATLAS, CMS, and HGCAL (DRD6); (ii) the subsequent further developments for e^+e^- colliders; (iii) and, lastly, the R&D for MC and FCC-hh. This proposal details the deliverables for the first R&D phase up to 2027 and highlights the R&D path from 2027 on. Several research goals (RG) and common areas (CA) are identified to be developed in available technology processes. The specification values below are expected to be significantly advanced or reached in at least one technology by the end of the first phase (<2027). The summary of the research goals is presented in Table 6.

WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

Table 6: WG1 research goals in the period 2024 - 2026

The list of common areas identified so far is the following:

- CA 1.1: Interconnection and data transfer;
- CA 1.2: Integration;

- CA 1.3: Non-silicon materials;
- CA 1.4: Simulation and characterisation.

The R&D deliverables are Multi-Project Wafer or shared Engineering Run submissions (MPW is used throughout this chapter to designate both) in different technologies and foundries as presented in Fig. 8. They cover four research goals to address the strategic program performance requirements outlined in the ECFA Detector R&D roadmap [1]. The MPW features and timeline are summarized in Fig. 8, while more details on the potential and complementarity of the various technologies are presented in the following sections. Once the DRD3 collaboration is formed, Work Package (WP) projects will be defined and the MPW details fine-tuned to ensure proper coverage of all the parameters. Developments in the common areas within DRD3 and with other DRDs will also be better defined. Particularly, this can concern developments of complex readout architectures and the first evaluation of the 3D integration of a sensitive CMOS chip with an independent digital chip in collaboration with DRD7.

3.2 Technology processes

The technology processes shortly introduced below complement one another in terms of features that are beneficial for the research goals of monolithic sensors in DRD3. All of the described technologies are accessible to the HEP community, usually through direct collaboration with institutes or through framework contracts with the foundries. The features available in these technologies are attractive for HEP detectors as their combination provides a complementary set of parameters to optimize the performance of future monolithic sensors:

- Wafer sizes of 200 mm and 300 mm;
- High resistivity bulk through high resistivity epitaxial and Czochralski substrates of p- and n-type;
- Processes with node sizes ranging from 65 nm to 180 nm and potential to optimize implant designs for charged particle detection (e.g. radiation hardness, timing resolution, etc.);
- Availability of MPWs and/or dedicated engineering runs with large reticles (in some cases, including options of reticle stitching or 3D stacking to logic wafers).

TPSCo 65 nm Developing the 65 nm technology to achieve the highest position precision in large-area sensors is an important goal. This technology uses an epitaxial layer, which is currently fixed at 10 μm. It features seven metal layers at this stage and the manufacturer offers engineering run submissions in 300 mm wafers. The stitching method to reproduce the reticle pattern (25 mm $\times$ 32 mm) can be used to allow large sensitive areas over a full wafer. Wafers can be thinned to much less than 50 μm. The small technology node allows the highest channel density achieved so far with pitches

DRD3 WG1 Monolithic silicon sensors		Assess technology performance for each RG - handle technical solution options for strategic programs of LS4 time scale				Toward 4D-tracking for future colliders
Research Goals	Timeline	2024	2025	2026	2027	≳ 28
	Technologies	Foundry submissions and Milestonses (MS)				
	TPSCo (TJ) 65 nm	design MPW1.1	submit MPW1.1 Q4-2025 (MLR2)	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q2-2027 (MLR3)	evaluate MPW1.2 (TJ 65 nm), design/submit/evaluate MPW1.3-1.n (all technologies) (possibly including in common submissions ER designs for dedicated experiments)
	TJ/AMS 180 nm, LFoundry 110/150 nm, IHP 130 nm	design MPW1.1 submit MPW1.1 Q4-2024	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q1-2026	evaluate MPW1.2	
RG1 Position precision	TPSCo (TJ) 65 nm	electrode size/shape/pitch, process variants 12" ER splits, thin epitaxial layer, stitching optimized for high channel density (low pitch)		MS1 establish position precision versus technology, channel configuration and readout mode MS2 establish time precision versus technology, channel configuration MS3 establish performance of readout variants for power consumption MS4 establish radiation tolerance, provide guidelines for choice of substrates select/merge MPW1.1 features add new technology features submit configurations for Vertex Detector, Central Tracking, Timing Layers, HGCAL	MS6 handle technical solutions for Vertex Detector (ALICE-3, LHCb-2, Belle-3, CMS/ATLAS) 1) high radiation tolerance/rate technlogies > 65 nm 2) high channel density, sitching TPSCo 65 nm MS7 handle technical solutions for Central Tracking (ALICE-3, EIC, LHCb-2, Belle-3), Timing Layers (ALICE-3, ATLAS, CMS) with stitching TPSCo 65 nm MS8 handle technical solutions for low power w/o and w/ precision timing, at medium and high rates	merge RGs and various technology achievements in selected technologies, extend all to stitching implement 3D integration consider finer nodes and new materials
	TJ/AMS 180 nm, LFoundry 110/150 nm, IHP 130 nm	electrode size/shape/pitch, wafer type/thickness, process variants 8" ER or MLM splits				
RG2 Timing precision	TPSCo (TJ) 65 nm	similar to RG1 optimized for fast signal collection speed and high S/N				
	TJ/AMS 180 nm, LFoundry 110/150 nm, IHP 130 nm	similar to RG1 optimized for fast signal collection speed and high S/N including gain layer option				
RG3 Readout architecture common with DRD7	TPSCo (TJ) 65 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium rates power distribution and control in large size stitched matrix				
	TJ/AMS 180 nm, LFoundry 110/150 nm, IHP 130 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium and high rates				
RG4 Radiation tolerance	TPSCo (TJ) 65 nm	process features in splits				
	TJ/AMS 180 nm, LFoundry 110/150 nm, IHP 130 nm	variants of substrates (Cz, epitaxial), resistivity, p-type and n-type				
RG5 Large-area CMOS	LFoundry 150 nm	include strip front-end		MS5 establish large-area versus technology, channel configuration	MS9 handle large-area technical solutions for Central Tracking in future collider experiments	
Common Areas	Interconnection & data transfer WG7/DRD7	3D integration demonstrator - TJ 180 (65) nm CIS (sensing) + 130 (65) nm CMOS (high rate/precision timing at high chan. density)				
	Integration & cooling WG7/DRD8	develop light mechanical designs and cooling, systems optimized to power consumption				
	Non-silicon materials WG6/DRD7	qualify radiation tolerance				
	Simulation & characterization WG4/WG5	develop dedicated monolithic CMOS tools				

Figure 8: WG1 research goals and technology developments planning

below 20 μm. Fully exploiting this high granularity potential will, however, need development of low-power readout coupled with a specific voltage distribution to cope with large active areas. The potential for a precise timing measurement will also be evaluated for the characteristic features of this technology. To further extend the ability to implement new functionalities and to increase the rate capability at high channel density, 3D stacking of the analog-sensitive component with a separate logic wafer will also be explored. Developments in the TPSCo 65 nm technology are recent and have been driven by the ALICE ITS3 project. A dedicated engineering run for ITS3 is foreseen in spring 2024. It will substantially advance the knowledge of the technology and also offer the possibility for few drop-in chiplets developed by experts having contributed to the first submissions. The first R&D phase proposed above will take advantage of the three Multi-Project Reticle (MPR) runs that are currently proposed by CERN to be shared with the community, with the first one in late 2025 (MPR2) and the subsequent other two spaced 18 months apart (MPR3 in spring 2027, MPR4 in late 2028). This is a reasonably fast turnaround cycle for testing and iterating a design in this technology. Note that there is CERN funding foreseen for a fraction of these MPR runs. These submissions will include the development of complex architectures, in collaboration with DRD7, that eventually could be ported to other technologies. Dedicated DRD3 engineering runs are possible, provided that DRD3 is able to fill the wafer and pay for it fully.

LFoundry 110 nm The LF11IS is an automotive-grade CMOS Image Sensor node offering a six aluminum layer (BEOL) stack. Access to fabrication is possible through regular MPW and Multi-Layer Mask (MLM) runs. The foundry allows for custom high-resistivity substrates on Front-Side Illuminated (FSI) and/or Back-Side Illuminated (BSI) process flows, including the possibility of using a dedicated maskset for backside lithography. While the maximum reticle size is 26 mm $\times$ 32 mm, the LF11IS technology has a stitching option. Based on this technology, sensors on active fully-depleted thicknesses ranging from 50 to 400 μm have been developed. The flexibility of the foundry process and product engineering teams allows exploring multiple wafer splits (n-epi thickness, n- or p-type starting substrate, substrate resistivity, implementation of a gain layer creating a monolithic LGAD, FSI or BSI process on different wafer thicknesses). In the framework of ARCADIA, INFN and LFoundry agreed on the terms to allow for the participation of third-party design groups to joint production runs. In this case, the third-party design group will be provided with regular access to the CMOS LF11IS iPDK (Interoperable Process Design Kit) for the implementation of proprietary architecture and sensor designs. Other than providing a library of signal samples for the chosen sensor geometry, INFN handles the sensor integration to the third-party design and final Design Rule Checking (DRC) of the design database during the preparation for the tapeout. This option enables a straightforward, low-risk, and very fast ramp-up of the R&D on sensors using LF11IS technology for new groups and design teams. This technology will develop 100 ps, 100 μm pixels (20-30 ps with additional gain layer). It will use n-epi active layer on p^+ substrate or high resistivity n-type substrate, thinned down to 100-400 μm.

IHP 130 nm The Silicon Germanium BiCMOS 130 nm process from IHP microelectronics combines state-of-the-art Heterojunction Bipolar Transistors (HBTs) performance and the advantages of a standard CMOS process. HBTs are ideal for high-performance timing applications thanks to their enhanced bandwidth and a better noise-power ratio than CMOS transistors. The process features a large n-well collection electrode that hosts the electronics. A nested p-well contains nMOS and PNP-HBT transistors. Isolation of the bulk of pMOS transistors from the collection n-well will be explored in future submissions. A small-scale demonstrator achieved a timing resolution of 20 ps at an analog power density of 2700 mW/cm^2 and 30 ps at 360 mW/cm^2. Preliminary radiation characterization shows good radiation tolerance. Sensors are implemented in high resistivity substrates up to 4 kΩ·cm and can be equipped with a Picosecond Avalanche Detector (PicoAD) gain layer for improved timing performance. The latest prototype with a 50 μm pixel pitch targets sub-10 ps timing resolution.

LFoundry 150 nm The LFoundry 150 nm process (LF15A) is a mixed digital/high-performance analog, high-voltage CMOS technology node. It features up to six layers of aluminum interconnection, with the possibility of an additional thick layer of top metal, particularly suited to efficiently route power lines to large pixel matrices. This process includes as well a deep p-well layer, which is useful for embedding digital logic inside the collecting electrode. The foundry offers standard and high-resistivity wafers, and has shown to be open to process modifications. There are typically two MPW shuttle runs organized per year. MLM engineering runs are also possible and can be particularly cost-effective for joint submissions handled by several teams. The LF15A technology has been successfully used in the past years for tracking based CMOS demonstrators (e.g. LF-CPIX, LF-MONOPIX chips, and RD50-MPW chips) and for non-amplified CMOS timing sensor concepts with performance better than 100 ps (CACTUS chips). Characterization of irradiated samples has shown the technology to be radiation tolerant up to dose levels suitable for the innermost layers of tracking detectors at the HL-LHC. The community is currently negotiating a framework agreement with this foundry to produce a certain number of submissions over a fixed period, taking advantage of special conditions and potentially lower production costs. This technology will develop fully depleted 50-250 μm thin sensors, with $<$25 μm pixels and use $>$2 kΩ·cm high resistivity substrates. It will also explore 30 ps/MIP timing with 250 μm pixels.

AMS/TSI 180 nm The AMS-Osram AG 180 nm and TSI Semiconductors 180 nm are high-voltage CMOS technologies. TSI discontinued its high-voltage CMOS technology in 2023, and efforts focus now on the AMS technology. The TSI process is layout compatible with the aH18 process of AMS. As part of their standard layer stack, both processes have a deep n-well, typically used to host low-voltage readout electronics while isolating them from the high-voltage substrate. They also have a deep p-well that integrates digital readout electronics within the deep n-well. They feature a total of seven (TSI)/six (AMS) metal layers. TCAD models are available. Fabrication on high-resistivity substrates is possible, and the foundry can manufacture designs on wafers provided by the customer. Stitching is possible too. The maximum reticle size is 2.1 cm $\times$ 2.3 cm. High-voltage CMOS sensors in this technologies have demonstrated a time resolution of 2.4 ns at low noise rates and shown an excellent performance concerning efficiency and noise even after irradiation with protons and neutrons with fluence up to 2×10^{15} n_{eq}/cm^2. The smallest pixel pitch demonstrated so far is 25 μm. Design submissions are engineering runs, although wafer sharing is possible. AMS 180 nm is the technology for the pixel tracker of the Mu3e experiment (MuPix), and LHCb is considering it for the proposed Mighty Tracker upgrade (MightyPix). Sensors in this technology have been thinned down to 50 and 70 μm, and demonstrated to work efficiently in the framework of the Mu3e experiment (50 μm for the vertex layers, and 70 μm for the outer tracker layers). This technology has been used to develop prototypes and final sensors for several other particle physics applications (e.g. CLICpix, ATLASpix), for test beam instrumentation (e.g. TelePix), and for applications in space (e.g. AstroPix).

TowerJazz 180 nm The Tower Semiconductor 180 nm CMOS imaging process is well-established in the HEP community. It provides cost-effective manufacturing and prototyping on 200 mm wafers. It features six metal layers plus the possibility for a final thick metal layer that can be used to facilitate signal and power distribution. The process includes deep p-wells to allow full CMOS functionality to embed digital and analog electronics side-by-side in the pixel. The foundry offers to produce on foundry-supplied and customer-supplied (after approval) wafer stock. Sensors have been successfully produced on epitaxial (up to 30 μm thickness) and high-resistivity Czochralski substrates, with a typical device thickness of 100 μm although the community has experience also with 50 μm and 300 μm devices. Through close collaboration with the foundry, the implantation profiles can be optimized for specific sensor needs, which has been done successfully to achieve high radiation hardness. The possibility to combine different implants in the pixel and optimize implantation profiles together with Tower engineers will be an essential means to develop optimized sensors for radiation hardness and timing capabilities. Prototyping takes advantage of regularly offered MPWs (up to four yearly shuttle runs). Also, MPW runs allow process modifications in individual layers related to charge collection. This process has been successfully used recently for a large family of small-electrode monolithic CMOS sensors ranging from ALPIDE and MIMOSIS sensors to radiation hard sensors like TJMonoPix and MALTA. With a reticle size of 30 mm $\times$ 25 mm, it provides sufficient space to prototype multiple sensors in a single engineering run for maximum processing flexibility and cost-effective prototyping.

Low-cost large-area CMOS sensors This refers to large-area monolithic CMOS sensors aimed at instrumenting hundreds of m^2 in central tracking applications in future collider experiments, such as e^+e^- colliders or beyond, where cost per unit area is the key issue rather than achieving the highest position precision or the highest radiation tolerance. These sensors do not need to be passive, and this R&D is moving towards a monolithic strip or large/elongated pixel with integrated front-end readout approach. Arguments for choosing strips over pixels rely on lower power consumption and simplified readout. Additionally, the strip geometry allows for either increasing the complexity and thus functionality or timing resolution of the electronics, or to distribute the power across larger areas thus making cooling more efficient. This R&D will use the LFoundry 150 nm process (LF15A) with p-type floatzone wafers without stitching initially, and might explore alternative processes and/or stitching at a later stage. The next submission is foreseen as an MPW run in early 2024, with the goal to include a strip front-end or at least elements of that. This will be followed by another MPW submission, tentatively in early 2026. This R&D has strong links with WG2.

3D stacking option Recently Tower Semiconductor and its European representative company Etesian have advertised the possibility of using waferstacking of the 180 nm CMOS Image Sensors (CIS) to its 130 nm mixed signal CMOS. The foundry performs the stacking, and it is offered to customers through a PDK. The 3D stacked 180 nm CIS + 130 nm CMOS is also accessible through regular MPWs organized by the foundry. This 3D stacked technology promises the potential for HEP sensors as 3D-stacked monolithic sensors with an optimized sensor layer and a 130 nm signal processing layer for more complex logic as required for high-rate and timing applications. The radiation tolerance is expected to be the same as that of the individual processes. This technology will develop 3D stacking, timing through different geometries with/without internal gain, and on-sensor time-stamping. It will use different resistivity substrates to expand to high radiation tolerance. Knowledge obtained in a medium node size (180 nm, 130 nm) provides cost-effective information on 3D integration that can be transferred to the 65 nm 3D stacked CIS + CMOS also offered by Tower.

3.3 Structuring projects

Developing monolithic sensors requires to gather simultaneously expertise on both sensing elements and microelectronics, calling for a strong organisation. Hence, it is critical that the research work will be structured early around Work Package projects proposed by groups of institutes interested in specific questions within the DRD3 research goals (RG). Projects will investigate RG by designing, manufacturing and measuring prototype sensors of different scale depending on the maturity of their development state, and developing the dedicated data acquisition systems as needed. The sensor prototype shall be produced in one or more CMOS technologies described above. It is proposed to implement projects along deliverables and milestones defined by the research groups in their proposal and guided by indications given in Fig. 8. A common methodology for this investigation is an iterative cycle:

a) design and simulation of the sensor,

b) submission of the designs as MPW,

c) development of the specific data acquisition system (e.g. chip carrier board, firmware, etc.),

d) characterization in lab measurements irradiations, beam tests as appropriate.

Institutes participating to projects can contribute to one or several of these phases. Is is important that the full set of expertise is present within the project, not only sensor design but also test. In order to efficiently use submissions groups are encouraged to share MPWs within DRD3, possibly in collaboration with DRD7, or to submit engineering runs.

The project definition will shortly follow the forming of the collaboration and will be based on proposals submitted by groups of research institutions. Proposals will follow a provided template which addresses:

- research goals related to DRD3,
- consortium of groups participating and their envisaged work sharing,
- implementation plan following deliverables and milestones defined in the project plan,
- submission plan and resource planning.

Along the DRD3 RG and milestones indicated in Fig. 8 the submitted proposals are expected to address a large variety of research goals for monolithic sensors. A non-exhaustive list of some examples is given below.

- Thin high granularity CMOS sensors addressing specifications, including hit rates and power dissipation, to ee-experiment's vertex detectors and trackers.
- Radiation hard CMOS sensors investigating variations of e.g. substrate choices, pixel designs and post-processing.
- Sensors with internal gain to provide high SNR, improved timing, improved radiation hardness and/or simplified FE-circuits for fine-pitch pixel detectors.
- Different novel readout architectures for pixel matrices to investigate optimal on-sensor signal transmission, data handling and compression.

4 WG2: Hybrid silicon sensors

WG2 aims to advance the performance of sensors for 4D tracking, and it is aligned with the goals of DRDT2. The scope of WG2 is quite broad, as it addresses the R&D of sensors for very different environments: vertex or tracker, low/high radiation, low/high occupancy, low/high power, and low/high material budget. Presently, sensors with 4D capabilities are foreseen in many systems, from Time-of-Flight systems with only 1-2 layers of sensors with the best possible resolution to large 4D trackers with many layers. In this latter case, if the temporal resolution is good enough, recognition algorithms can use four coordinates in the reconstruction, simplifying the pattern recognition. Broadly speaking, the challenges at hadron colliders are mostly linked to radiation levels (mainly in the vertex detector) and high occupancy. In contrast, at lepton colliders, the challenges are related to material budget and low power consumption.

It is noted that the various developments comprise studies on the sensor production techniques including e.g. passive CMOS sensor technologies.

4.1 Spatial and temporal resolutions at extreme radiation levels

For this R&D, the new innermost layers of ATLAS/CMS and the LHCb velo pixel systems are used as stepping stones for the formidable developments needed for FCC-hh. Due to their short drift path and low depletion voltage, 3D sensors are strong candidates for these upgrades.

- **RG 2.1 Reduction of pixel cell size for 3D sensors.**
  - 2024-2025: 3D sensors test structures with pixel size smaller than the current $50 \times 50\ \mu m^2$ or $25 \times 100\ \mu m^2$
  - 2026-2028: Large size 3D sensors with reduced pixel size.
  - $\geq$ 2028: Expand the number of foundries capable of producing 3D sensors for HEP applications.
- **RG 2.2: 3D sensors with a temporal resolution better than 50 ps.**
  - 2024-2025: Production of a small matrix with pitch equal to or less than $55 \times 55\ \mu m^2$ to be connected with existing read-out ASICS
  - 2026-2028: Production of large-size sensors (using the selected geometry from the R&D runs) and interconnection with custom-made read-out ASIC

4.2 Spatial and temporal resolutions at low radiation levels and low material and power budgets

Future upgrades beyond LHC phase-II might seek to introduce 4D layers at moderate radiation levels (1 - 3 $\cdot 10^{15}$ n_{eq}/cm^2), with a spatial resolution of about 10 - 30 μm. Sensors for lepton colliders as well as lepton-hadron colliders require a very low material budget and minimal power consumption. Presently, sensors with moderate values of internal gain, the so-called Low-Gain Avalance Diodes (LGAD), are the most promising candidates. In fact, low gain allows for an increased signal size while keeping the noise almost constant, an important feature in timing applications. Low gain is also important for applications that require a low material budget as the sensor can be very thin, and the power of the electronics can be reduced since the "first amplification stage" is contained in the sensor itself. The broad LGAD technology includes several specific and different designs, e.g. Trench-Isolated LGAD (TI-LGAD), Inverted LGAD (iLGAD), AC-coupled LGAD, also known as Resistive Silicon Detectors (AC-LGAD/RSD), Deep-Junction LGAD (DJ-LGAD), and can be employed also in MAPS designs.

- **RG 2.3: LGAD Sensors with very high fill factor, and an excellent spatial and temporal resolution.**
  - 2024-2025: LGAD test structures of different technologies (TI-LGAD, iLGAD, AC-LGAD/RSD, DJ-LGAD), matching existing read-out ASICs.
  - 2026-2028: Large LGAD sensors based on the best-performing technology.
  - 2025-2028: Investigation of radiation hardness of LGAD technology beyond $\sim 2.5 \cdot 10^{15}$ n_{eq}/cm^2.
- **RG 2.4: LGAD sensors for Time-of-Flight applications**
  - 2024-2026: Production of LGAD sensors with large size for Tracking/Time-of-Flight applications to demonstrate yield and doping homogeneity. Study of spatial and temporal resolutions as a function of the pixel size.
  - 2026-2028: LGAD structures with 4D capabilities produced with vendors capable of large-area productions to demonstrate the industrialization of the process.

4.3 WG2 Research Goals

Table 7 list the WG2 research goals.

WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing ($\leq 55 \times 55$ μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6" and 8"
RG 2.4	LGAD for ToF (Large area, < 30 μm, < 30 ps)

Table 7: WG2 research goals in the period 2024 - 2026

5 WG3: Radiation damage characterization and sensor operation at extreme fluences

This WG aims to provide a fundamental scientific understanding of radiation damage processes in solid-state detectors and detector materials at low, high, and extreme radiation levels of up to $5 \cdot 10^{18}$ n_{eq}/cm^2 and 5000 MGy, as anticipated for the forward calorimeters in the FCC-hh after an integrated luminosity of 30 ab^{-1}. The existing and newly generated knowledge will be used to optimize the radiation tolerance of the various detector types under development within the collaboration through defect and material engineering, device engineering, and optimization of operational conditions. The work is organized in two areas. The first is the study of the radiation damage mechanisms in detector materials, including the formation of microscopic defects and their impact on device performance; the second is the study and modeling of radiation damage in devices. In both areas, the full range from very low to high fluences and finally up to extreme fluences beyond $2 \cdot 10^{16}$ n_{eq}/cm^2 has to be covered. The latter work covers the Roadmap DRDT 3.3. on extreme fluence operation, while WG3 reaches deeply into all four Roadmap DRDTs for solid-state detectors wherever radiation damage is of concern.

5.1 Radiation damage and hardening studies at material level

Understanding radiation damage at the microscopic level and the consequences on materials and device properties is a necessary prerequisite for efficient and successful detector development. Comprehensive investigations of defects generated in irradiated sensors providing accurate evaluations of defect concentrations and trapping parameters can be achieved by employing specific spectroscopic techniques based on capacitance or current measurements (e.g. DLTS, TSC, TSCap). Such methods have been successfully applied on fabricated silicon sensors up to fluences of about 10^{15} n_{eq}/cm^2. They provide both the characteristics of radiation-induced defects that are also fundamental input parameters to sensor performance simulations under various conditions and knowledge for developing material and defect engineering strategies. As the extrapolation of damage parameters to higher fluences has proven to be too pessimistic, and the defect formation process is not a linear function of fluence, further characterization work at higher fluences is essential but exceeds the range of applicability of present experimental characterization methods. Therefore, the understanding of the radiation damage at extreme fluences requires, in addition, comprehensive modeling of defect generation, including the higher order radiation-induced defects, and the employment of other techniques suitable for detecting defects in large concentrations, i.e., above 10^{16} cm^{-3}, such as EPR, FTIR, XRD, Raman, and PL. Even more demanding is the understanding of radiation damage in wide band gap (WBG) and other materials where presently, compared with silicon, significantly less knowledge exists. In addition, the changes of the fundamental semiconductor properties (e.g., carrier mobilities, carrier lifetime) at extreme fluences are very poorly known, although they are needed for any detector design work. These challenges will be addressed in the years to come, starting with developing the defect-engineered strategies for obtaining detailed and precise electrical characterization of point and cluster defects generated by irradiations up to fluences of 10^{16} n_{eq}/cm^2 by means of DLTS, TSC, and TSCap techniques. Highly irradiated devices (above 10^{17} n_{eq}/cm^2) will start to be investigated by EPR, FTIR, XRD, Raman and PL, to provide the needed information about the chemical structure of radiation-induced defects and their introduction rates, to be used in developing a realistic radiation model up to extreme radiation fluences. The change in the carrier lifetime and mobility will be evaluated from carrier lifetime and Hall effect measurements.

5.2 Radiation damage and hardening studies at device and system levels

The detector community will need a wide variety of radiation damage studies in the near and long term. Tracking and timing detectors, including, for example, several configurations of LGAD and 3D sensors, are already aimed at the earliest LHC upgrades. These will continue to need regular irradiations with various particle species up to approximately $5 \cdot 10^{16}$ n_{eq}/cm^2. Technology development in new directions will also need radiation testing and radiation damage modeling; this includes large area and thin silicon devices, applications for the LHCb and ALICE upgrades, the Electron-Ion Collider, and space-based detectors. New efforts in high-granularity calorimetry and quantum-imaging detectors are already seeking characterization within radiation contexts. Devices proposed for later upgrades need radiation damage studies in the near term too, for evaluation of monolithic CMOS and ASICs. Within the community, there are already calls for facilities able to provide up to $1 \cdot 10^{18}$ n_{eq}/cm^2, with multiple beam energies and species. TCAD and GEANT4 simulations are underway for new structures and require validation with data. Data are urgently needed from TCT instruments and testbeams, combined with dedicated data collected by the LHC experiments for leakage current and depletion.

New sensor materials are under exploration, requiring either new or extended parameterized models of their radiation damage response. These include all materials studied in WG6, particularly the wide bandgap semiconductors, which may benefit from reduced cooling requirements. Radiation studies are also needed for new vertical and heterogeneous integration techniques directly connected to materials improvements. The foundational research toward understanding how fundamental material properties, such as mobility, effective dopant concentrations, and carrier lifetimes, must also continue and reach a more solid standing. The semiconductor detector community needs to understand the validity limit of the current models (e.g., Hamburg Model) and where the presently used non-ionizing energy loss (NIEL) hypothesis fails to determine the best directions in defect and device engineering.

We do not lose sight of the fact that technology transfer beyond High Energy Physics, for example, medical imaging, dosimetry, nuclear safety, and security, requires rigorous radiation validation.

The present community for developing radiation-tolerant semiconductor detectors includes many institutes comprising university groups and national laboratories. Regular training is being offered at nearly all of them to expand the community and develop expert junior researchers. Milestones to be achieved in the next three years include (i) improved or new models for new materials and extreme radiation conditions; (ii) a transfer of information from models to simulations; and (iii) sufficient irradiation facilities and test beam support for this diverse program. Critical infrastructures on the timescale of six years are the reliable availability of facilities providing integrated fluence on the order of 10^{18} n_{eq}/cm^2, in both charged and neutral species.

5.3 WG3 Research Goals

The research goals of WG3 are summarized in Table 8.

WG3 research goals <2027	
	Description
RG 3.1	Start of building up data sets on radiation-induced defect formation in WBG materials
RG 3.2	Continue developing silicon radiation damage models based on measured point and cluster defects
RG 3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation
RG 3.4	Expand the measurements and models of silicon and WBG sensors properties in the fluence range 10^{16} to $1 \cdot 10^{18}$ n_{eq}/cm^2

Table 8: WG3 research goals in the period 2024 - 2026

6 WG4: Simulation

The simulation work will be dedicated to the development of common simulation packages, tools, and radiation models. There will be two lines of activities that will be pursued: TCAD tools and so-called Monte-Carlo (MC) tools. While the former is commonly used in sensor design, process simulation, and radiation damage modeling the latter are extensively tested in sensor performance evaluation (with particle and Transient Current technique) benefiting from much faster code and integration of other software packages e.g. GEANT4.

Another important activity in WG4 will be the continuation of radiation hardness modeling, bulk, and surface, starting from the defect level using mainly TCAD, but also MC tools. Radiation hardness models for WBS will be explored and developed.

The WG4 will be an important part of many working group and work packages: it will contribute to the simulations of sensor development and performance in WG1 and WG2, it will collaborate with WG3 to incorporate in the simulation the latest understanding of radiation damage, it will be used to optimize the developments of common tools (WG5), and will facilitate the use of WBS (WG6) by incorporating their properties in the simulation package.

6.1 Activities

The following activities are foreseen in the WG4

- TCAD activities will focus on providing verification of tools (mainly Silvaco and Synopsys, but also looking to other tools emerging) implementation of new physics models (impact ionization, mobility parametrization etc.), exporting tools, communication with software companies (e.g. implementation of WGs) and keeping the implementation of common solutions to device simulations.

- TCAD simulations will be complemented with charge transport simulation tools - Monte Carlo tools - allowing detailed studies of complex sensor performance. Different tools have been developed so far, but currently, the most supported and advanced tools are Allpix Squared and Garfield++, which will form the main/production framework, while other tools will continue to be used as verification and development tools. It is foreseen that improvements in MC simulations will eventually be integrated into AllPix2 and Garfield++. One obstacle for Monte-Carlo tools is currently the lack of implementing adaptive/time-dependent weighting and electric fields in induced current simulations.

- Modeling of the radiation damage in simulations has been evolving over the last two decades, but there is not a general model that, starting from the defect levels, comprehensively describes all the macroscopic properties of silicon, especially at extreme fluences (WG3). This is why it is important to define a common framework for process simulation, aimed at evaluating the impact of such model on innovative devices, technologies or materials.

- Development of signal processing tools that can be used with MC and TCAD tools and general digitization models for different sensors technologies.
- Owing to the emerging technology requirements of near future high-energy physics experiments, the present WG has to adopt long-term strategies to promote/initiate discussion with designers of future experiments, involved in the development of new detector concepts, to create a link between current expertise and next requirements.
- Last important item is – since the interdisciplinary nature of simulation – the establishment of a cooperation framework among the different WGs and WPs, as well as with other synergistic DRD collaborations.

6.2 WG4 Research Goals

The research goals of WG4 are summarized in Table 9.

WG4 research goals <2027	
	Description
RG 4.1	Flexible CMOS simulation adaptable to different technology nodes and development of connections between tools for device-level simulation and electronic circuit design/validation
RG 4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools
RG 4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.
RG 4.4	Developing of bulk and surface model for $10^{16}\text{cm}^{-2} < \Phi_{eq} < 10^{17}\ \text{cm}^{-2}$
RG 4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields

Table 9: WG4 research goals in the period 2024 - 2026

7 WG5: characterisation techniques, facilities

WG5 involves the establishment of a community-driven working group that focuses on the development, improvement, and dissemination of methods and techniques for characterizing sensors. By bringing together experts and leveraging collective resources, the working group aims to foster collaboration, knowledge sharing, and innovation in the field of sensor characterization within the particle physics community.

This working group operates across different Detector R&D Themes (DRDT) along three activity lines:

- Actively engage in the development, improvement, and diffusion of cutting-edge methods and techniques for sensor characterization. This involves exploring novel approaches and refining existing methodologies to assess and understand the performance and behaviour of sensors.
- The working group facilitates sharing of knowledge, resources, and expertise among participating researchers and institutions by identifying common infrastructures for sensor testing and fostering joint research activities. These collaborative endeavours aim to develop and deliver state-of-the-art infrastructures, such as the Caribou data acquisition system, specifically designed for the comprehensive testing and evaluation of sensors.
- Promoting the use of unique characterization facilities. These facilities may possess rare capabilities, specialized equipment, or specific expertise in sensor characterization. The project seeks to raise awareness and encourage researchers to leverage these facilities to explore advanced characterization methods. The project aims to foster collaboration between researchers and these facilities, facilitating access to specialized resources.

7.1 Working group implementation

The working group implements two types of activities to fulfill its objectives. Firstly, there are joint research activities that involve the creation or improvement of new testing methods or testing infrastructures. These activities will be typically structured as common projects with specific research goals. Typical examples of such activities are developments of techniques like Two photon absorption Transient Current Technique (TPA-TCT) or defect spectroscopy methods.

Secondly, the working group engages in networking activities aimed at coordinating access to unique testing infrastructures. These infrastructures may include high-energy or high-intensity beams, micro-beam TRIBIC facilities, and EMC assessment laboratories, irradiation facilities among others. The focus of these activities is to increase awareness among researchers about the availability of these facilities for sensor characterization. Additionally, the working group organizes dedicated workshops to provide training on different sensor characterization techniques. These workshops serve to educate researchers on the use of new and existing characterization methods and will be organized with the help of WG8.

7.2 WG5 Research Goals

The research goals of WG5 are summarized in Table 10.

WG5 research goals <2027	
	Description
RG 5.1	Extension of the TPA-TCT to wide-band semiconductor characterization (SiC and diamond)
RG 5.2	Upgrade Caribou DAQ hardware, firmware and software to advanced Ultrascale+ FPGA platform
RG 5.3	Efficient exploitation of common infrastructure (such as TPA-TCT, test beams, EMC facilities or Caribou): Promoting awareness within the community during the DRD3 workshops, dedicated showcase of use and subsidizing access fees or providing grants for specific projects
RG 5.4	Organizing mini-workshops for training on the use of characterization techniques and DAQ tools

Table 10: WG5 research goals in the period 2024 - 2026

8 WG6: Wide bandgap and innovative sensor materials

Wide band-gap (WBG) semiconductors have some attractive properties and also some associated problems. Whilst a wide bandgap reduces the leakage current, maintaining low noise levels even at high temperatures, it also increases the electron-hole generation energy. This increase implies that the number of electron-hole pairs generated for the same deposited energy is lower in WBG materials.

However, the substantial reduction of the noise level ensures that the overall signal-to-noise ratio (SNR) for WBG-based detectors is high enough, even after irradiation. In addition, the high breakdown field allows operation at high internal electric fields, minimizing the carrier transit time and the trapping probability. Tolerance to larger operating temperatures can also significantly simplify the system design.

Although innovative semiconductors, such as 2D materials, require investigation the current level of their development for particle physics use is still relatively low. As a result, a Blue-sky funding scheme should be applied to support further research in these areas.

WG6 is well aligned with the DRDT3.2 and DRDT3.3 since some WBG semiconductors can be used for timing applications due to the high carrier saturation velocity, and their potential radiation hardness can make them suitable material for use at extreme fluences particularly when taking all aspects of opeartion (cooling, leakage) into account.

8.1 Diamond

The high energy physics community has extensively studied diamond as a wide band-gap semiconductor material for sensors since many years; experiments, and accelerators have used diamond-based beam conditions monitors successfully for decades. A poly-crystalline synthetic diamond (pCVDD) with a wafer charge-collection-distance (CCD) of 400 microns is available today, and the aim is to increase the CCD to 500 microns and improve its uniformity accross the wafer. Diamond detectors have been extensively tested for radiation hardness and were found to be limited by charge trapping with mean free path of only 16 microns after 10^{17} cm^{-2} 24 GeV protons which results in insufficient charge (few 100 e) for successful operation.

3D diamond detectors with a femtosecond laser process to convert diamonds into graphite electrodes can address this problem. The first 3D diamond detector device is planned for use in the ATLAS Phase-II upgrade as a small beam condition monitor, and it represents a stepping stone towards larger area applications needed for future projects like the FCC-hh. Further studies and innovative geometries are needed to comprehensively assess 3D diamond detectors' radiation tolerance. This includes studies of charge multiplication via impact ionization through adapted electrode geometries to improve radiation tolerance and timing performance.

8.2 Wide-band semiconductor

SiC has found a widespread use in power devices recently. The quality of this material has reached levels comparable to that of silicon. Additionally, 150 mm SiC wafers have become standard in the semiconductor industry, and soon 200 mm wafers will be introduced to the market. The high-quality material required for SiC sensors is typically epitaxially grown using Chemical Vapour Deposition (CVD), which allows for precise control of crystal film thickness, doping, and homogeneity. Recently, SiC epitaxial layers up to a thickness of 200 μm have been obtained. However, the material's resistivity must be increased to deplete these layers with reasonable bias voltages. Alternatively, MIP detection in thin layers with reasonable SNR would need signal amplification in the material.

In the coming years, the main technological challenges for SiC detectors will involve studying the radiation hardness of high-quality materials and understanding the radiation induced defect formation. This will facilitate fabrication of more radiation-hard materials and provide reliable simulation tools necessary for designing new detectors and predicting their performance in extreme fluence environments. Recent studies have shown that SiC detectors have better timing performance than silicon detectors, necessitating further research to explore the possibility of including a gain layer into the bulk as done for the standard LGAD. A multiplication mechanism in SiC diodes has been observed after neutron irradiation, but it is not yet understood.
In the mid-term, SiC could be used as beam loss and intensity monitors, as well as in medical applications like (micro-) dosimetry and neutron/plasma detection in high-temperature environments.

GaN is the most rapidly growing semiconductor material used in industrial applications such as telecommunications, power management, high-temperature operation, opto-electronics, and aerospace. However, defects in the GaN crystal, such as dislocations and unintentional doping, still present a challenge in terms of device-level performance. In the past decade and due to the rapid improvement of material quality of epitaxially grown films, the promise of GaN as a detector material has been demonstrated by several groups. Nevertheless, the widespread use of GaN devices in higher radiation environments (HL-LHC and beyond) will require development to improve their radiation hardness. That in turn requires a thorough understanding of the displacement damage and resulting material defects in GaN. The realiable predictive models calibrated to irradiated GaN sensors on both native substrates and SiC should be used in device design. This aligns well with developments in the industry where material quality is perceived as the key to the development of fast RF devices with sub-ns resolution (5G and beyond) and monolithic designs of GaN embedded in Si or SiC substrates for fast power switching and nuclear technology applications.

8.3 WG6 Research Goals

The research goals of WG6 are summarized in Table 11.

WG6 research goals <2027	
	Description
RG 6.1	Development of small cell 3D diamond detectors (cages / interconnects, base length 25 μm) and possible exploitation of impact ionization
RG 6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.
RG 6.3	Improve tracking and timing capabilities of WBG materials
RG 6.4	Apply graphene and/or other 2D materials in radiation detectors, understand signal formation.

Table 11: WG6 research goals in the period 2024 - 2026

9 WG7: Interconnect and device fabrication

Interconnections are one of the critical aspects of future detector and electronics evolution. They have a fundamental role for integrating the sensor and readout ASICs, and in constructing multi-tier electronics. Interconnection technologies enter at different stages of detector construction: from the fast hybridization necessary for the qualification of prototypes to the reliable flip-chip of modules and they need to assure reliable operation for years under stringent radiation, thermal and mechanical specifications. Special interconnections are also key to resolving specific problems, for example in terms of pitch or mechanical/electrical properties.

The goal of the DRD3 interconnection task is to organize the different technological readiness levels of interconnection solutions and the effort towards future advances in the field to match the requirements of future detectors in a coherent and coordinated way.

During the preparation phase, some groups expressed interest in Mechanics and Advanced Cooling R&D. This work will be conducted in the framework of DRD 8. For reference, the groups are listed in in the Mapping Tables 18.

9.1 Maskless interconnections: anisotropic conductive films or pastes (ACF, ACP)

Small-pitch hybrid pixel detectors produced with solder bump-bonding techniques are widely used in current and future HEP experiments. The cost of the complex metallization and interconnect processing, performed in highly specialized foundries, dominates the production cost per unit area, and the need to process whole readout wafers dominates the prototyping costs. In addition, this introduces a long turnaround time during the prototyping phase, where several submissions are made, and usually, a limited number of devices are used for the test. The DRD3 interconnection working package studies technological alternatives to the standard flip-chip techniques to develop fast, possibly in-house, connection processes able to be used for fast testing of new productions and possibly at the device level. The advantage of avoiding specialized hybridization vendors translates into significant savings of time and money.

Interconnection of large-pitch ($\mathcal{O}(1\text{ mm})$) hybrid pixel detectors is also very important, for example in large-area timing detectors. The solder bump-bonding technologies used in small-pitch interconnection are an overkill in this case, driving the cost and complexity. Large-pitch interconnects are also required for the integration of detectors into functional low-mass modules, using a chip-to-flex flip-chip approach. The development of a fast, cheap and reliable interconnection process can therefore be very beneficial for these large-pitch hybridisation and module-integration applications.

Anisotropic Conductive Films (ACF) and Anisotropic Conductive Pastes (ACP) are interconnection technologies based on microscopic conductive particles suspended in an adhesive medium, a film, or a paste. Thermocompression of the ACF/ACP between two conductors results in a permanent attachment and a reliable electrical connection only in the direction of the compression. ACF is the dominating interconnect technology for displays (LCD and OLED) and is widely used also in e.g. camera modules and RFID manufacturing. For the application of HEP pixel detectors, critical parameters such as bonding force, adhesive film thickness, particle material, diameter, and density of particles need to be developed for the specific layout and topology of the respective sensors and readout ASICs. One of the main advantages of these technologies is that they may not require lithographic masks for deposition, are affordable, and can be performed in-house by many laboratories. Processing can happen both at die-to-die and die-to-wafer levels.

Additional advanced interconnect technologies such as nano-wires, gold-stud bonding and additive micro-structured ink-jet printing will be investigated for specific applications as possible alternatives to conductive adhesives. This study needs to be complemented with an investigation of the radiation resistance of these new technologies.

Relevant short-term (3 years) research goals in this development are (i) consolidate the connection yield necessary for tracking detectors applications; (ii) demonstrate a process optimization that could satisfy pixel pitch of the order of $30\mu m$ or below. In the mid-term (3-6 years), the main research goals are to test and verify (i) the radiation hardness of the process to fluences and doses typical of future experiments at colliders and (ii) the reliability of the technology under the thermal and mechanical specifications determined by the above applications.

9.2 Improvement and diffusion of classical interconnection technologies

Classical interconnection techniques provided to High Energy Physics Experiments by commercial vendors and RTOs are nowadays reaching the necessary standards in terms of yields and typical technical specifications but remain expensive and time-consuming processes. The construction of the LHC upgraded trackers for High Luminosity coming in parallel for several detectors on the same timescale also showed that the production capacity of most of these vendors can be easily saturated. Progress can be achieved following two directions. The first is to make the most common interconnection techniques affordable to existing infrastructure in home laboratories. This can be achieved, for instance, with the introduction of maskless processes. The second is to organize and sponsor the development of advanced processes and the cooperation of commercial vendors and academic groups to address specific complex issues: for example, the need for smaller pixel pitches, the resolution of process temperature constraints, the electrical properties of interconnections in terms of maximum current or capacitance, or the technique used by industry in the interconnection (die-to-die or die-to-wafer).

In the short-term, research goals are the development of maskless post-processing for some of the most standard technologies. In the mid-term, (i) the most standard technologies should be available in full or in part inside specialized academic laboratories and (ii) a device-to-wafer approach to favour the multi project wafer (MPW) submissions, where only a small part of each production wafer is used by a collaboration.

9.3 3D and vertical integration for High Energy Physics silicon detectors

3D and vertical integration are technologies already largely used in electronics. They are available via industry, and in this way, they profit from the commercial drive coming from consumer electronics. The use in High Energy Physics experiments has already been probed to some extent to merge - for instance - tiers in different technologies. A typical example is a digital layer connected to an analog tier built in a different process. Vertical integration might also have a fundamental role in the integration of different devices which need to be interconnected and that in today's detectors are exchanging data via external solutions such as flexible circuits. The vertical stacking can also allow to contact / power / read a lower tier through an intermediate one with the use, for instance, of specific vias. The interconnection Work Package of DRD3 should coordinate the access to specific industrial processes for laboratories involved in High Energy Physics detectors. While single groups might still be able to deal with secondary industrial actors in the field of vertical integration, the mediation of DRD3 will have a larger chance of success for the involvement of big industrial players, granting continuity and resources. Research goals for the short-term are (i) the demonstration of wafer-to-wafer process in front-end to sensor connection; (ii) the demonstration of the use of TSV to pass power or data through sensors or front-end layers. For the mid- and long-term, the goal is to demonstrate the interconnection capability for post-processed devices.

9.4 WG7 Research Goals

WG7 research goals <2027	
	Description
RG 7.1	Yield consolidation for fast interconnections
RG 7.2	Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to $< 30\mu m$)
RG 7.3	Development of maskless post-processing for classical bump-like interconnection technologies
RG 7.4	Development of wafer-to-wafer in presently advanced interconnection technologies
RG 7.5	Development of VIAS in multi-tier sensor/front-end assemblies

Table 12: WG7 research goals in the period 2024 - 2026

10 WG8: Outreach and dissemination

WG8 aims at promoting outreach and disseminating the activities of the DRD3 collaboration in coordination with other similar international and ECFA activities.

The WG8 activities can be broadly divided into:

- Disseminating knowledge on solid-state detectors to people working in high-energy physics (training, lectures, mobility)
- Disseminating knowledge on solid-state detectors to high-school students and the general public.

10.1 Disseminating knowledge on solid-state detectors to people working in high-energy physics

These activities aim to provide training and disseminate the experimental techniques needed in DRD3 activities.

- Organize schools for Ph.D. students and young post-docs on TCAD, FPGA programming, Geant4, AllPix2 etc.
- Organize stages for undergraduate students and promote exchange programs between labs. Financial support might be offered.
- Participation in instrumentation schools, offering lectures on DRD3 topics (for example, the CERN or FNAL schools).
- Share knowledge of measurement techniques such as device characterizations using IV, CV characteristics, transient studies using TCT, detector telescopes built using beta sources, handling and measurements of irradiated sensors.
- Present DRD3 work at conferences, providing opportunities for young researchers to be speakers at important international conferences.
- Publish papers and proceedings so that the DRD3 activities are documented in printed papers.

One exciting aspect is to create partnerships between established and new laboratories so that the upcoming groups can profit from the accumulated knowledge of the more experienced groups.

The DRD3 website will be the point of entry to advertise all DRD3 activities. It will contain links to the DRDs meetings; it will list opportunities for conferences, stages, and so on. It will also collect documentation on how to perform the various experimental techniques.

10.2 Disseminating knowledge on solid-state detectors to high-school students and the general public

Many of the DRD3 members are engaged in outreach activities at various levels, such as high-school seminars, hands-on experiments for young students, and community meetings. WG8 aims to collect materials and suggestions for these activities so that it will be easier for new members to carry on the same activities in new places.

10.3 WG8 Research Goals

The research goals of WG8 are summarized in Table 13.

WG8 research goals <2027	
	Description
RG 8.1	Design and set-up of the DRD3 web site
RG 8.2	Collection of the outreach material
RG 8.3	Set-up and organize schools and exchange programs
RG 8.4	Set-up of the DRD3 conference committee

Table 13: WG8 research goals in the period 2024 - 2026

11 DRD3 Resources (2024 - 2026)

The questionnaire asked resources for the following two categories:

- **Present situation:** Resource allocation expected on existing funding lines for the period 2024-26.
- **Strategic R&D:** Resource allocation coming from the funding requests for strategic R&D you intend to file.

Table 14 shows the resources available to DRD3 in the period 2024 - 2026.

Resources available to the DRD3					
	Present situation			Strategic R&D	
	Permanent [FTE/y]	Non Permanent [FTE/y]	Budget [kCHF/y]	Non Permanent [FTE/y]	Budget [kCHF/y]
Total	170.7	156.3	5070.2	170.9	7898.5

Table 14: DRD3 resources per year in the period 2024 - 2026

The resources for each research goal are presented in Table 15 while the resources per task and work package are presented in Table 16

Resources per each research goal					
	Present situation			Strategic R&D	
Research goal	Permanent [FTE/y]	Non Permanent [FTE/y]	Budget [kCHF/y]	Non Permanent [FTE/y]	Budget [kCHF/y]
1.1	16.5	15.8	531.3	18.2	851.1
1.2	10.8	11.8	354.3	12.4	554.0
1.3	12.1	12.5	397.2	14.0	941.8
1.4	12.5	11.5	412.3	12.7	590.9
Total	52.0	51.5	1695.2	57.3	2937.7
2.1	3.4	5.0	83.6	4.8	152.9
2.2	8.5	6.9	266.3	7.1	267.5
2.3	11.9	12.9	328.2	13.7	464.7
2.4	4.9	6.8	145.4	5.0	103.4
Total	28.7	31.6	823.4	30.7	988.6
3.1	3.6	4.2	100.1	3.7	167.9
3.2	4.1	2.5	114.8	5.8	381.1
3.3	9.8	6.7	203.8	6.6	315.9
3.4	7.2	8.4	157.3	8.5	311.4
Total	24.8	21.8	576.0	24.5	1176.3

4.1	3.7	2.9	82.1	3.4	178.4
4.2	5.6	5.6	114.2	6.0	299.9
4.3	2.1	1.7	54.9	2.6	89.1
4.4	4.4	3.3	144.8	3.8	137.6
4.5	1.7	1.8	28.2	1.7	38.7
Total	17.4	15.3	424.2	17.5	743.6
5.1	2.9	2.4	47.8	2.3	82.9
5.2	5.8	5.2	141.9	5.8	164.3
5.3	3.8	3.3	100.8	2.4	95.5
Total	12.6	10.9	290.5	10.4	342.6
6.1	1.5	1.6	47.5	0.9	45.9
6.2	3.9	2.4	160.6	3.8	210.2
6.3	1.8	1.9	146.1	2.8	178.4
6.4	2.5	1.5	20.2	1.6	39.6
Total	9.6	7.5	374.5	9.1	474.1
7.1	2.2	1.1	60.3	3.6	111.8
7.2	3.5	1.9	125.9	4.6	195.8
7.3	3.5	1.7	90.6	4.7	161.6
7.4	4.5	2.9	147.9	4.7	169.7
7.5	1.6	1.3	48.8	1.2	88.2
Total	15.3	8.8	473.4	18.6	726.9
8.1	0.5	0.4	25.2	1.2	15.2
8.2	1.3	1.5	13.6	2.7	67.9
8.3	5.2	4.6	244.2	4.9	300.2
8.4	3.3	2.4	129.9	2.9	125.3
Total	10.3	8.9	413.0	11.6	508.7

Table 15: Resources per year for each research goal in the period 2024 - 2026

Resources per each work package and task					
	Achievable in Present Situation			**Additional Strategic**	
TASK	Permanent [FTE/y]	Non Permanent [FTE/y]	Budget [kCHF/y]	Non Permanent [FTE/y]	Budget [kCHF/y]
T1.1	19.9	18.5	602.0	21.1	966.5
T1.2	14.8	14.9	442.6	15.9	699.1
T1.3	14.6	14.4	456.8	16.1	1009.2
T1.4	16.3	14.7	511.6	16.2	752.5

WP1 Total	65.5	62.6	2013.0	69.4	3427.4
T2.1	17.8	16.5	507.9	16.4	653.4
T2.2	24.4	24.9	688.6	22.8	889.1
WP2 Total	42.2	41.5	1196.5	39.2	1542.5
T3.1	12.4	11.5	450.1	13.2	618.4
T3.2	8.6	8.6	240.7	8.8	344.7
T3.3	21.5	16.9	502.8	20.5	958.7
WP3 Total	42.6	37.0	1193.6	42.5	1921.8
T4.1	5.4	3.3	168.2	4.5	265.6
T4.2	6.6	4.3	212.7	6.1	305.2
T4.3	5.9	5.0	196.4	6.5	310.2
T4.4	2.6	2.6	89.8	2.8	125.9
WP4 Total	20.5	15.2	667.1	19.9	1006.9

Table 16: Resources per year for each Work Package in the period 2024 - 2026.

Table 16 lists the resources for each of the four work packages on the granularity of the individual tasks within the work packages. The resources that are expected to be available on existing budget lines or through very likely to be received future resources are shown as *Present situation* funds, while additional funds required to fulfill the complete strategic R&D work program and yet to be requested through future funding requests are labelled as *Additional Strategic* funds. The presented data are given under the assumption that all participating institutes join the Work Package(s) covering their submitted expression of interest in research areas of the DRD3 collaboration.

11.1 Resources for each working group

Figure 9 shows the resources per research goal while Figure 10 shows the resources for each working group.

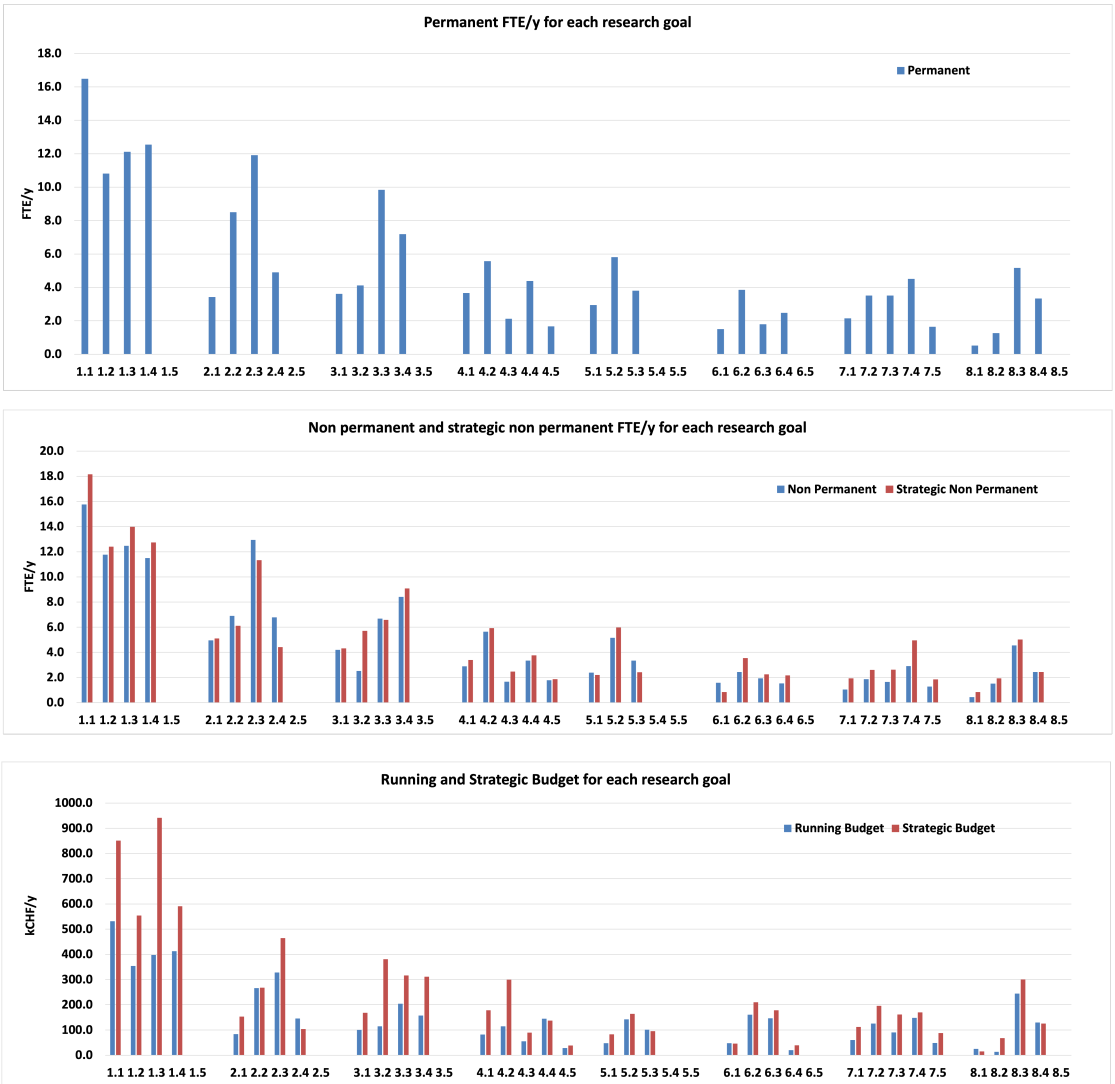

Figure 9: Resources per year for each research goal in the period 2024 - 2026

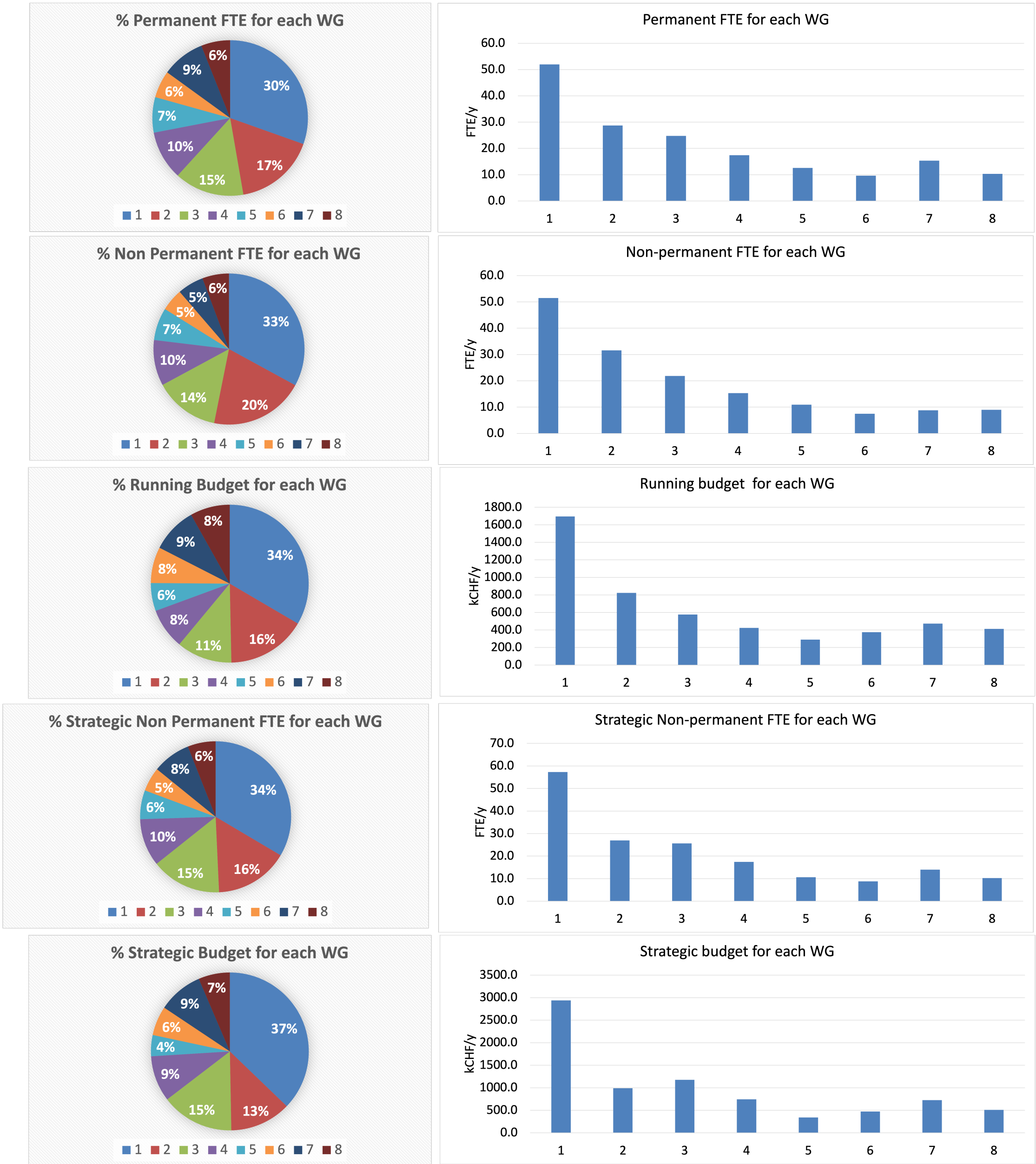

Figure 10: Resources per year for each working group in the period 2024 - 2026

12 Path to the DRD3 collaboration

The institutes participating in the proposal designated a contact person who served as a member of the provisional institution board at the time of the submission of the first proposal. Additionally, these participating institutions provided a comprehensive list of individuals involved in the proposed DRD3 activities.

Following the submission of the first version of the proposal to the DRDC, the DRD3 proposal team collected nominations for the collaboration board chair (CB chair). The election of the collaboration board chair, utilizing the CERN e-voting system, occurred immediately after the provisional approval of DRD3 and prior to the inaugural meeting of the collaboration. The DRD3 proposal team together with elected CB chair collected nominations for the spokesperson of the collaboration (SP). The inaugural meeting with elections of the SP took place in February 2024. This marked the conclusion of the DRD3 proposal team's mandate.

The SP proposed the organizational scheme of the collaboration, WG/WP conveners/leaders, and the SP deputies which were endorsed by the collaboration at the CB meeting in April 2024.

The WG/WP leaders with DRD3 management team (SP, deputies and CB chair) will collaboratively prepare the agenda and program for the first DRD3 week. The DRD3 manamegent formulated the rules of collaboration which should be discussed and agreed in the collaboration. These rules will be to large extent transferred also to the Memorandum of Understanding (MoU). The establishing of all collaboration bodies should be proposed to the collaboration by the first DRD3 week.

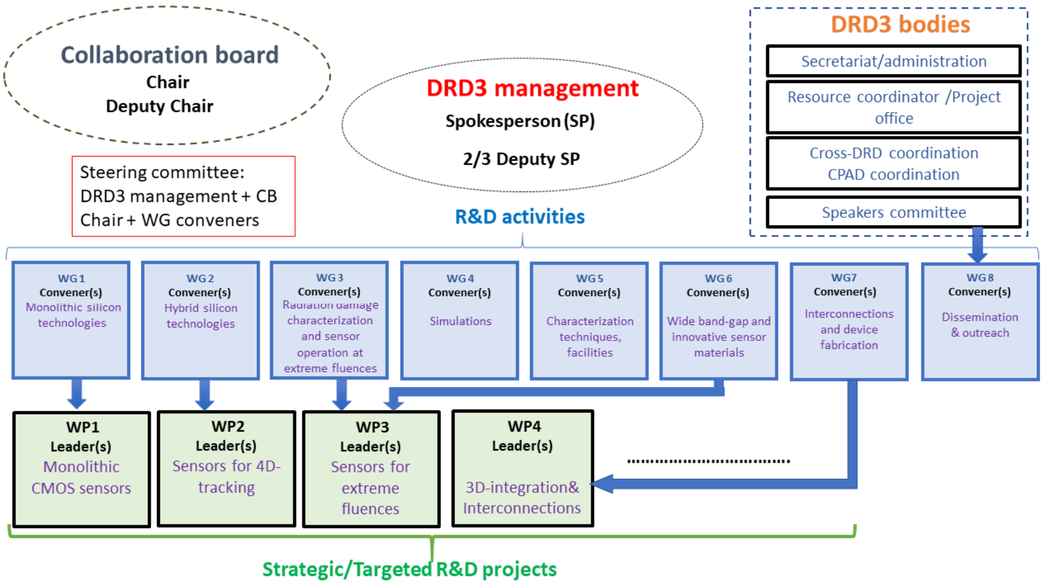

Figure 11: DRD3 organizational chart as of 2024. The blue lines denote the WG conveners taking also roles of designated WP leaders and Speaker's committee chair.

12.1 Funding for DRD3 strategic R&D

Funds for the strategic R&D come from national funding agencies and other sources and belong to the respective institutes. The strategic R&D will be the focus of the DRDC reviews.

12.2 Funding for DRD3 blue-sky R&D

Each institute will contribute to the DRD3 Blue-sky common fund. The amount of this levy is expected to be initially 2,000 CHF per year. The new DRD3 CB will define the rules for the funding scheme.

12.3 Funding for DRD3 operation

Each institute will contribute to the cost of the DRD3 collaboration with the host institution covering most of these costs. These costs include, for example, the personnel for administrating the DRD3 collaboration. The new DRD3 CB will define the amount of this levy. We encourage the DRDC to establish a common secretariat for the DRDs.

12.4 Funding presently available in the RD50 collaboration

At the end of 2023, the RD50 collaboration ceased to exist. The funding still present in the RD50 common fund will be transferred to the DRD3 collaboration. This fund will be managed by and available to former RD50 members.

13 Annex - I: List of institutions

	Country	Institution	CB representative	Contact
1	Austria	Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften (OEAW-HEPHY Vienna)	Thomas Bergauer	thomas.bergauer @ oeaw.ac.at
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Table 17: List of DRD3 institutions

14 Annex II: Relationship between work packages and research goals

Tables 18 shows the various links between the work package and the research goals.

Work Package		3.1 Monolithic CMOS sensors				3.2 4D Tracking		3.3 Extreme Fluence			3.4 Intercon.			
Tasks		Spatial resolution	Temporal resolution	Read-out architecture	Radiation Tolerance	3D sensors	LGAD	Wide band-gap materials	Diamond	Silicon	maskless interconnect	in house post-processing	advanced interconnect	mechanics and cooling
RG Description														
1.1	Spatial resolution: ≤3 μm position resolution	X		X									X	X
1.2	Temporal resolution: towards 20 ps timing precision		X	X									X	X
1.3	Readout architectures: towards 100 MHz/cm^2, and 1 GHz/cm^2 with 3D stacked monolithic sensors			X	X								X	
1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRa			X	X								X	
1.5	Low-cost large-area CMOS sensors	X	X	X	X								X	
2.1	Reduction of pixel cell size for 3D sensors					X					X	X		X
2.2	3D sensors for timing (≤ 55 × 55 um, < 50 ps)					X					X	X		X
2.3	LGAD for 4D tracking < 10 um, < 30 ps, wafer 6” and 8”						X				X	X		X
2.4	LGAD for ToF (Large area, < 30 um, < 30 ps)						X				X	X		X
3.1	Build up data sets on radiation-induced defect formation in WBG materials							X	X					
3.2	Develop silicon radiation damage models based on measured point and cluster defects	X	X	X	X	X	X			X				
3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation	X	X	X	X	X	X			X				

3.4	Measure and model the properties of silicon and WBG sensors in the fluence range 10^{16} to $10^{18} \mathrm{n_{eq}cm^{-2}}$							X	X	X				
4.1	Flexible CMOS simulation adaptable to different technology nodes and development of connections between tools for device-level simulation and electronic circuit design/validation	X	X	X	X									
4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools	X	X	X	X	X	X	X	X	X				
4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.	X	X			X	X	X	X	X				
4.4	Developing of bulk and surface model for $10^{16}\mathrm{cm}^{-2} < \Phi_{eq} < 10^{17}\ \mathrm{cm}^{-2}$							X	X	X				
4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields	X	X			X	X							
5.1	Develop TPA-TCT	X	X			X	X			X				
5.2	Common infrastructure	X	X	X	X	X	X	X	X	X				
5.3	Networking and training on methods	X	X	X	X	X	X	X	X	X				
6.1	3D diamond detectors, cages / interconnects, base length 25 μm , impact ionization					X			X					
6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.							X						
6.3	Improve tracking capabilities of WBG materials					X	X	X						
6.4	Apply graphene and/or other 2D materials in radiation detectors; understand signal formation.						X	X		X				
7.1	Yield consolidation for fast interconnections					X	X				X			
7.2	Demonstration of in-house process for single dies and a range of pitch (down to $< 30\mu m$) pixel interconnections					X	X				X	X		

7.3	Development of maskless post-processing for classical bump-like interconnection technologies					X	X				X	X		
7.4	Develop wafer-to-wafer in presently advanced interconnection technologies					X	X					X	X	
7.5	Develop VIAS in multi-tier sensor/front-end assemblies	X	X	X	X	X	X					X	X	

Table 18: Mapping of DRDTs, WPs, and research goals

15 Annex - III: Involvement of each institution in the work packages

Workpackage	3.1 Monolithic CMOS sensors				3.2 4D Tracking		3.3 Extreme Fluence			3.4 Intercon.			
Tasks	Spatial resolution	Temporal resolution	Read-out architecture	Radiation Tolerance	3D sensors	LGAD	Wide band-gap materials	Diamond	Silicon	maskless interconnect	in house post-processing	advanced interconnect	mechanics and cooling
Institute													
Aerospace Science and Technology Department, National and Kapodistrian University of Athens	X	X	X	X						X			
AGH University of Krakow, Faculty of Physics and Applied Computer Science						X			X				
Aix-Marseille University			X			X	X				X		X
Ankara University													
Argonne National Laboratory		X	X			X						X	X
Bolu Abant Izzet Baysal University													
Brookhaven Narional Laboratory	X	X	X	X	X	X		X			X		X
Brown University						X	X		X				
Brunel University London	X			X			X		X				
Caltech													
Carleton University - National Research Council	X		X	X			X		X				
Cavendish Laboratory, University of Cambridge	X	X	X	X					X				
CEA-Irfu	X	X	X	X					X				
Centro Nacional de Aceleradores, CNA (Universidad de Sevilla, Junta de Andalucía, CSIC)					X	X	X	X	X				
Centro Nacional de Microelectrónica (IMB-CNM-CSIC)					X	X	X	X	X			X	X
CERN	X	X	X	X	X	X	X		X	X		X	X
Charles University	X	X				X			X				
CiS Forschungsinstitut für Mikrosensorik GmbH				X		X			X	X		X	

CPPM, Marseille	X	X	X								X		X
Daresbury Laboratory, STFC													
Department of Physics and Technology, University of Bergen			X	X	X				X				
DESY	X	X	X								X		X
Duke University													
Escuela Técnica Superior de Ingeniería (School of High Engineering), University of Sevilla	X	X	X					X					X
Federal University of Rio Grande do Sul (UFRGS)							X						
Fermilab	X	X	X	X	X				X		X	X	X
FNSPE CTU				X		X	X		X				
Fondazione Bruno Kessler	X	X			X	X			X	X	X	X	
Fraunhofer IZM									X	X	X		
Galician Institute for High Energy Physics (IGFAE)					X	X			X			X	
Glasgow University	X		X	X	X			X	X	X	X	X	X
GSI Helmholtzzentrum für Schwerionenforschung GmbH	X		X	X		X		X					
Halbleiterlabor der Max-Planck-Gesellschaft						X			X	X	X	X	X
Heidelberg, Physics Institute	X	X	X	X				X				X	
Helsinki Institute of Physics (HIP)					X	X		X	X				
Horia Hulubei National Institute for RD in Physics and Nuclear Engineering							X		X				
IFIC (CSIC-UV)	X		X	X		X			X			X	X
IJCLAB					X			X	X		X		
Indian Institute of Technology Madras		X		X	X	X	X		X				X
INFN Genova					X	X			X			X	X
INFN Bari	X		X	X	X				X			X	
INFN Firenze					X	X		X	X	X	X	X	
INFN Lecce													
INFN Padova	X		X	X	X								X
INFN Perugia					X	X	X	X				X	X
INFN Pisa	X	X	X						X				X
INFN Torino	X	X	X			X			X				
INFN Trieste	X	X	X	X	X	X	X	X	X	X	X	X	
Institut de Fisica d'Altes Energies (IFAE)		X		X	X	X			X				
Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften (OEAW-HEPHY Vienna)	X	X	X	X		X	X						

Institut für Physik Humboldt-Universität zu Berlin			X						X				
Institute for Experimental Physics, University of Hamburg						X	X		X				
Institut pluridisciplinaire Hubert Curien (IPHC)	X	X	X	X									
Institute of Experimental and Applied Physics, Czech Technical University					X	X							
Institute of High Energy Physics, CAS	X		X	X		X	X						
Institute of Nuclear and Particle Physics National Center for Scientific Research (NCSR) DEMOKRITOS	X		X	X	X	X			X				
Institute of Physics, Czech Academy of Sciences, Prague				X			X		X				
Institute of Plasma Physics and Laser Microfusion							X	X					
Instituto de Física de Cantabria (CSIC-UC)					X	X	X		X				
Instituto Tecnológico de Aragón (ITAINNOVA)					X	X	X					X	
IP2I Lyon CNRS/IN2P3	X	X	X							X			
IPA, ETH Zürich	X	X		X				X	X				X
Istanbul University-Cerrahpasa, Institute of Nanotechnology and Biotechnology						X	X		X				
Istanbul University-Cerrahpasa, Institute of Nanotechnology and Biotechnology			X				X	X	X	X	X		
Jožef Stefan Institute (JSI)	X			X	X	X	X	X	X				
Karlsruhe Institute of Technology (KIT)	X	X	X	X		X			X	X	X	X	
KEK, High Energy Accelerator Research Organization	X	X	X	X	X	X	X		X				
Laboratoire AstroParticule et Cosmologie (APC)	X		X						X				
Laboratoire de Physique Subatomique et de Cosmologie LPSC							X						
Lappeenranta-Lahti University of Technology (LUT)				X	X	X		X	X	X	X		X
Lawrence Berkeley National Laboratory						X	X						X
LHEP, University of Bern	X	X		X	X	X							

LIP, Laboratório de Instrumentação e Física Experimental de Partículas		X		X		X	X		X			X	
Los Alamos National Laboratory	X	X	X	X	X		X	X		X	X	X	X
LPNHE Paris		X	X	X		X			X	X	X	X	X
Ludong University				X	X				X				
Max-Planck-Institut für Physik (Werner-Heisenberg-Institut)	X	X			X					X	X	X	
National Institute of Materials Physics						X	X		X				
National Institute of Science Education and Research				X	X	X			X			X	
National Technical University of Athens Department of Physics	X	X	X	X	X	X	X		X				X
Nikhef	X	X	X	X	X	X	X		X				X
Oak Ridge National Laboratory	X	X	X	X		X		X	X	X	X	X	
Ohio State University				X		X	X	X					
Oregon University													
Physics Institute, University of Goettingen	X	X	X	X		X							
PSI	X	X	X		X								
Purdue University					X	X			X				X
Queen Mary University of London									X				X
Ruder Boskovic Institute							X	X					
Rutherford Appleton Laboratory							X	X					
Santa Cruz Institute for Particle Physics (SCIPP) University of California- Santa Cruz	X		X	X		X	X	X	X			X	
Simon Fraser University						X			X			X	
SLAC National Accelerator Laboratory						X							
Stony Brook University													
Tel Aviv University							X	X	X				
The University of Manchester			X		X	X		X					X
TRIUMF		X			X	X			X		X	X	X
TU Dortmund University, Department of Physics		X	X	X	X							X	
UC Santa Cruz, Radiological Instrumentation Lab										X			
Universidad Andrés Bello, SAPHIR Millennium Institute of ANID	X	X	X			X	X	X	X	X	X	X	X
Universidad Técnico Federico Santa María	X		X	X	X	X							X

Universidade de São Paulo					X	X							
Università di Milano and INFN Sezione di Milano	X				X		X			X	X	X	X
Universita‘ degli Studi di Milano - Bicocca and INFN	X	X		X	X	X	X	X	X				
University of Birmingham	X	X	X	X		X			X				
University of Bonn, Physikalisches Institut	X	X	X	X	X		X		X	X	X	X	
University of Bristol	X	X	X			X	X	X		X		X	X
University of Chicago													
University of Delhi					X	X		X					X
University of Edinburgh	X		X	X		X			X				X
University of Freiburg		X		X	X								
University of Illinois at Chicago	X	X	X	X	X	X			X	X	X	X	X
University of Ioannina, Physics Department, High Energy Physics group	X	X	X										
University of Liverpool	X	X		X		X	X		X		X	X	X
University of Massachusetts, Amherst													
University of Montenegro					X	X	X	X	X				X
University of Muenster, Institut fuer Kernphysik	X	X			X	X				X		X	X
University of New Mexico	X		X	X	X	X	X	X					X
University of Oslo, Department of Physics	X	X	X	X	X	X	X	X	X	X	X	X	X
University of Oxford Sub Department of Particle Physics	X	X	X	X	X	X	X		X			X	X
University of Science and Technology of China	X	X	X		X	X						X	
University of Tennessee-Knoxville	X			X	X	X	X		X	X	X		
University of Texas at Arlington													
University of Trento and TIFPA-INFN	X	X		X	X				X				
University of Warwick				X	X				X			X	
University of Washington													
University of West Bohemia	X	X			X		X						
University of Zagreb, Faculty of Electrical Engineering and Computing, Department of Electronics, Micro and Nano Electronics Laboratory		X	X	X									
University of Zurich	X	X				X						X	X
Vilnius University, Institute of Photonics and Nanotechnology						X	X	X	X				
Weizmann Institute of Science	X	X		X	X		X	X	X			X	

Table 19: Involvement of the DRD3 institutions in each of the task. Note: some institutions did not express an interest.

16 Annex IV: List of research goals

Table 20 lists the DRD3 research goals. Additional RGs can be added following the request of DRD3 collaborators.

WG1 research goals	
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, and 1 GHz/cm^2 with 3D stacked monolithic sensors
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors
WG2 research goals	
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing ($\leq 55 \times 55$ μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6" and 8"
RG 2.4	LGAD for ToF (Large area, < 30 μm, < 30 ps)
WG3 research goals	
RG 3.1	Start of building up data sets on radiation-induced defect formation in WBG materials
RG 3.2	Continue developing silicon radiation damage models based on measured point and cluster defects
RG 3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation
RG 3.4	Expand the measurements and models of silicon and WBG sensors properties in the fluence range 10^{16} to $1 \cdot 10^{18}$ n_{eq}/cm^2
WG4 research goals	
RG 4.1	Flexible CMOS simulation adaptable to different technology nodes and development of connections between tools for device-level simulation and electronic circuit design/validation
RG 4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools
RG 4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.
RG 4.4	Developing of bulk and surface model for $10^{16}\mathrm{cm}^{-2} < \Phi_{eq} < 10^{17}$ cm^{-2}
RG 4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields
WG5 research goals	
RG 5.1	Developments and promotion of novel characterization techniques (TPA-TCT)
RG 5.2	Efficient exploitation of common large infrastructure
RG 5.3	Networking and training on methods
WG6 research goals	
RG 6.1	3D diamond detectors, cages / interconnects, base length 25 μm , impact ionization
RG 6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.
RG 6.3	Improve tracking capabilities of WBG materials
RG 6.4	Apply graphene and/or other 2D materials in radiation detectors understand signal formation.
WG7 research goals	
RG 7.1	Yield consolidation for fast interconnections

RG 7.2	Demonstration of in-house process for single dies and a range of pitch (down to <30 μm) pixel interconnections
RG 7.3	Development of maskless post-processing for classical bump-like interconnection technologies
RG 7.4	Develop wafer-to-wafer in presently advanced interconnection technologies
RG 7.5	Develop VIAS in multi-tier sensor/front-end assemblies
WG8 research goals	
RG 8.1	Design and set-up of the DRD3 web site
RG 8.2	Collection of the outreach material
RG 8.3	Set-up and organize schools and exchange programs
RG 8.4	Set-up of the DRD3 conference committee

Table 20: List of research goals in the period 2024 - 2026

17 Annex - V: DRD3 Proposal Team

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18 Acronyms used in the proposal

- ACF: Anisotropic Conductive Films
- ACP: Anisotropic Conductive Pastes
- BEOL: Back-End Of Line
- BSI: Back-Side Illuminated
- CA: Common Area
- CP: Common Project
- DJ-LGAD: Deep-Junction LGAD
- DLTS: Deep Level Transient Spectroscopy
- DMAPS: Depleted Monolithic Active Pixel Sensor
- DRC: Design Rule Checking
- DRDT: Detector R&D Theme
- EPR: Electron Paramagnetic Resonance
- FD-MAPS: Fully-Depleted Monolithic Active Pixel Sensor
- FSI: Front-Side Illuminated
- FTIR: Fourier Transform Infrared Spectroscopy
- iLGAD: inverted LGAD
- iPDK: Interoperable Process Design Kit
- LGAD: Low-Gain Avalanche Diode
- MAPS: Monolithic Active Pixel Sensor
- MC: Monte Carlo
- MPW: Multi-Project Wafer
- PDK: Process Design Kit
- PL: Photo Luminescence
- RG: Research Goal
- RSD: Resistive AC-Coupled Silicon Detectors
- RTO: Research and Technology Organisations
- SiC: Silicon Carbide
- SoA: Silicon on Aluminum
- TCAD: Technology Computer-Aided Design
- TCT: Transient Current Technique
- TI-LGAD: Trench-Isolated LGAD
- TPA: Two-Photon Absorption
- TRIBIC: Time-Resolved Ion Beam Induced Currents
- TSC: Thermally Stimulated Currents
- TSCap: Thermally Stimulated Capacitance
- TSV: Through Silicon Vias
- WBS: Wide Band-Gap Semiconductor
- XRD: X-Ray diffraction

19 References

References

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[3] https://cpad-dpf.org/.