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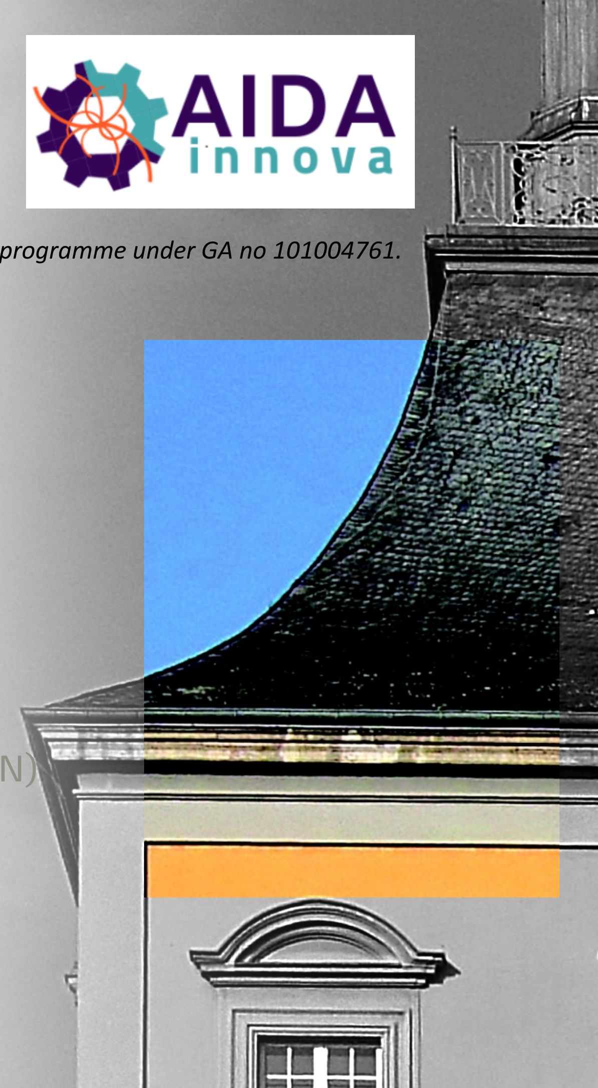
ULTRA-THIN HYBRID PIXEL DETECTORS USING WAFER-TO-WAFER BONDING

Y. DIETER, F. HÜGGING, S. ZHANG (UNIVERSITY OF BONN),
I.-M. GREGOR (DESY & BONN), T. FRITZSCH (FRAUNHOFER IZM BERLIN)

1ST DRD3 WEEK, WG7/WP4 SESSION,
CERN, 19 JUNE 2024



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ULTRA THIN HYBRID PIXEL DETECTORS

- Want to reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:
  - Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
  - Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
  - Thinning of FE and sensor parts to the minimum.
  - Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

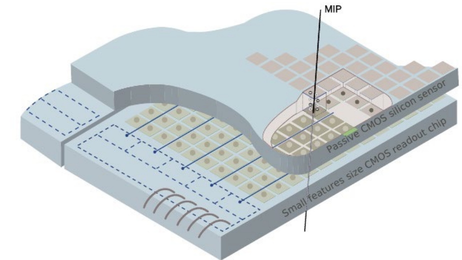
→ Target is the development of ultra-thin hybrid pixel detectors based on:

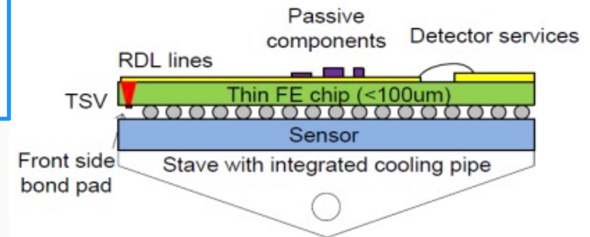
- 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
- ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS

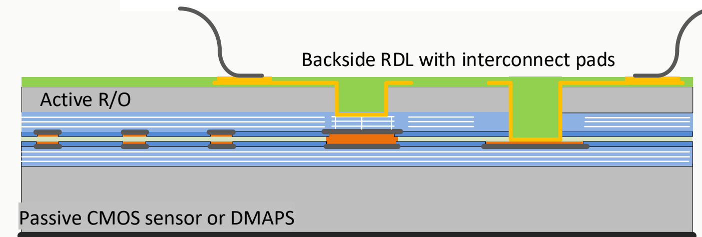
Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)

TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)

Ultra thin hybrid pixel module:
~20 µm FE &
50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)







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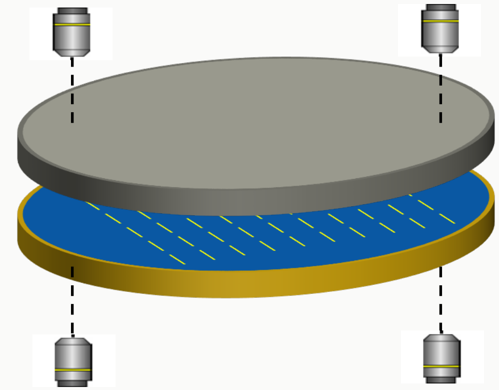
PROOF OF CONCEPT PROJECT FOR AIDAINNOVA

- Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:
  - Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
  - Use TimePix3 chip wafers (GF 130 nm on 200 mm wafers)



- Developing and optimization of hybridization process including thinning and interconnection from chip's backside at IZM.
- Longer Term: Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics

CMOS PIXEL SENSOR DESIGN

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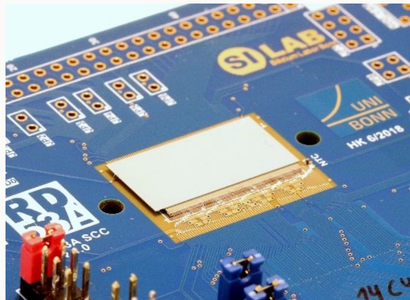
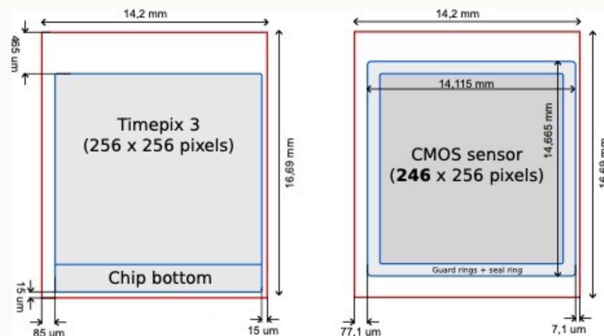
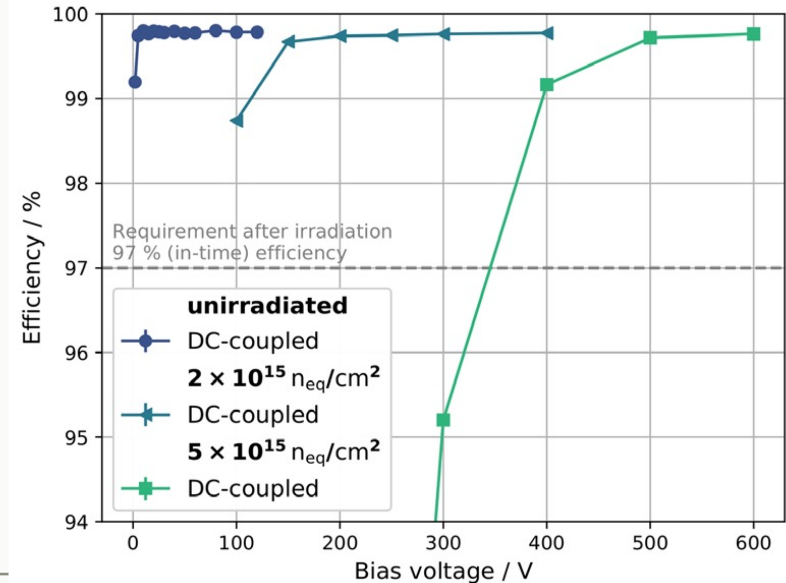
- Starting point for sensor: passive CMOS sensors developed in LFoundry 150 nm technology
- Radiation tolerant n-in-p pixel design in 150 nm CMOS technology
- CMOS fabrication process offers 200 mm wafers → fit to TimePix3 wafers
- Towards „thin hybrid sensor“:
  - Copy layout from former submissions
  - Adjust pixel size to Timepix3
  - Dedicated wafer layout

More information about passive CMOS sensors:

“Development and Characterisation of Passive CMOS Sensors for Pixel Detectors in High Radiation Environments”, PhD thesis Y. Dieter







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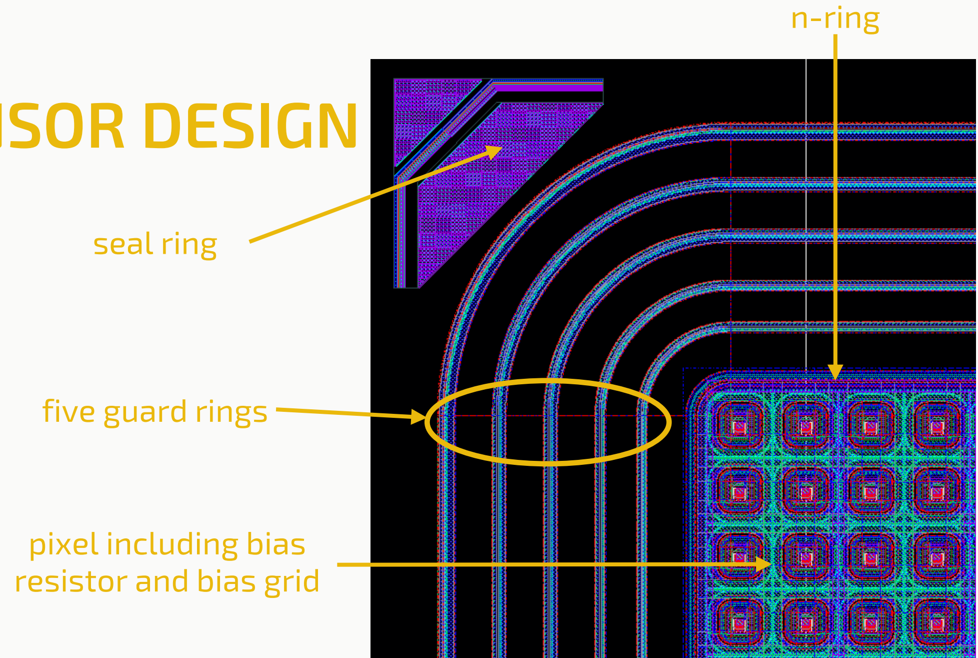
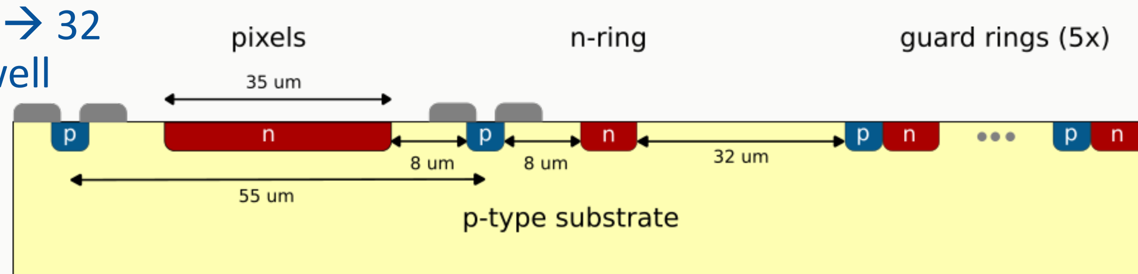
CMOS PIXEL SENSOR DESIGN

- Strategy: „copy“ layout from former passive CMOS submissions at LFoundry:
  - Match pixel size with TimePix3 pixel size → 55 µm pixels
  - Increase n-well size to 35 um → keep 8 µm spacing between n-well and p-stop
  - Poly-silicon bias resistor implemented (and bias grid)
  - N-ring surrounding the pixel matrix → 32 µm spacing between n-ring and p-well (from 1st guard ring)
  - Five n^+p guard rings





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W2W BONDING PROCESS DEVELOPMENT AT IZM

- **WP1: Design development and manufacturing of process qualification wafer, design preparation of functional TIMEPIX3 and DMAPS sensor wafer**
  - 1.1 Definition of technological approach for ultra-thin low-mass hybrid pixel detectors
  - 1.2 Process qualification design including test structures
  - 1.3 Fabrication of process development wafer
  - 1.4 Design and mask preparation for TIMEPIX3 readout electronics and DMAPS active sensor wafer
- **WP2: Wafer bonding and thinning process**
  - **Bonding material evaluation and process setup**
- **WP3: Wafer bonding with capacitive coupled IOs and conductive IOs**
- **WP4: Backside wafer process with TSV-etching and backside metallisation process**

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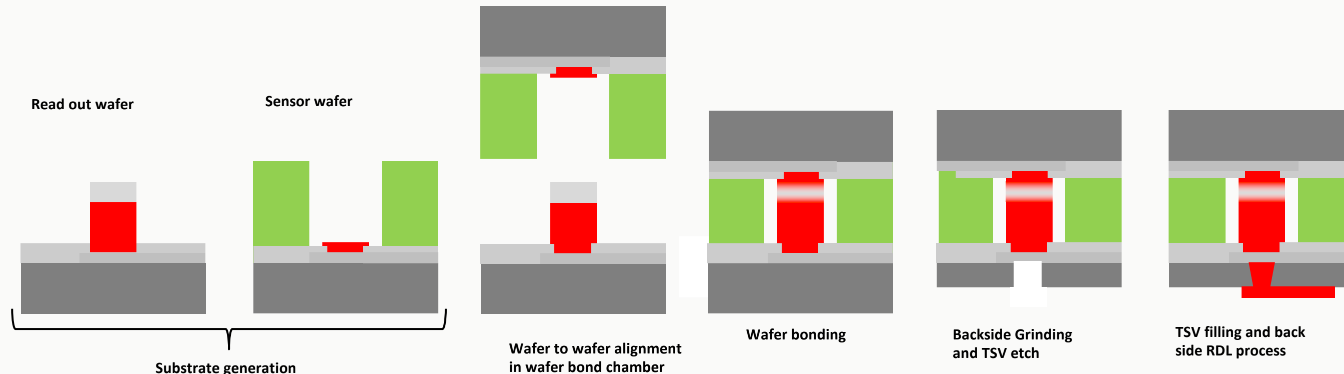
W2W BONDING - GENERAL PROCESS FLOW

- The Cu/Sn wafer bonding is a well established process
- The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously (polymer hybrid wafer bonding)
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required



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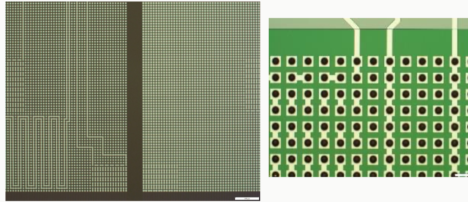
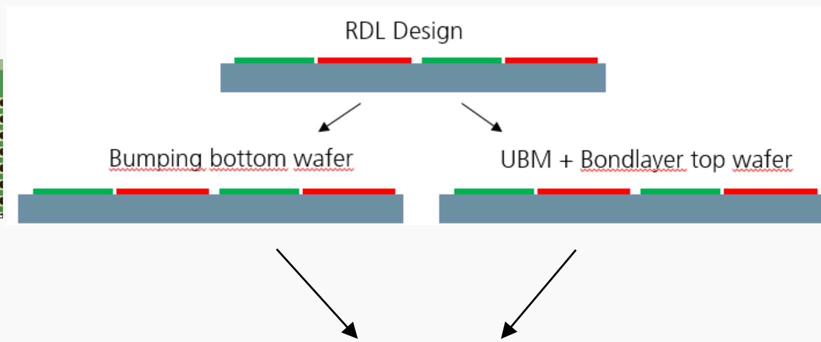
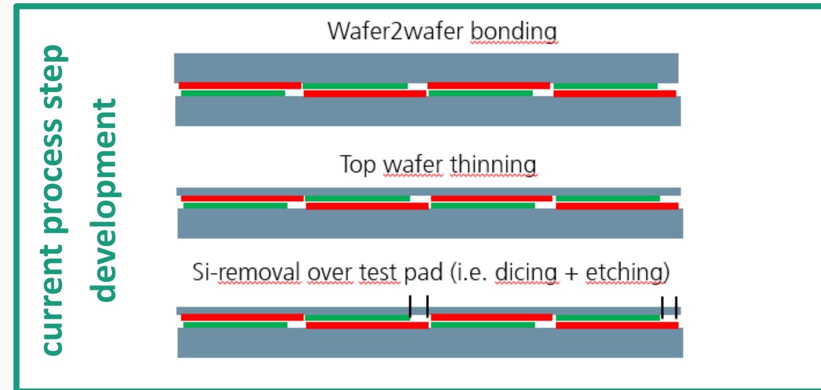
PROCESS SETUP USING DAISY CHAIN WAFER

W2W bonding setup bottom wafer:

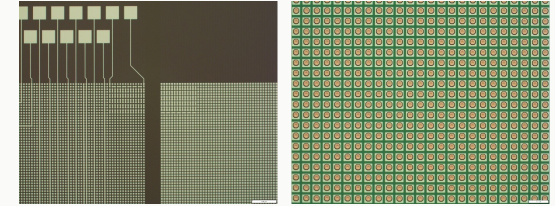


Bottom wafer with Cu-SnAg pillar





W2W bonding setup top wafer:



Top wafer with Cu-Pad and polymer layer

Process Development Goal:

Evaluation of a bonding material that enables the combination of a polymer glue bonding process with the Cu-SnAg pillar bonding process

Process evaluation with different wafer stacks:

I. Planar Glass-Si wafer: optical bonding interface characterization (fast track)

II. Planar Si-wafer with UBM: polymer bonding with topography wafer

III. Daisy-chain-test wafer (silicon to silicon): bonding process evaluation with focus on polymer layer thickness – Pillar/UBM height tolerances

Some details of different wafer stack types

see next slides

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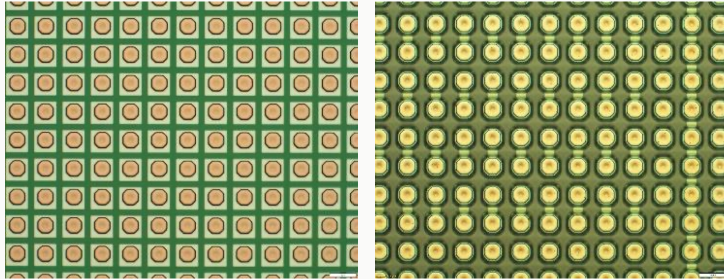
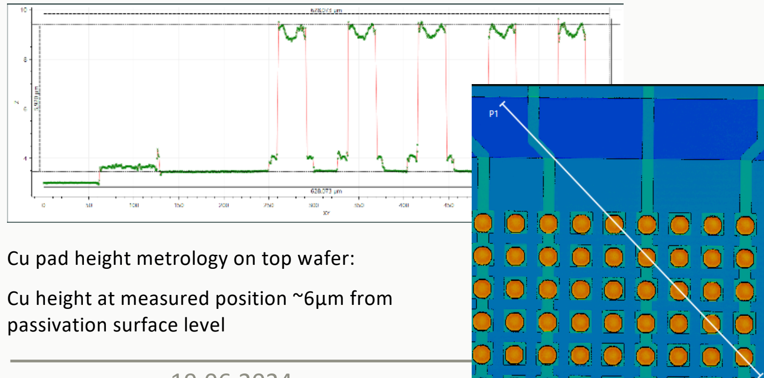
W2W BONDING – PROCESS EVALUATION III: DAISY-CHAIN-TEST WAFER

TOP wafer: Cu UBM pad and patterned polymer layer



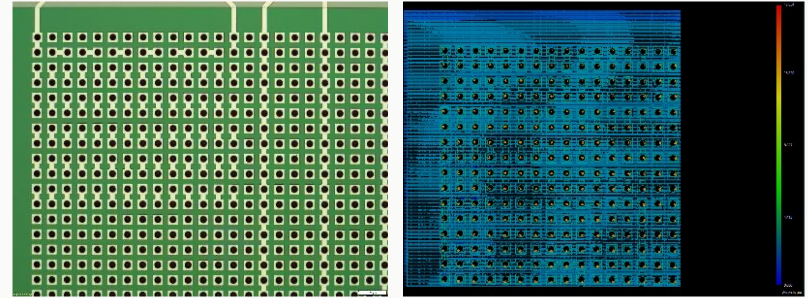
Cu-UBM pad wafer without (left) and with polymer bond layer (right)

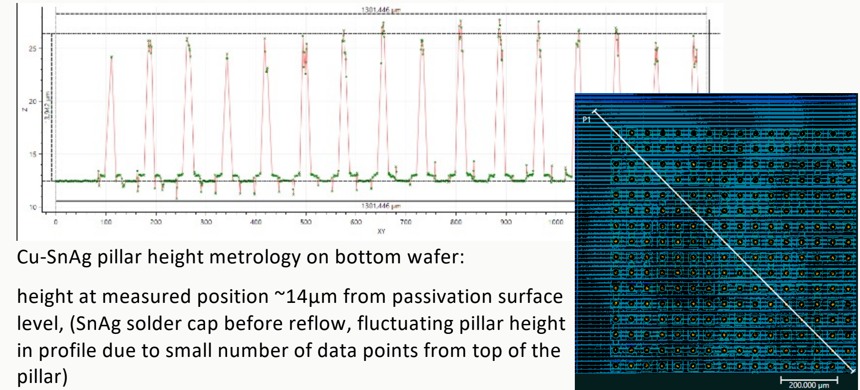


Cu pad height metrology on top wafer:

Cu height at measured position ~6µm from passivation surface level

BOTTOM wafer: Cu-SnAg pillar





Cu-SnAg pillar height metrology on bottom wafer:

height at measured position ~14µm from passivation surface level, (SnAg solder cap before reflow, fluctuating pillar height in profile due to small number of data points from top of the pillar)

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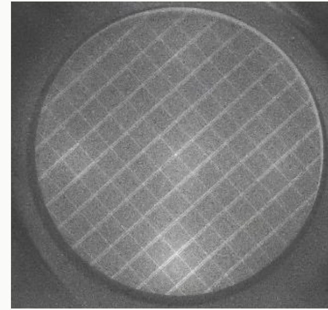
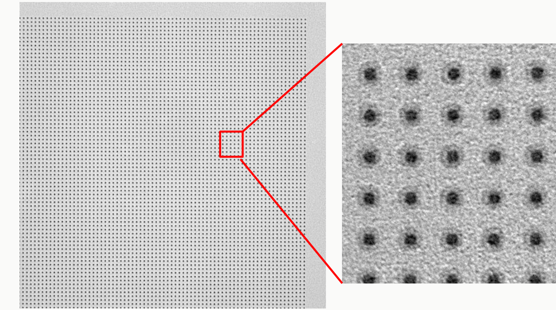
W2W BONDING – PROCESS EVALUATION III: WAFER TO WAFER BONDING

Bonding process evaluation using daisy-chain-test wafer:

TOP wafer: UBM pad and patterned polymer layer
BOTTOM wafer: Cu-SnAg pillar



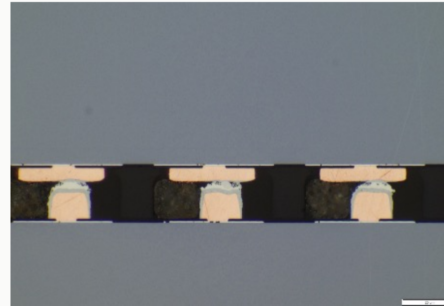
Full wafer IR image, details are to small for bond layer characterization

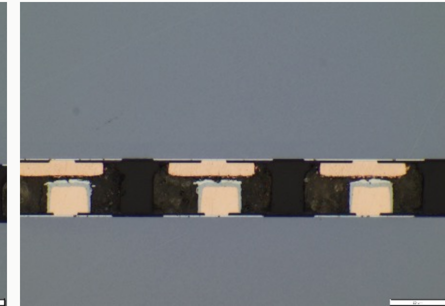


X-ray inspection of bonded chips: UBM pads - medium gray, pillar - dark gray; UBM and pillar are different in size

Preliminary Process Results:

- Process evaluated for 20µm polymer layer thickness, measured bond layer thickness: 21µm (+/- 0.5µm across the wafer)
- Pillar height: 13…15µm (as plated) (tolerances across the wafer) Cu pad height: 5.5µm (+/- 0.5µm across the wafer)
- Thinning of top wafer to 80µm thickness possible
- Dicing of wafer stack possible
- Low adhesion between top and bottom chip after dicing (chips can be easily de-bonded)
- Large area solder transfer from CuSnAg-pillar (bottom chip) to Cu pad (top chip) visible after top chip debonding but some pillars are not connected to Cu pads (see cross section)





cross section after wafer to wafer bonding:
Left: slightly connected pillars, solder transfer to Cu pad (top) visible
Right: gap between pillar and pad, no solder transfer to Cu pad (top) visible

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W2W BONDING – PROCESS EVALUATION SUMMARY

Preliminary conclusions:

- Lateral dimension (x, y) of bonding structures are sufficient to handle the W2W alignment tolerances (pad-, pillar-, polymer-via diameter)
- Very narrow tolerances in z-direction: pad – pillar – polymer thickness
- Bonding strength has to be increased, investigation of source for low adhesion strength ongoing

Next steps and investigations:

- increase of polymer adhesion strength: double layer approach, pre-conditioning, …
- increase of solder amount on pillar: adjust electro-plating layer height ratio Cu-SnAg
- bonding process optimization: adjust pressure-, time-, temperature-profile of the bonding process
- Electrical measurement of daisy-chain structures of bonded chip stack (additional 80µm silicon etch of probe pad area required)

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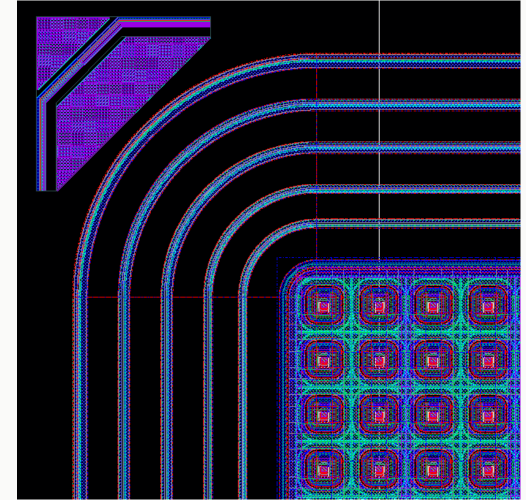
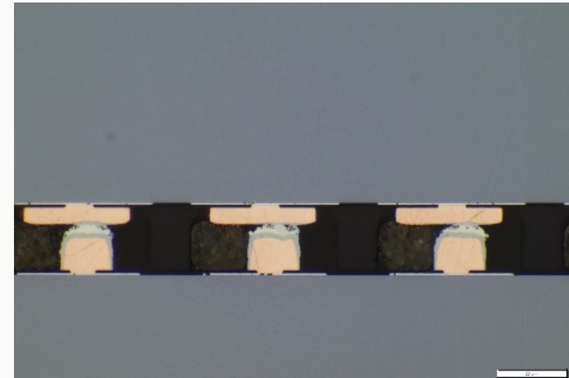
CONCLUSIONS + NEXT STEPS





- Preparations for W2W with Timepix3 and passive CMOS sensor well progressing
  - Timepix3 wafer available and feasible for W2W bonding
  - Sensor wafer design finished and processing about to start
  - W2W bonding process setup with daisy chain at IZM well advanced but still some optimizations needed
- Next steps:
  - Finishing W2W process setup and optimization including electrical test results on daisy chain wafers
  - Processing of passive CMOS sensor wafer designed for W2W bonding with Timepix3 wafers

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BACKUP

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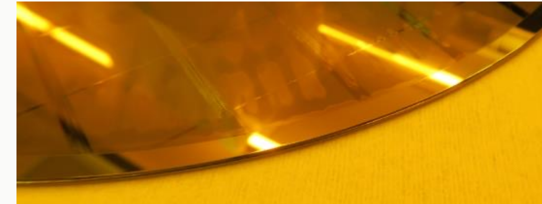
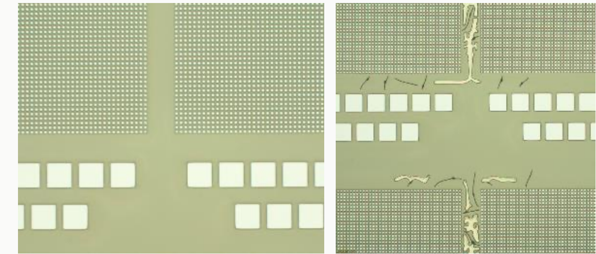
W2W BONDING – PROCESS EVALUATION I

TOP wafer: planar Si-wafer with patterned polymer layer
BOTTOM wafer: planar glass-wafer

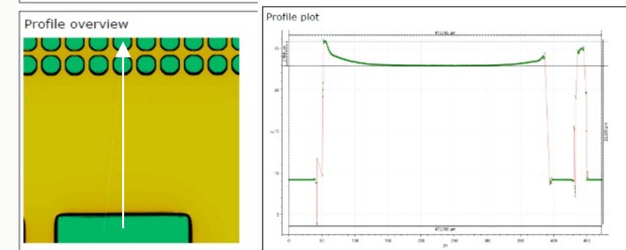
- **Wafer to wafer polymeric bonding material evaluation:**
  - Development of process chain for metal - polymer hybrid bonding
  - Silicon-glass wafer bond for visual inspection
  - (Evaluation of different bonding materials – to be continued)
- **Processing of setup bond wafer:**
  - Bond layer thickness adjustment
  - Bond layer planarity optimization
  - pre-conditioning of polymer
  - Influence of curing temperature
  - Bond parameter setting (pressure, temperature, time)
- **Evaluation target:**
  - Polymer layer height and planarity
  - Void-free bonding
  - No outgassing during bonding process
  - Lateral structure size stability



Si-Glass wafer stack (glass wafer on top)



Left: good bond; right: voids in bondlayer



Bond-layer thickness and planarity measurement (measurement before bonding)

W2W BONDING – PROCESS EVALUATION II

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TOP wafer: planar Si-wafer with polymer

BOTTOM wafer: pillar/UBM pad test wafer without solder

Polymer layer height and planarity

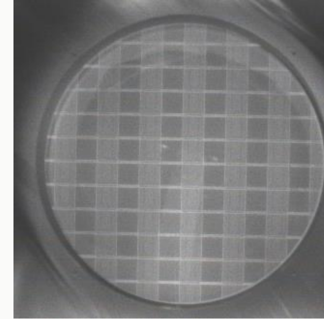
- Polymer process on planar Si-wafer
- Planarization process developed and evaluated
- Evaluation of bonding layer thickness along the process chain, calculation of pillar and UBM height

Bonding test and characterization

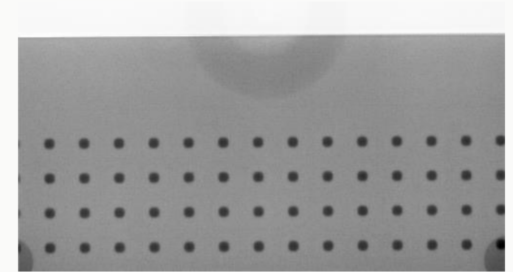
- Bonding test using pillar/UBM pad test wafer without solder for layer height analysis in combination with topography
- Check of characterization methods (IR, X-ray, cross section)

Preliminary Process Results

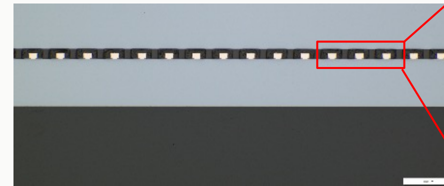
- Process evaluated for 20µm polymer layer thickness
- Bonding parameter profile setup tested (temperature, pressure, time, ramping)
- Bonding test successful: no delamination, stable pattern structure

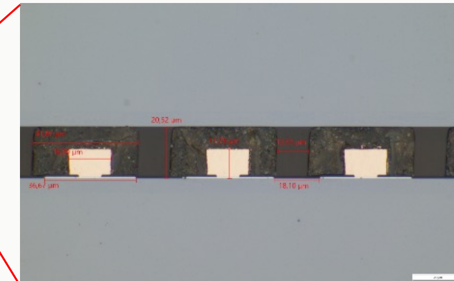


Full wafer IR image, details are to small for bond layer characterization



X-ray inspection of bonded chips, poor contrast of bond layer details and aluminium lines, only Cu pads visible

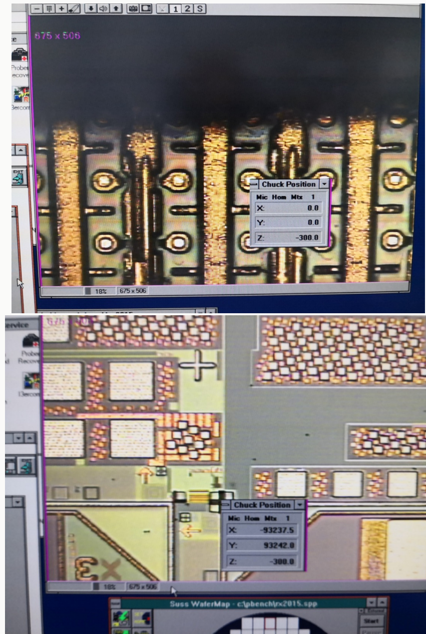


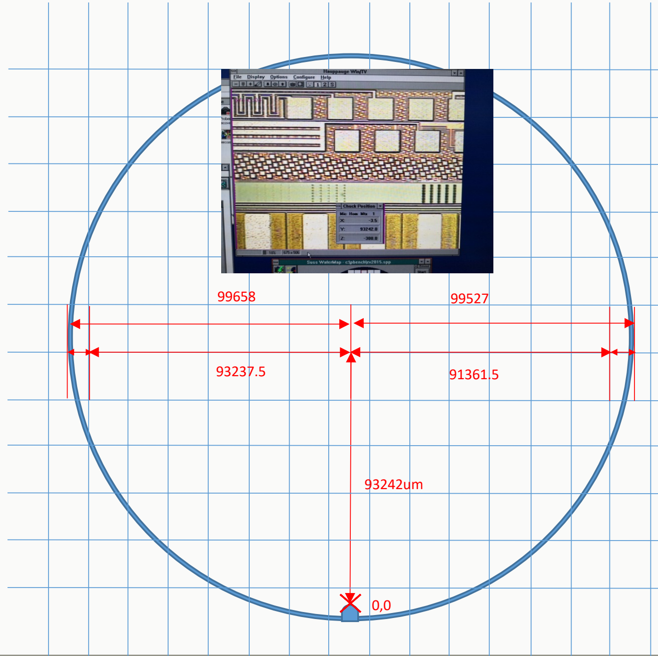


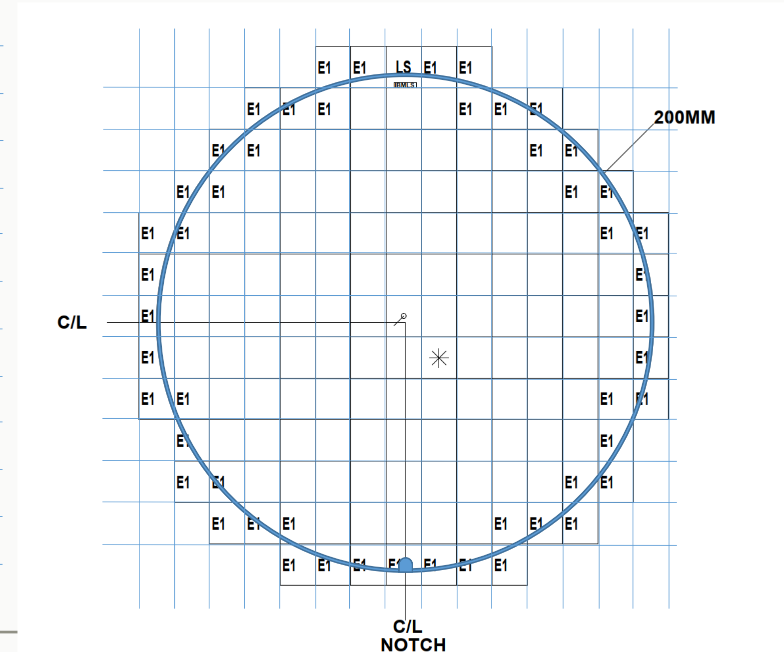
Bond layer evaluation and feature height measurement using Cu pillar + RDL test wafer
Recalculation of the required pillar + UBM height based on bond layer thickness results

TIMEPIX 3 WAFER EVALUATION

- TimePix3 Wafer have been checked to be compatible with W2W bonding:
  - Several wafers have been measured to confirm the reticule stepping is the same for all wafers
  - Wafer topography have been checked in detail by IZM and TimePix collaboration







pictures by M. Campbell et al.

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CMOS PIXEL SENSOR - SUBMISSION

- Full engineering run at LFoundry
  - Wafer2wafer bonding requires custom wafer layout
  - Reticle has to match with Timepix3 for proper overlay
- 25 wafers on high-resistivity Cz-Si and 150 um thickness
- Final details to be discussed with Lfoundry
- Start engineering run end of June