All-Silicon Module: Belle II and Beyond

- ▷ The PXD Module at Belle II
- ▷ Outlook – the way forward

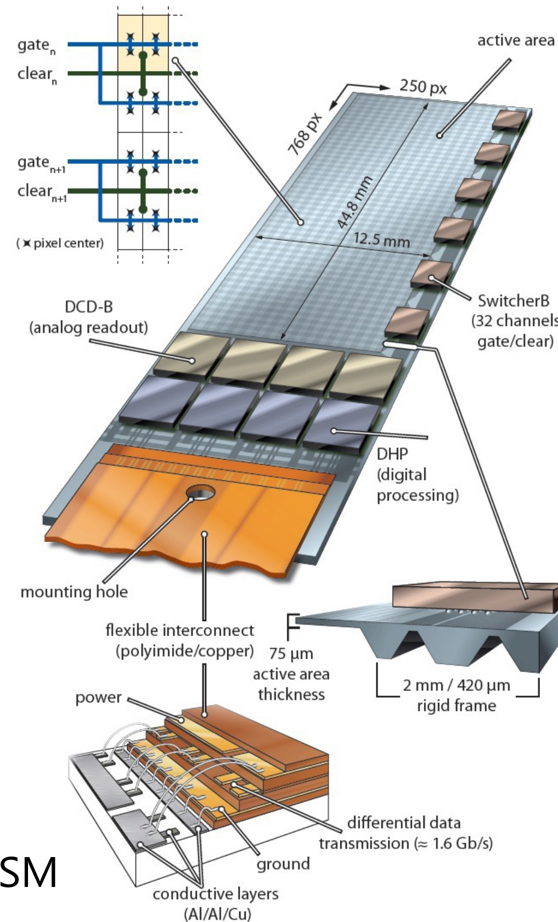
Ladislav Andricek

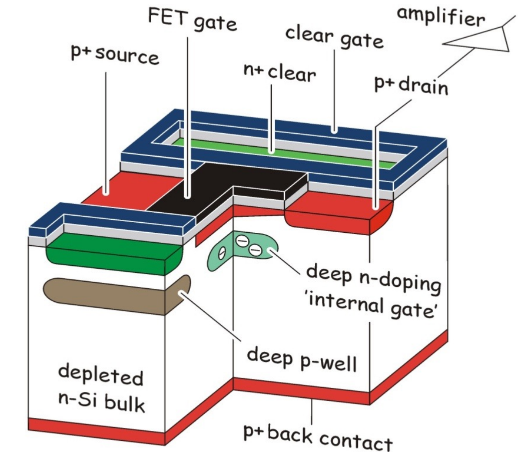
for the team at the Semiconductor Laboratory of the Max Planck Society

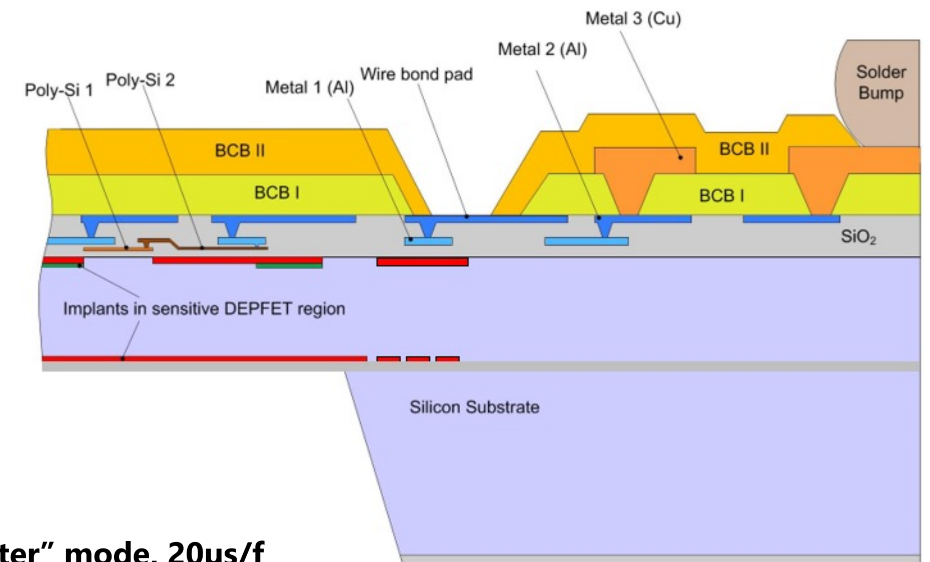
the DEPFET all-silicon module for Belle II PXD

- ▷ module design starts on wafer level
- ▷ module is one piece of silicon
  - ↳ Sensitive area (APS)
  - ↳ High density interconnect (HDI)
- ▷ HDI as board for non-sensor parts
  - ↳ UMC 180, TSMC 65, IBM/AMS/TSI 180
  - ↳ Passive components
  - ↳ On-module solder interconnect
- ▷ Off-module interconnect with flex
  - ↳ Solder and wire bonds
- ▷ “MCM-D”, “2.5 D”, “SoC” … We call it ASM

All-Silicon Module







- ▷ **Thin pixel array operated in „rolling shutter” mode, 20µs/f**
  - ↳ **Only 4/768 rows active a time → low power in active area**

the DEPFET all-silicon module for Belle II PXD

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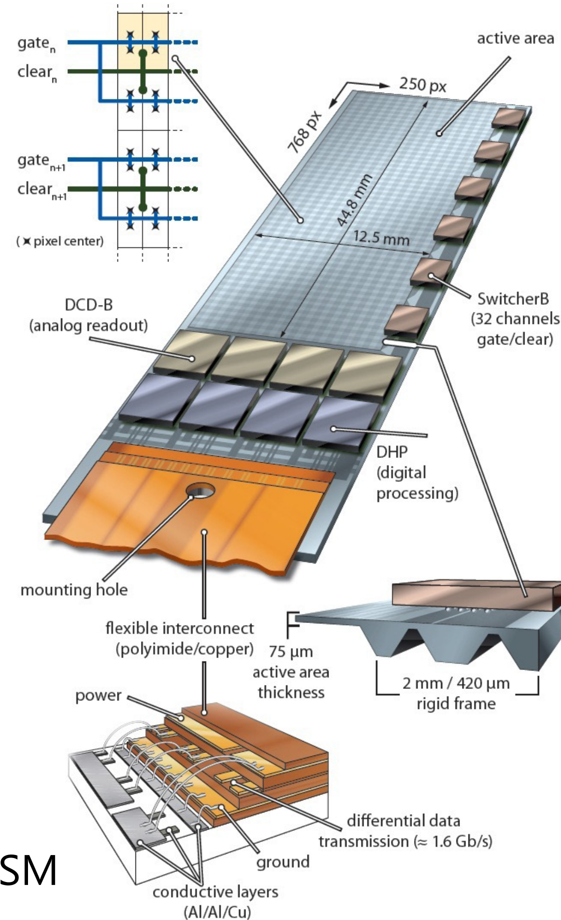
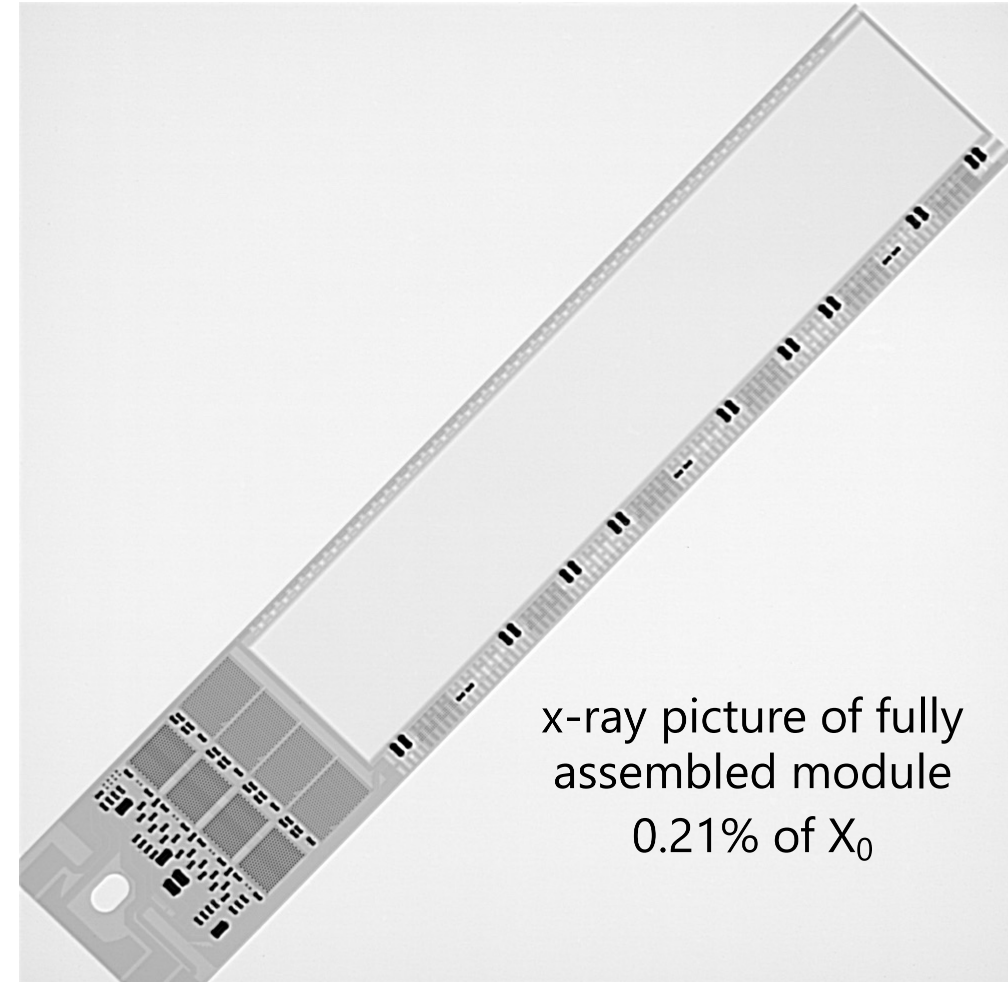
All-Silicon Module

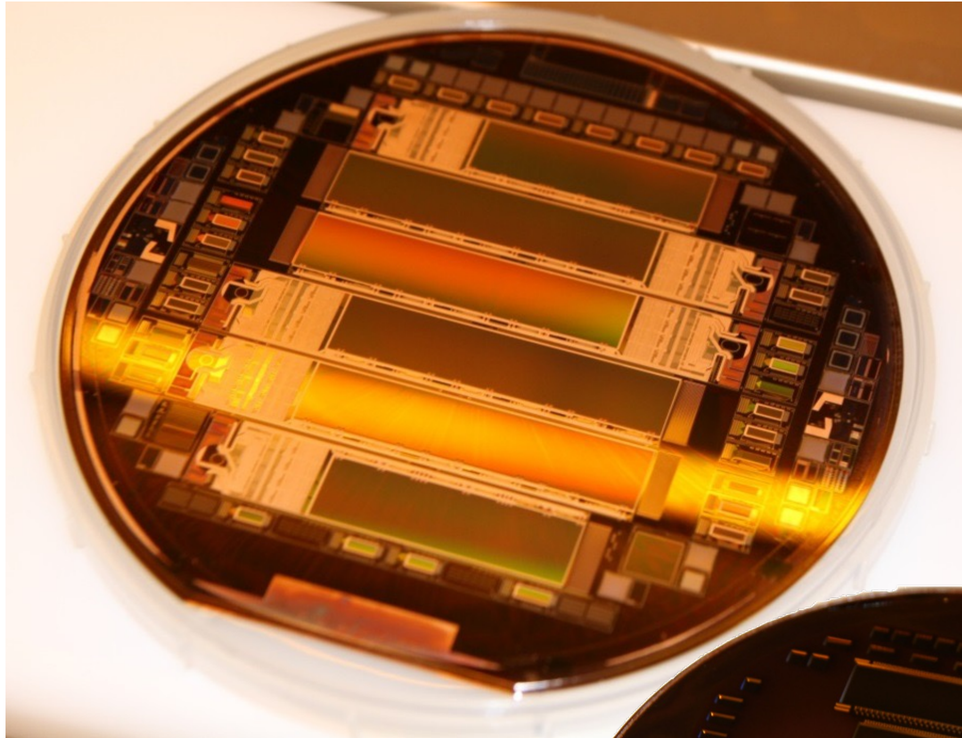


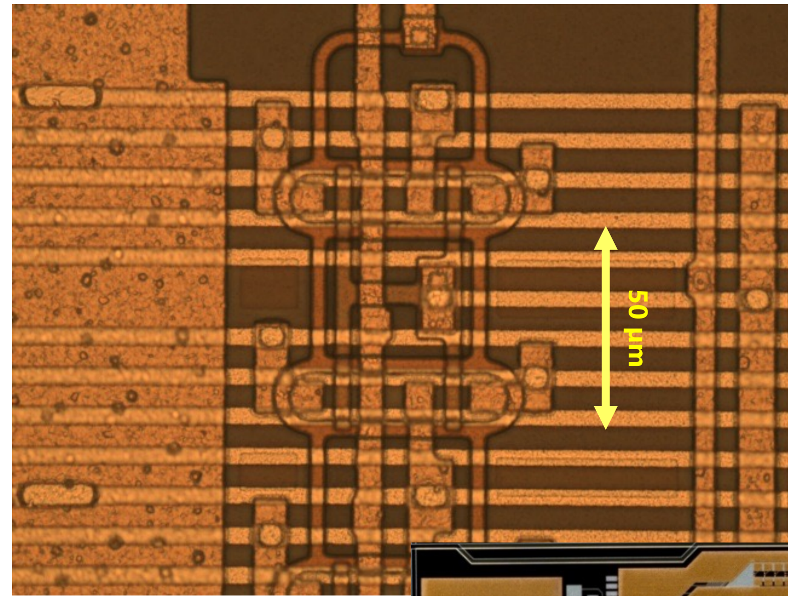


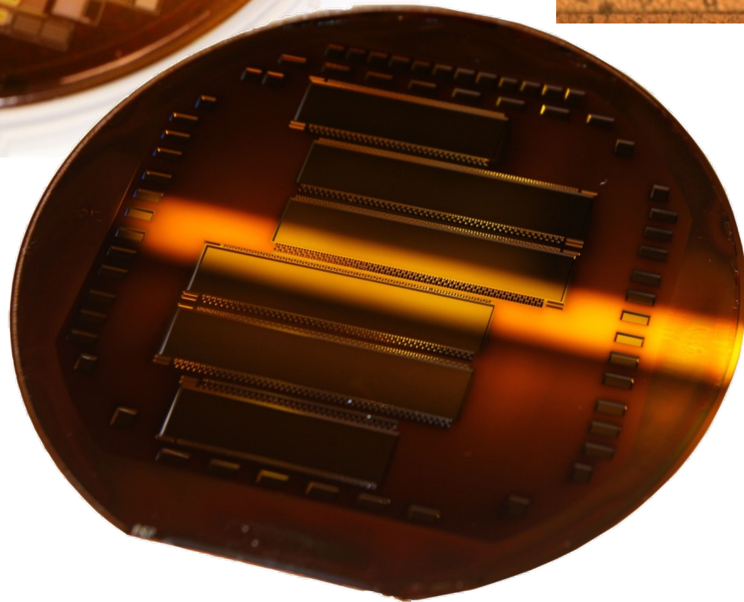
x-ray picture of fully assembled module

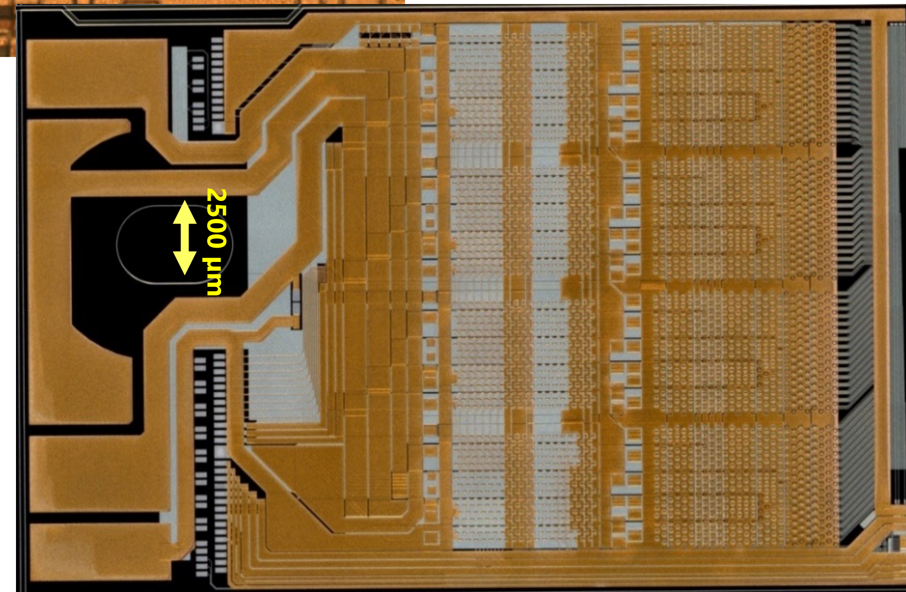
0.21% of X_0

Module design on wafer level

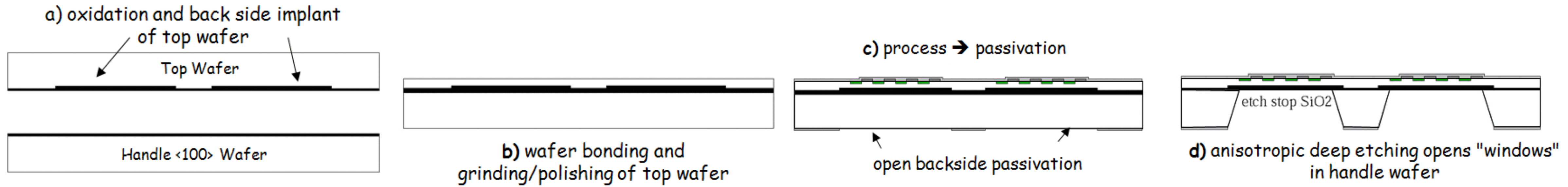


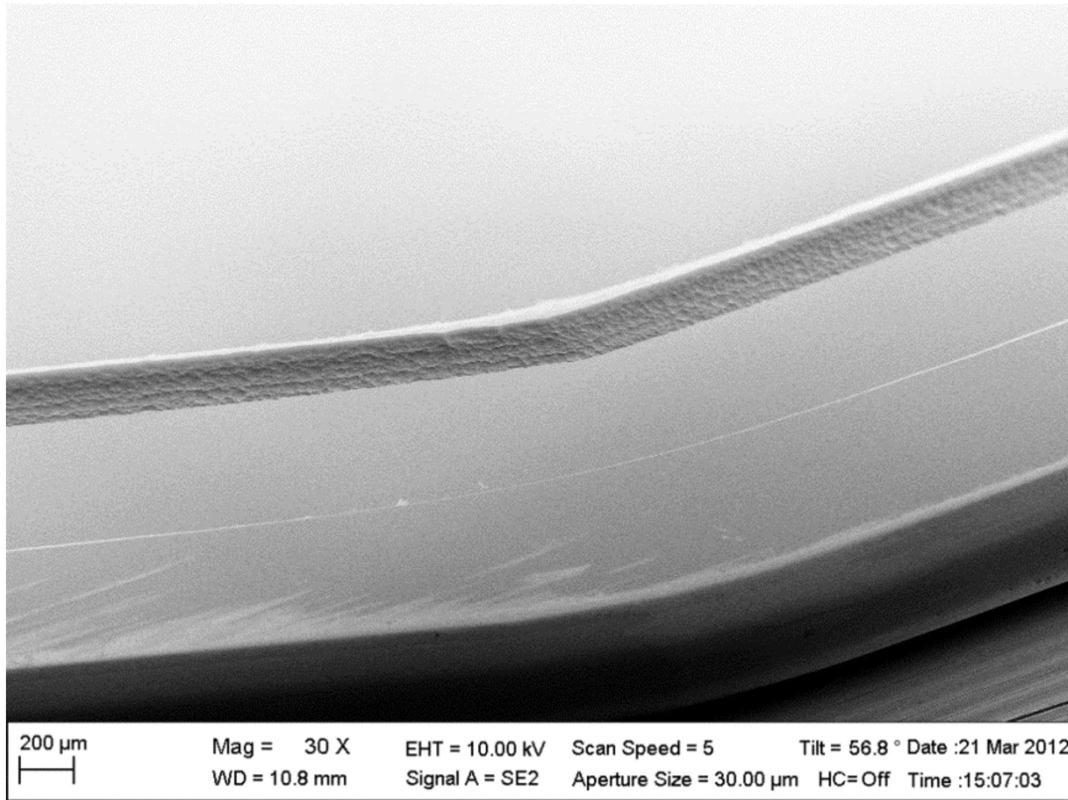


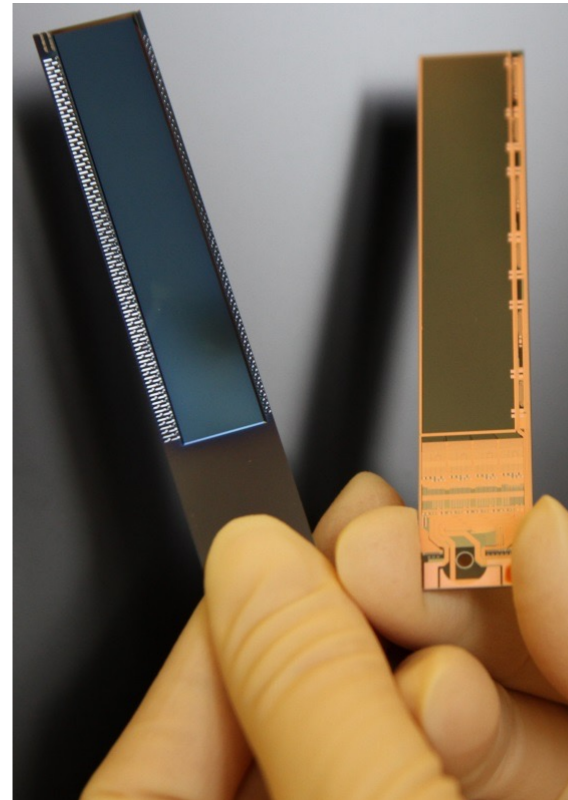




how to make thin DEPFETS





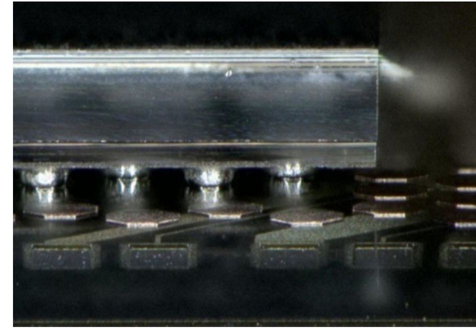


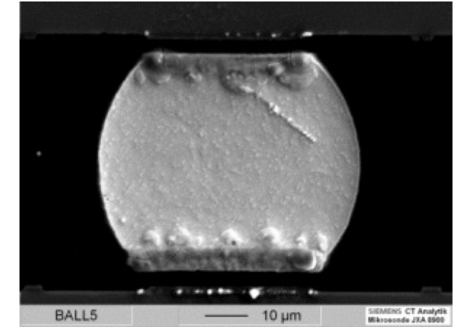
- thickness of the sensitive area is an (almost) free parameter
- thin area supported by a monolithically integrated silicon frame

module assembly overview

Flip Chip of ASICs (~240°C):

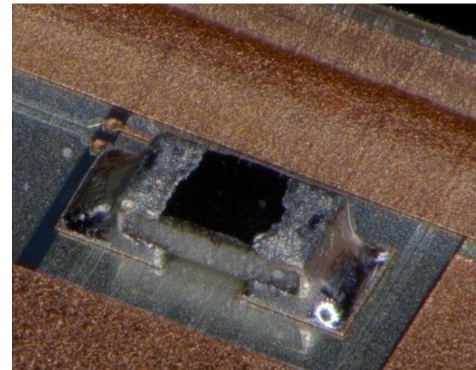
- ▷ Bumped ASICs have (almost) the same solder balls (SnAg)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ SWB bumping on chip and wafer level as post-process
- ▷ Bump bonding on customized support plates
- ▷ Initially at IZM, then at HLL

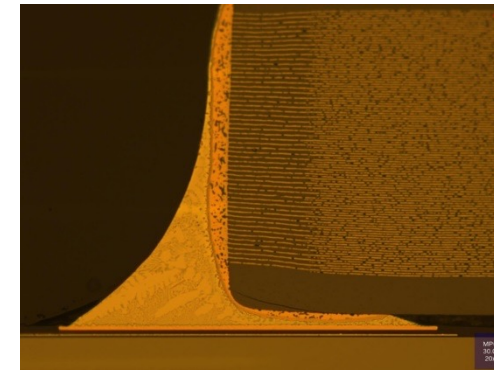




SMD placement (~200°C):

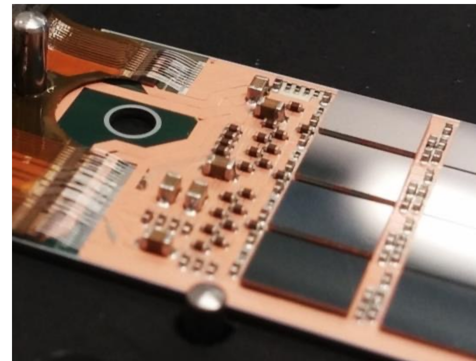
- ▷ Passive components (termination resistors, decoupling caps)
- ▷ Dispense solder paste, pick, place and reflow

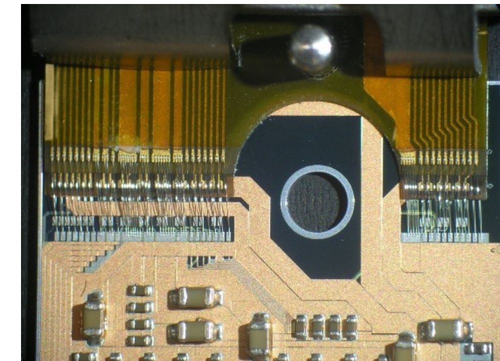




Kapton attachment (~170°C), wire bonding:

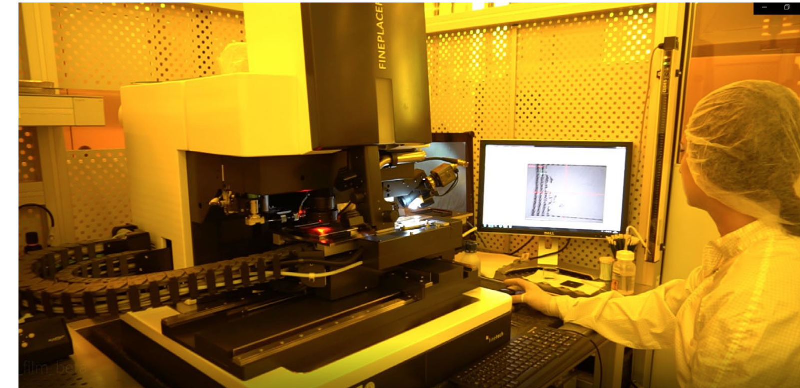
- ▷ Solder paste printing on kapton, vapor phase soldering
- ▷ Wire-bond, wedge-wedge, 32 µm Al bond wires

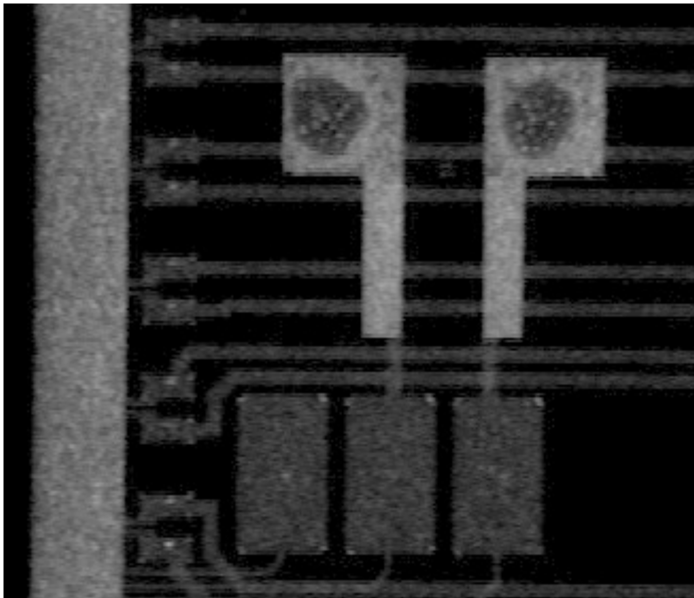


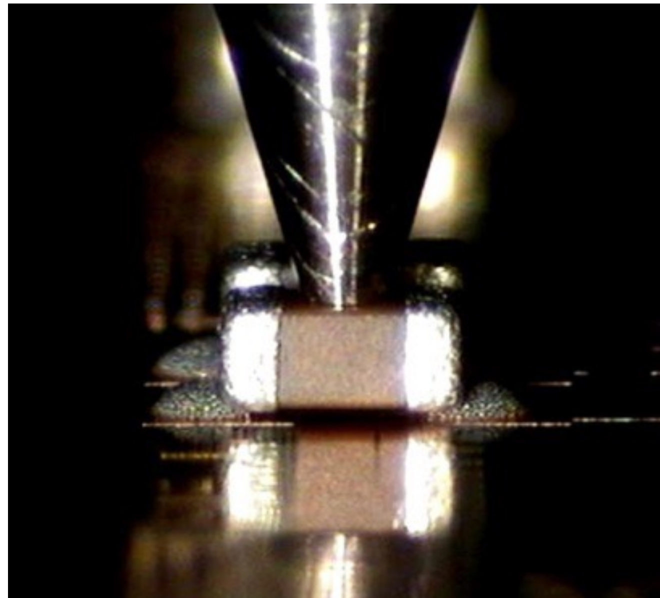


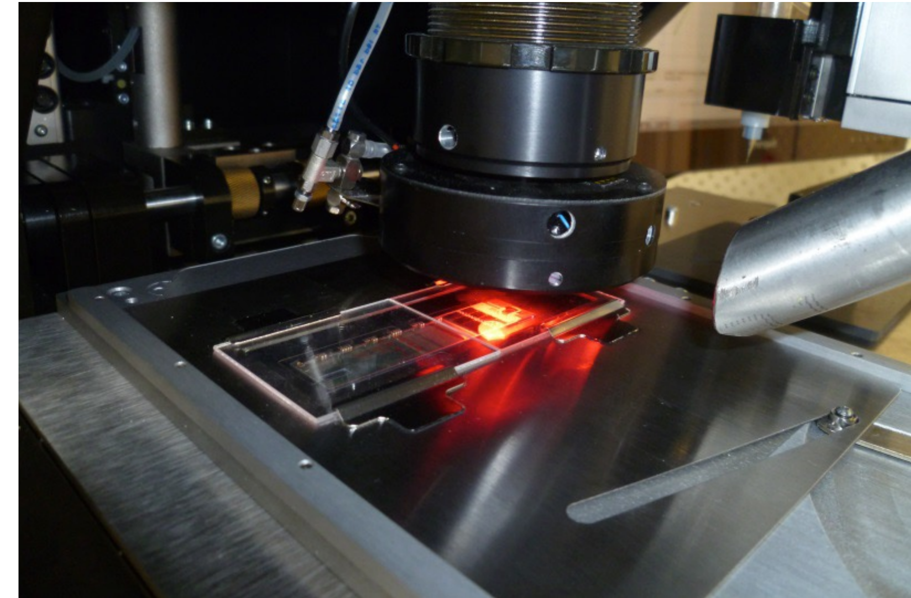
SMD assembly

- ▷ Each module has about 100 capacitors and resistors of various formats (0402, 0201, 01005)
  - ↳ Very small footprint, no screen printing of solder possible, delicate handling of module …
  - ↳ Adapted SMD technology installed at HLL
- ▷ Automated micro assembly tool, the same as for flip-chip
  - ↳ Additional dispense system
- ▷ Process flow
  - ↳ Condition module, dispense solder, place SMD parts, reflow in process chamber



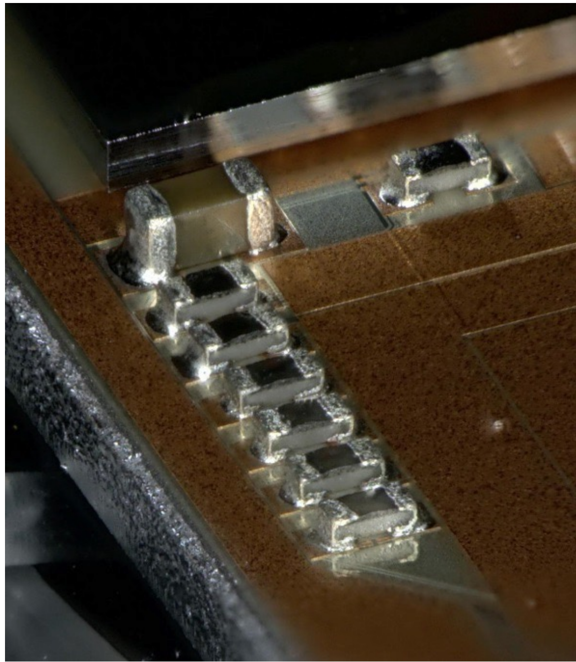


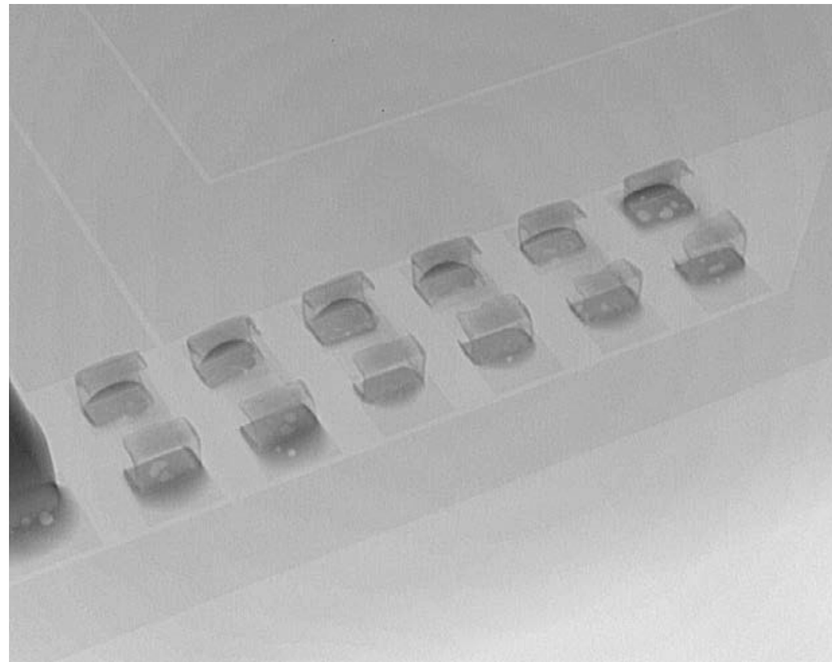




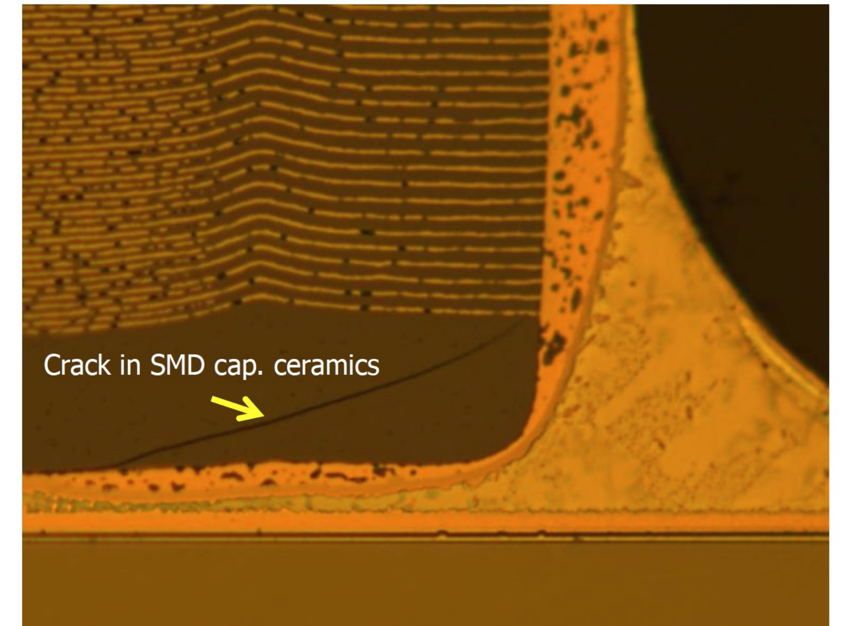
Process qualification

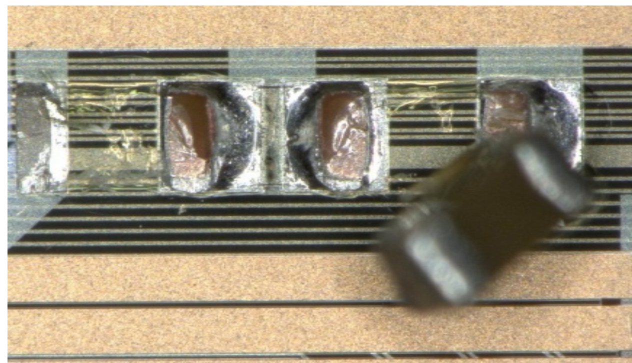
- ▷ Extensive tests and QC/QA: shear tests, cross section, metallurgy, thermal stress tests …

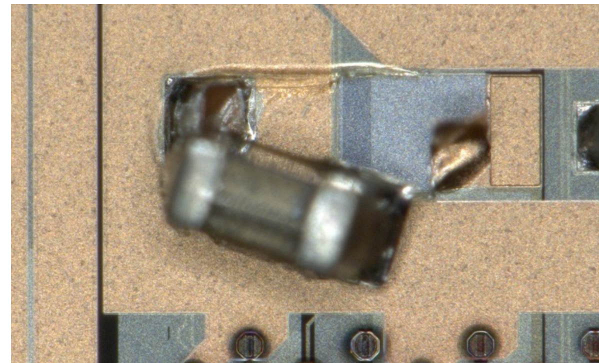


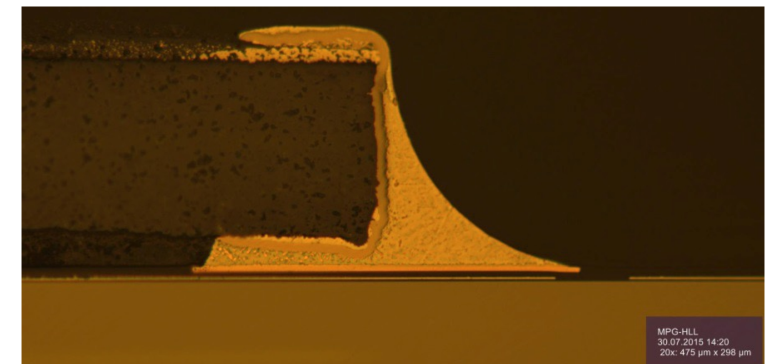


Optimization, fine tuning, reliability … → **need higher quality SMDs**

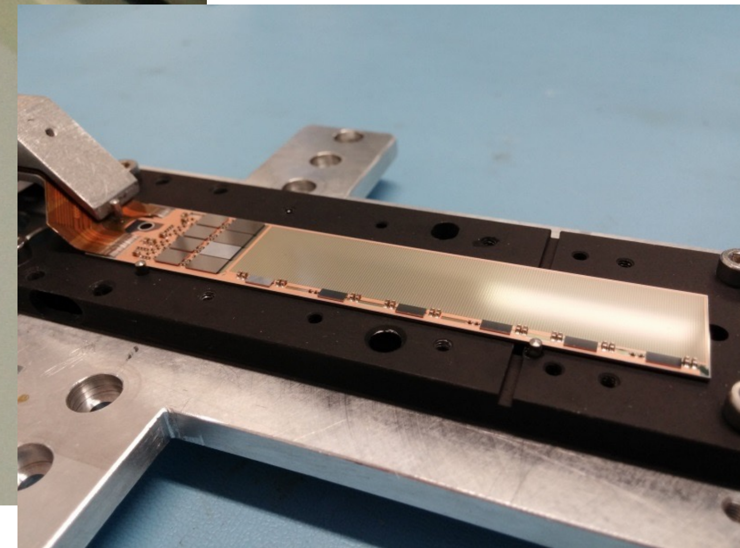






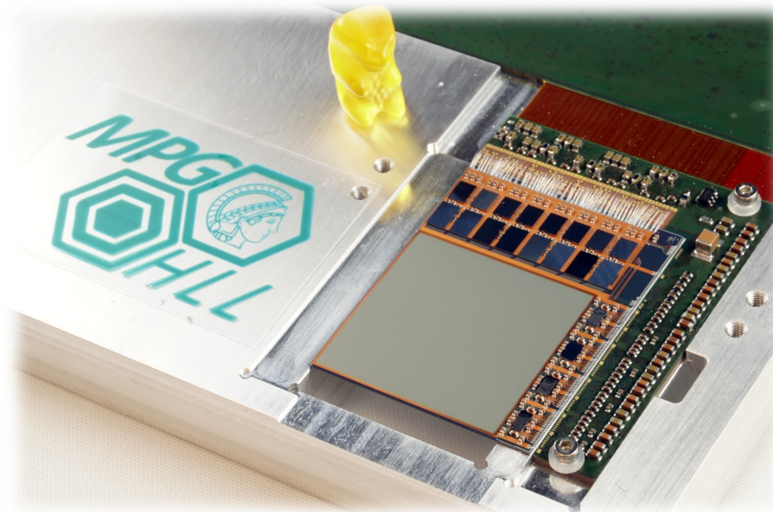


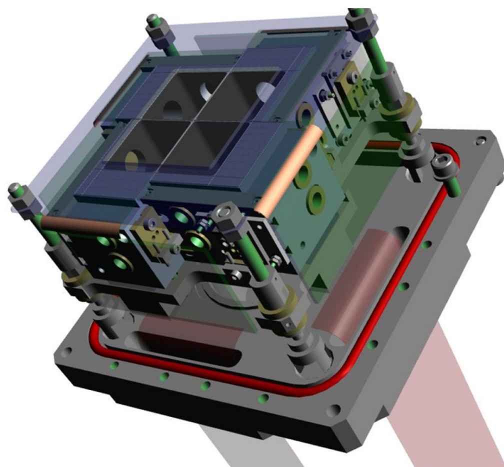
module 0

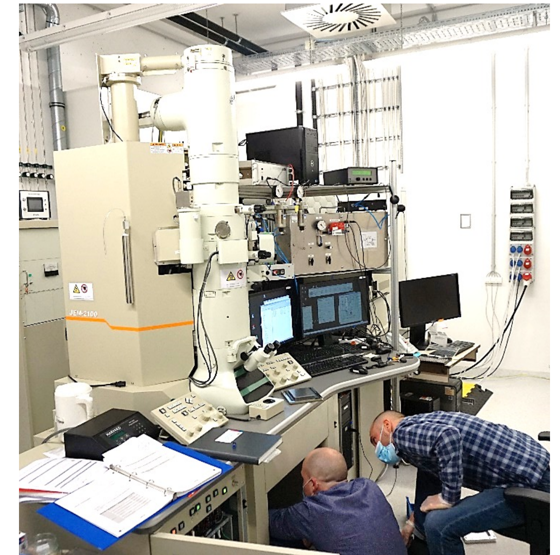


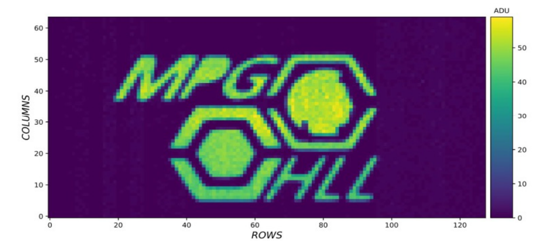
Direct Electron Detector - EDet

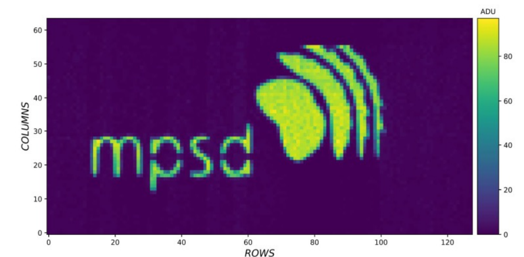
- ▷ Application of the ASM concept for a different application – direct electron detection in TEMs
  - ↳ Sensitive DEPFET area thinned to 30 µm and 50 µm



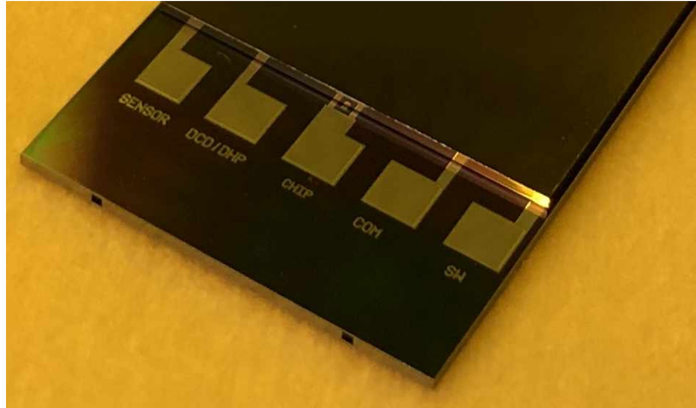


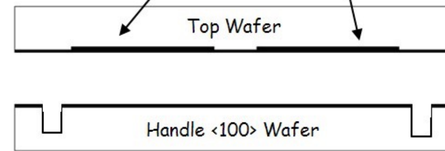


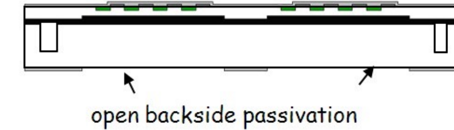


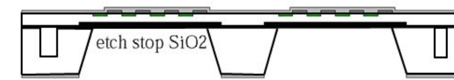


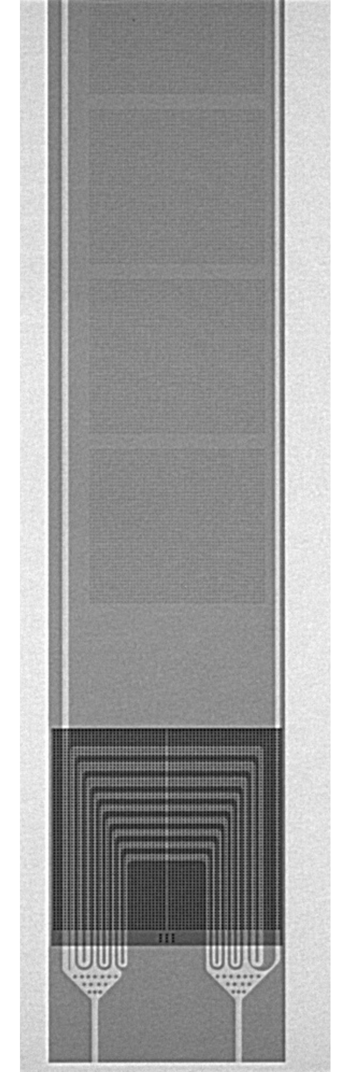
Introducing micro-channels to the ASM









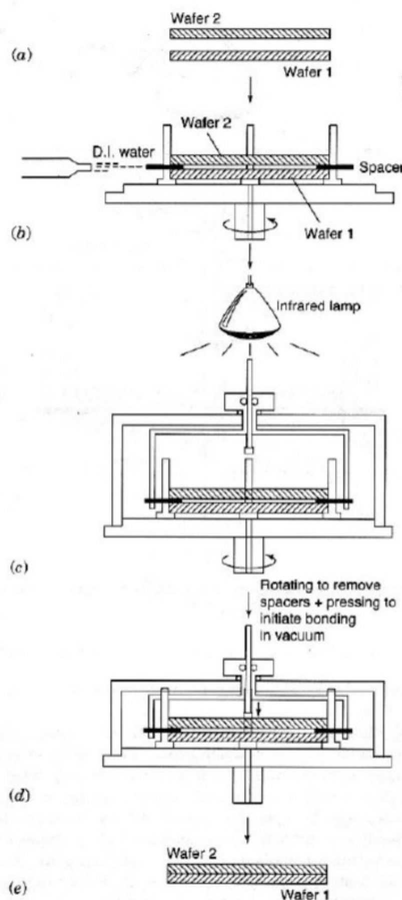


- Designed for DEPFET sensors for HEP applications
  - Back side implant first, etch channels in handle wafer
  - Wafer bonding/SOI fabrication, processing of wafers with cavities (C-SOI)

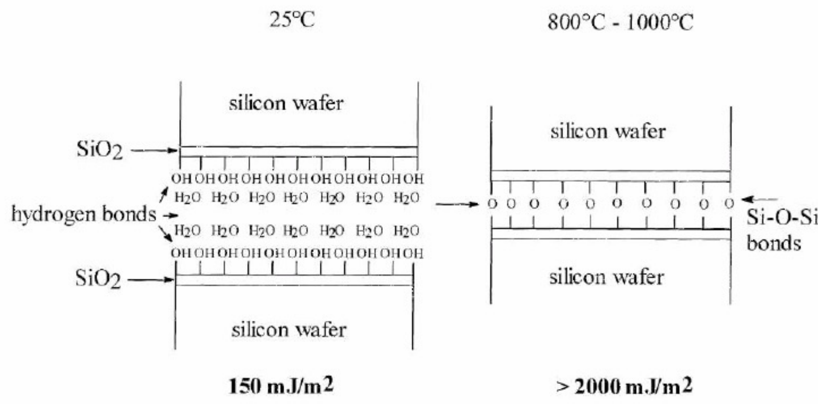
- C-SOI wafer design and fabrication specific for each project

- **More flexibility, if cavities and bonding are introduced in post-processing steps**

Direct Wafer Bonding - reminder

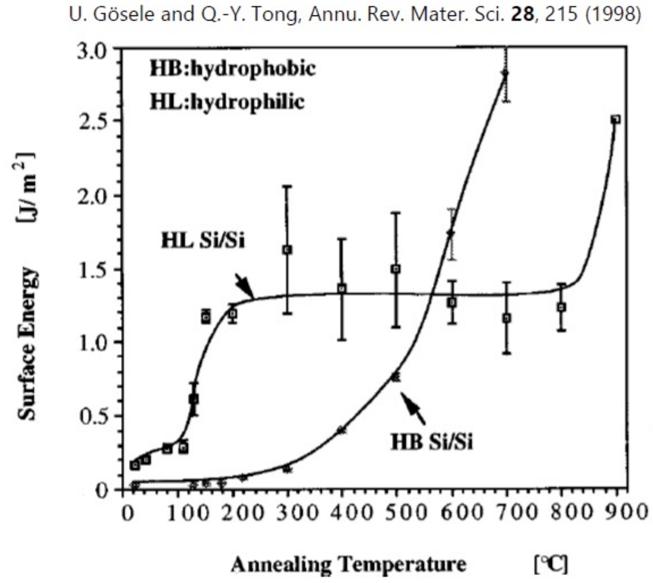


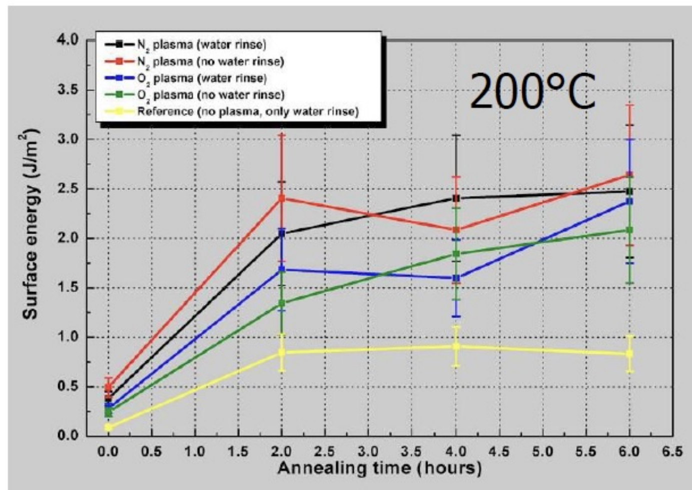
Q.-Y. Tong and U. Gösele "Semiconductor Wafer Bonding"
John Wiley & Sons, Inc.



- Relatively simple process
  - ↳ Needs just clean, (very) smooth surfaces
- High Temp. for good bonding (>2 J/m^2)
  - ↳ → not BEOL compatible
- bonding in UHV or with prior plasma treatment reduces annealing temp. well below 400°C

U. Gösele and Q.-Y. Tong, Annu. Rev. Mater. Sci. **28**, 215 (1998)

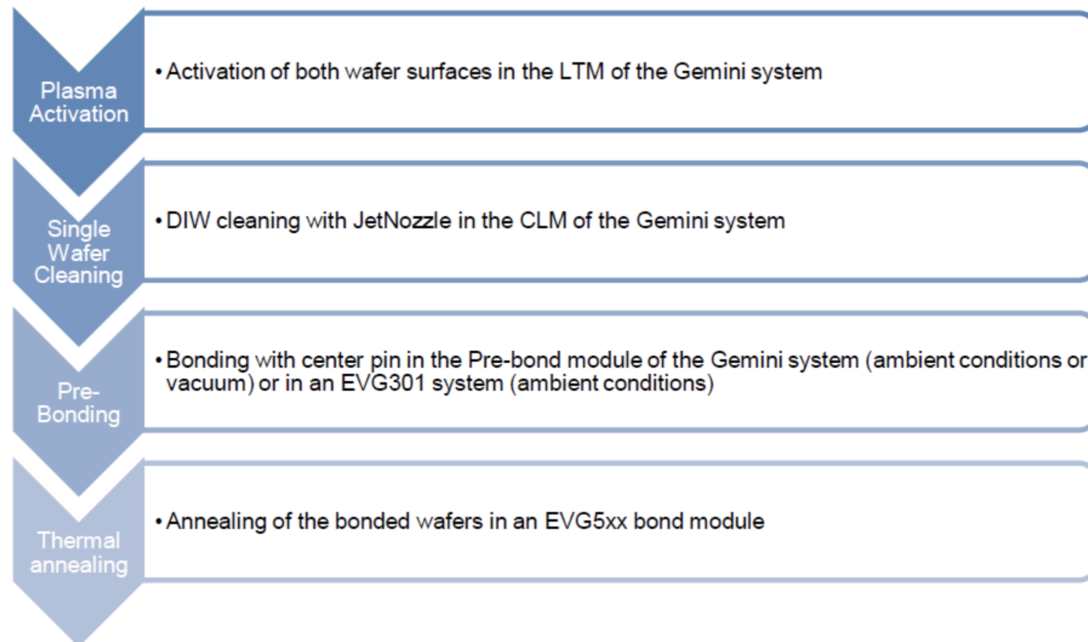


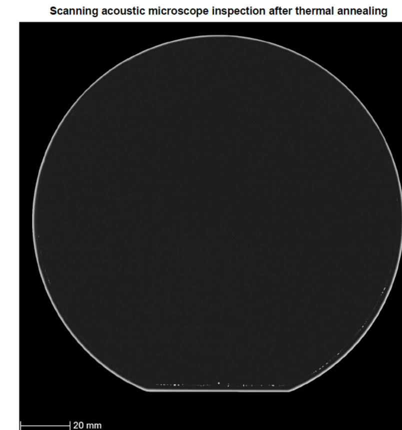


"Plasma Activation – An Enabling Technology for Wafer Bonding",
Eric F. Pabo, EV Group, Semicon West 2010

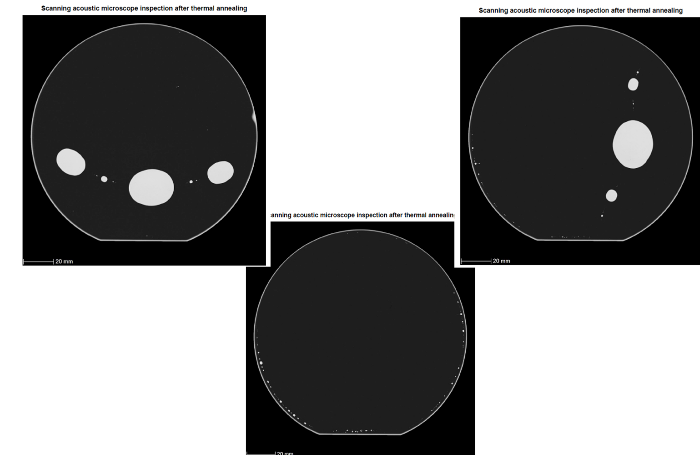
Low temperature bonding tests at EVG, Austria

- 1st DWB tests at equipment manufacturer EVG very successful
  - ↳ Focused on bonding of implanted oxide, tests still yielded surface energies of about 1 J/cm^2
- 2nd round to optimize surface energy at low annealing temperature
  - ↳ Twelve 6″ DSP FZ wafer pairs prepared at HLL (oxidation, cleaning)
    - ↳ six pairs as path finder for best parameter set (plasma/atmosphere/temperature)
    - ↳ six pairs to confirm and increase statistics





- 9/12 bonds look like this

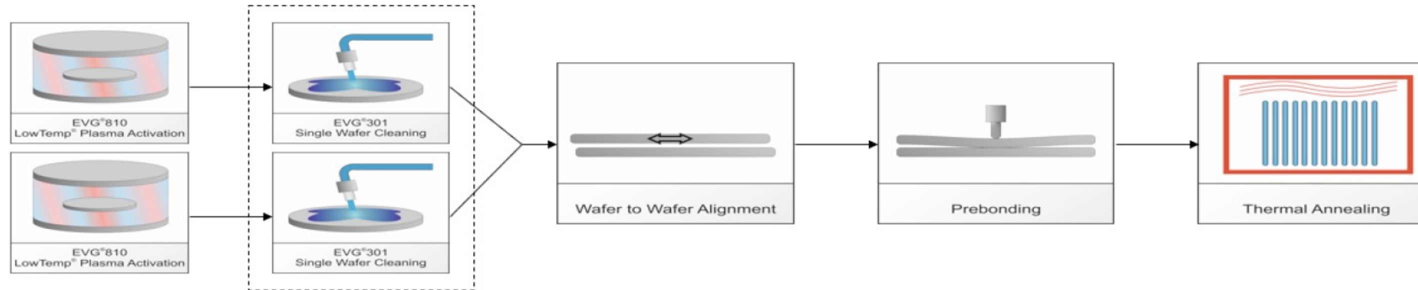


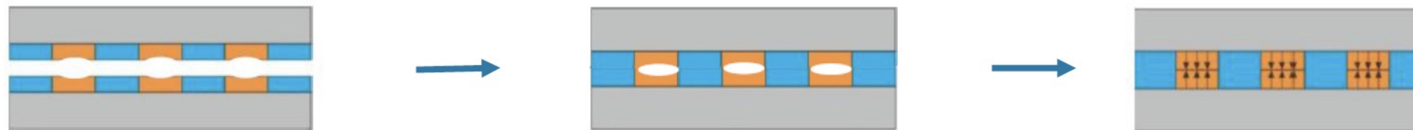
- 3/12 bonds with edge voids and larger area voids due to particles or surface quality variations

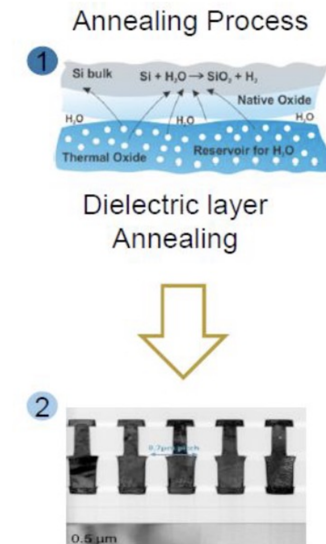
- **Result: reliable, reproducible, and wide process window with T<300 °C and surface energy > 2 J/cm^2**

Wafer bonding – more general

- Very versatile basic process step for (heterogenous) integration
  - Wafer-to-wafer or collective chip-to-wafer bonding
    - Si to Si, Si to other materials like compound semiconductors, e.g.
    - “Hybrid bonding”: embedded Cu-Cu bonds for electrical interconnections



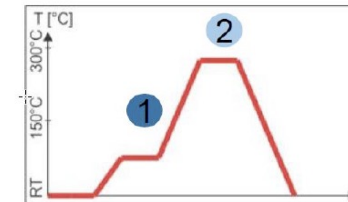




Wet cleaning and plasma activation are applicable for surface preparation.

Wet cleaning can include the use of chemicals for metal oxide removal

Wafers will be aligned using F2F optical alignment. Once aligned, wafers will be contacted at room Temperature.



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Wafer bonding process line (6" and 8") at HLL

- Plasma activation: EVG810

- Cleaning/prep: EVG301

- Direct and adhesive bonding: EVG501
  - ↳ SOI, C-SOI

- Hybrid Bonding: EVG Smart-View
  - ↳ Aligned W2W bond

- Wafer preparation
  - ↳ "Bosch" Process for C-SOI
  - ↳ Post-processing: RDL on ASIC and sensor wafer
  - ↳ CMP
  - ↳ Re-constitution of Wafer from KGDs

- **Contract with tool manufacturer for equipment supply and process support in preparation**

In Summary

- Based on the experience with the all-silicon module for Belle II PXD, the HLL is extending this technology to other applications
  - ↳ detectors for HEP, photon science in general, low-energy particle detection
  - ↳ photonic applications, quantum computing

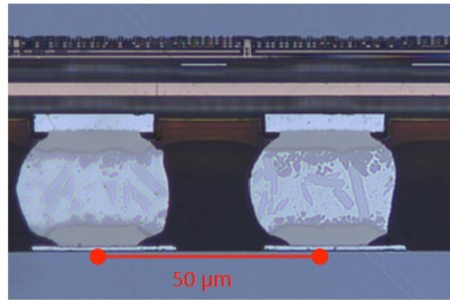
- The vision is heterogeneous integration of very different technologies on support silicon (active or passive)
  - ↳ Sensor + CMOS + Photonics 2.5D and 3D integrated

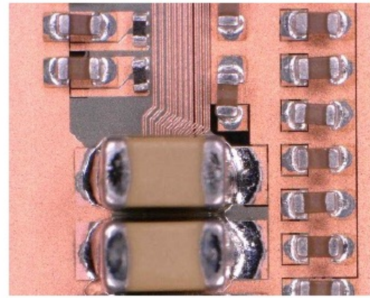
- Additional post-processing tools and technologies for 6″ and 8″ wafers are being installed in the new clean room
  - ↳ ICP-DRIE, CMP (not presented here)

- Key technology is wafer bonding at BEOL compatible temperatures
  - ↳ Direct bonding, adhesive bonding
  - ↳ Hybrid bonding allowing for advanced fine-pitch vertical interconnection

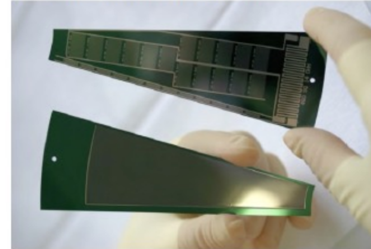
Backup

A few few pictures from past projects – more to come!



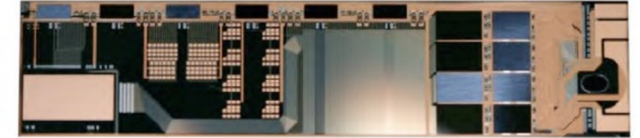


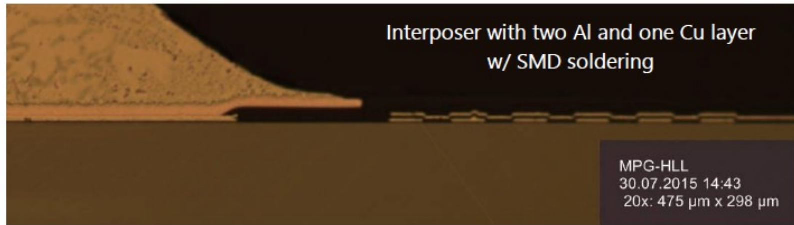
Thermo-mechanical modules

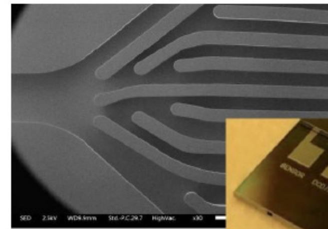


Thin Si with integrated heaters

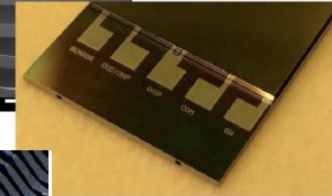
Si interposer /w flip-chipped ASICs and SMD passives



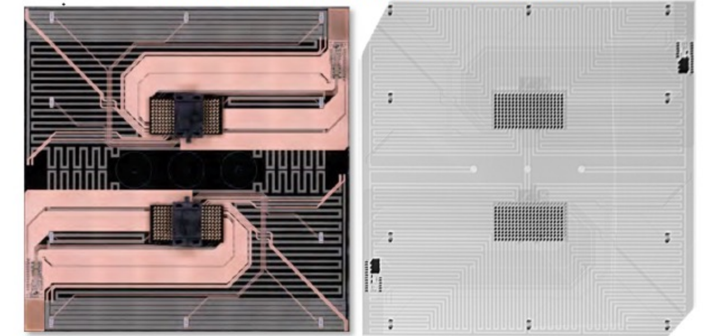




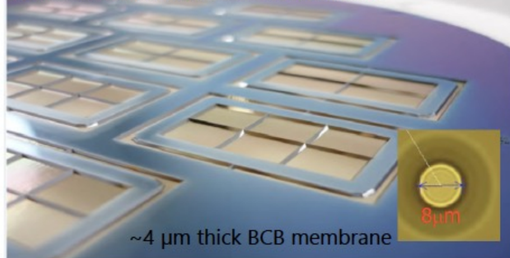
Micro-channel-cooling

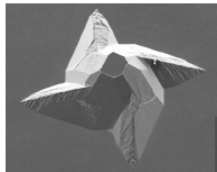


Interposer with integrated cooling channels

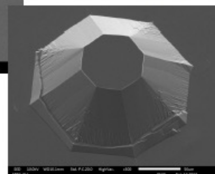


Perforated thin membranes as sample holders

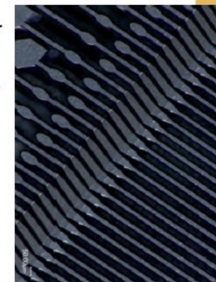


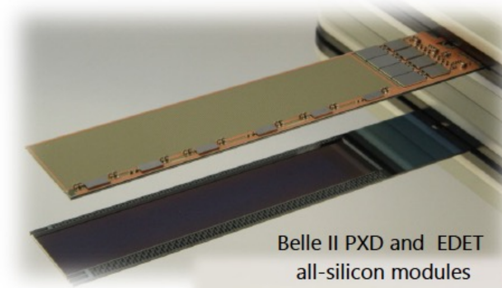


High purity Si pins
as crystal holders

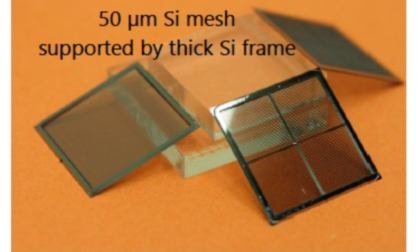


Metallization over
extreme
topography
"Molecular traps"

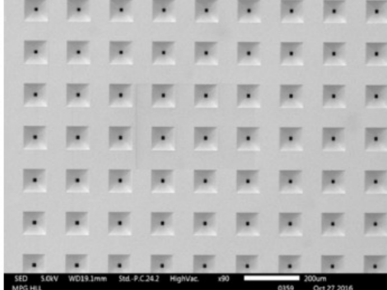


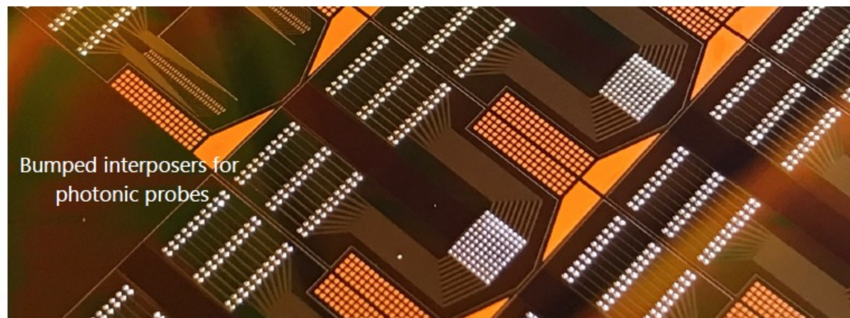


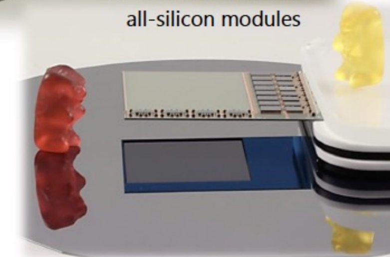
Belle II PXD and EDET
all-silicon modules

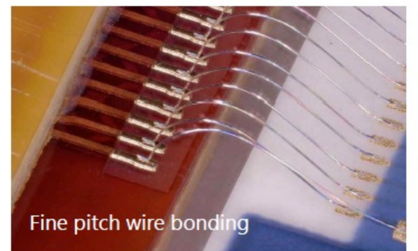


Sample holders for FEL studies









The way forward: **overview**

- ▷ Extend sputtering capability on existing sputter system
  - ↳ targets are easy to exchange
    - ↳ → new metals possible
  - ↳ replace 2/4 DC sputter guns with RF biased ones
    - ↳ → sputtering of isolators (SiO2, Al2O3 ..)
  - ↳ software upgrade for co-sputtering and reactive sputtering

- ▷ Improve lithography capability
  - ↳ Use of e-beam lithography system installed at MQV partners
  - ↳ HLL contribution: installation and qualification of required photo resist systems suitable for e-beam

- ▷ Extend structuring capability
  - ↳ Installation of ICP-DRIE for silicon
    - ↳ TSV, Si wave guides

- ▷ Extend interconnect capabilities and post-processing of ASICs and/or PICs
  - ↳ Install CMP of SiO2 and metals as preparation for wafer bonding
  - ↳ Install and W2W and C2W direct and hybrid bonding
    - ↳ Low temperature bonding <350 °C mandatory

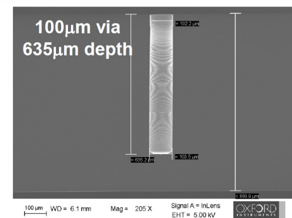
The way forward: **ICP-DRIE "dry etching"**

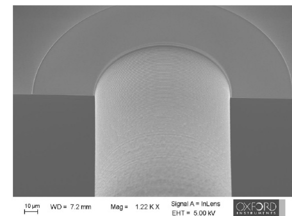
- Oxford Instruments Estrelas System, single wafer etcher for up to 8" wafers
  - ↳ Hook-up, process installation, and commissioning ongoing → end of 2025
- Main process modules
  - ↳ Deep Si etch ("Bosch Process")
    - ↳ TSV, fluidic channels, large area partial thinning of wafers, also as post-process option
  - ↳ "mixed gas" process
    - ↳ Shallow Si etching with very smooth side walls for Si wave guides

3. Bosch: TSV etching

- Advanced packaging applications
  - ~5% Si exposed on a 500 μm thickness wafer
  - Use SiO_2 as a stop layer

Parameter	a	b
Process Chemistry	SF_6-C_4F_8	SF_6-C_4F_8
Wafer size (mm)	**150**	**200**
Exposed area (%)	5	5
Clamping method	ESC	ESC
Via size (μm)	100	100
Depth (μm)	500	500
Etch rate (μm/min)	> 7	> 6
Selectivity to PR mask	> 70	> 70
Selectivity to SiO_2 mask	> 120	> 120
Profile control (°)	90±1	90±1
Bosch scallop (nm) (peak to peak)	< 200	< 200
Uniformity within wafer (±/%)	< 3	< 3





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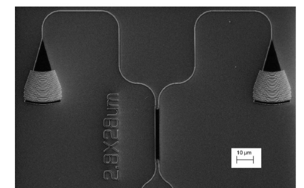
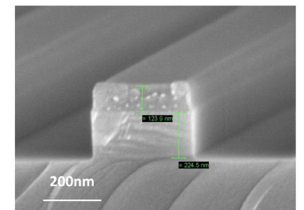
4. Mixed gas Si etching

- Si waveguide applications
  - SOI wafers
  - Etch a top Si layer of 220nm thickness
  - Smooth sidewalls and accurate control

Parameter	a	b
Process Chemistry	SF_6-C_4F_8	SF_6-C_4F_8
Wafer size (mm)	**150**	**200**
Exposed area (%)	25	25
Clamping method	ESC	ESC
Trench size (μm)	5	5
Depth (nm)	220	220
Etch rate (nm/min)	> 50	> 40
Selectivity to PR mask	> 1.5	> 1.5
Selectivity to SiO_2 mask	> 2.5	> 2.5
Profile control (°)	90±2	90±2
Added sidewall roughness (nm)	< 2 (rms)	< 2 (rms)
Uniformity within wafer (±/%)	< 5	< 5





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