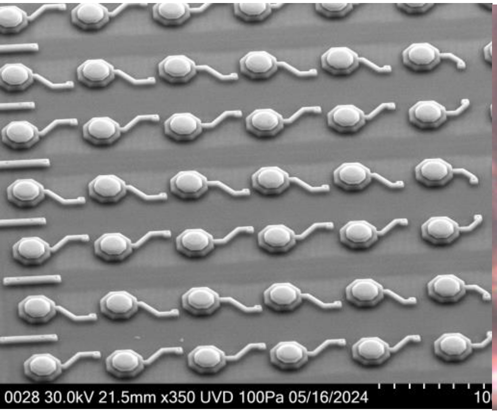
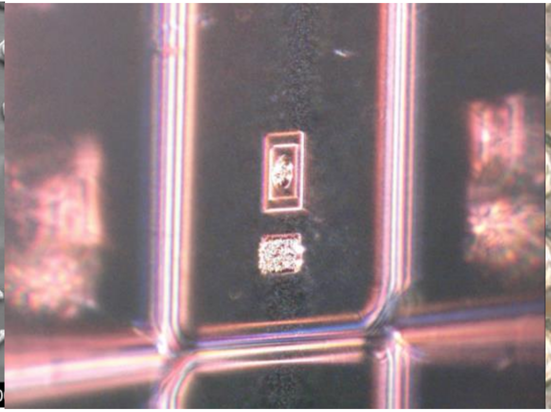
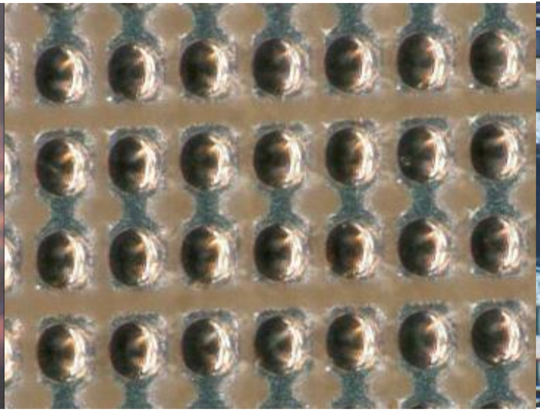
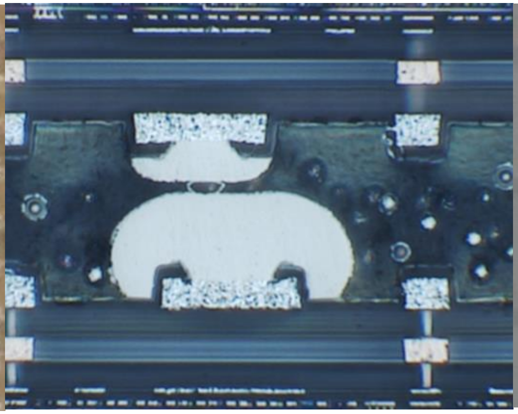
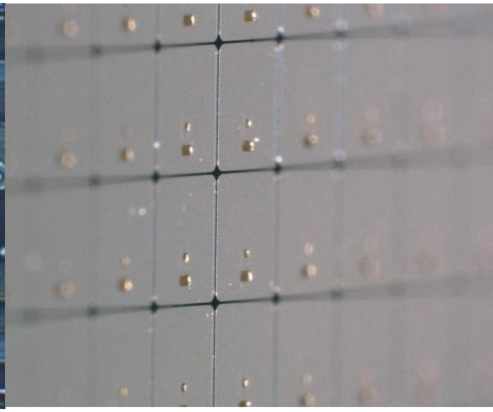
Development of an in-house Ni/Au plating process for pixel-detector hybridisation and module integration



DRD3 Week: Solid State Detectors R&D

19/06/2024

Haripriya Bangaru[1], Justus Braach[1,2], Giovanni Calderini[3], Dominik Dannheim[1], Ahmet Lale[1] , Rui De Oliveira[1], Mateus Vicente Barreto Pinto[4], Janis Viktor Schmidt[5], Peter Svihra[1], Matteo Centis Vignali[6], Alexander Volker[5], Xiao Yang[1]

1: CERN 2: Hamburg University 3: LPNHE-Paris, Centre National de la Recherche Scientifique
4: Universite de Geneve 5: KIT - Karlsruhe Institute of Technology 6: FBK

Motivation

Development of an in-house module hybridization technique in two main steps:

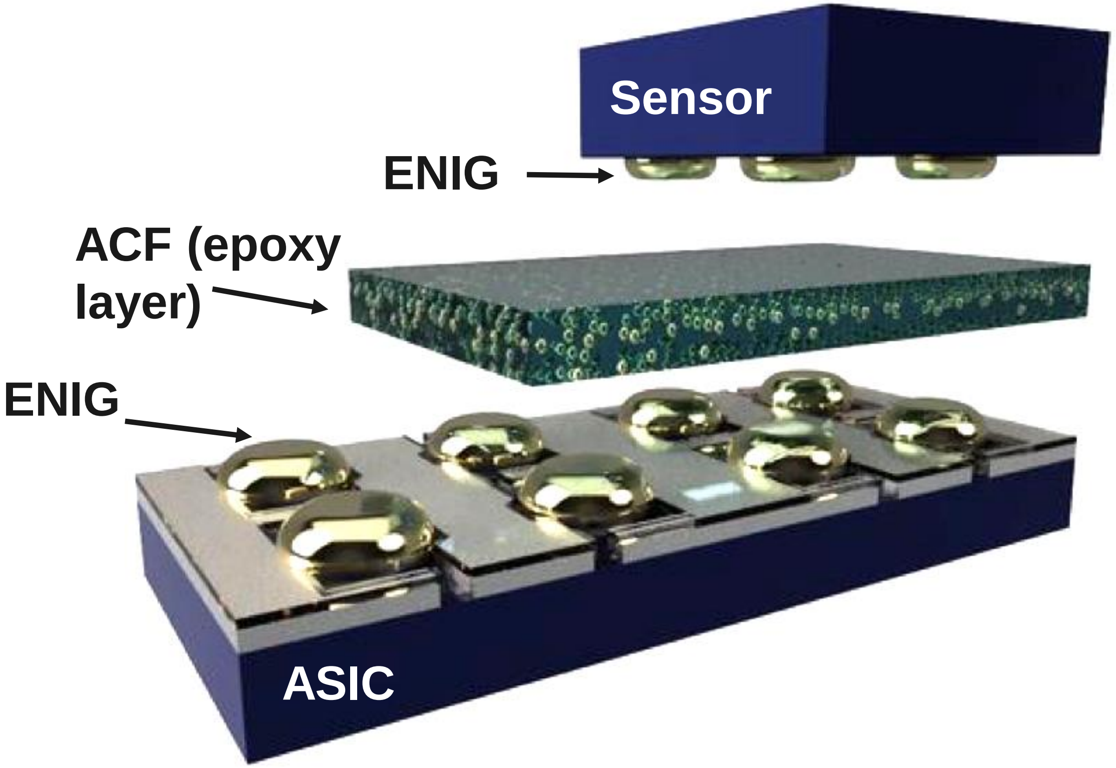
1. Creation of bumps on the pads of sensor and ASIC with ENIG plating
2. Flip-chip assembly with an adhesive layer between the chips

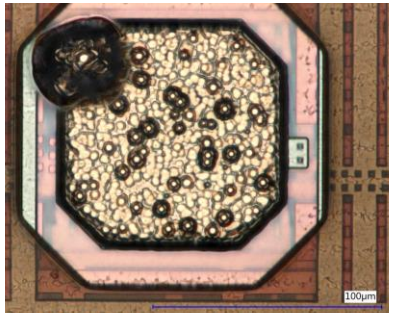
Basis for interconnection technologies

- Pad metallisation is required for most interconnection technologies
- **For adhesive-based bonding:** Need for sufficiently large cavity volume between sensor and ASIC after bonding to fit excess adhesive
- Deposition height variable for different applications

In-house production

- Single die processing possible
- Short turnaround time
- Quick adjustments possible
- Quality control
- Maskless, cost-efficient



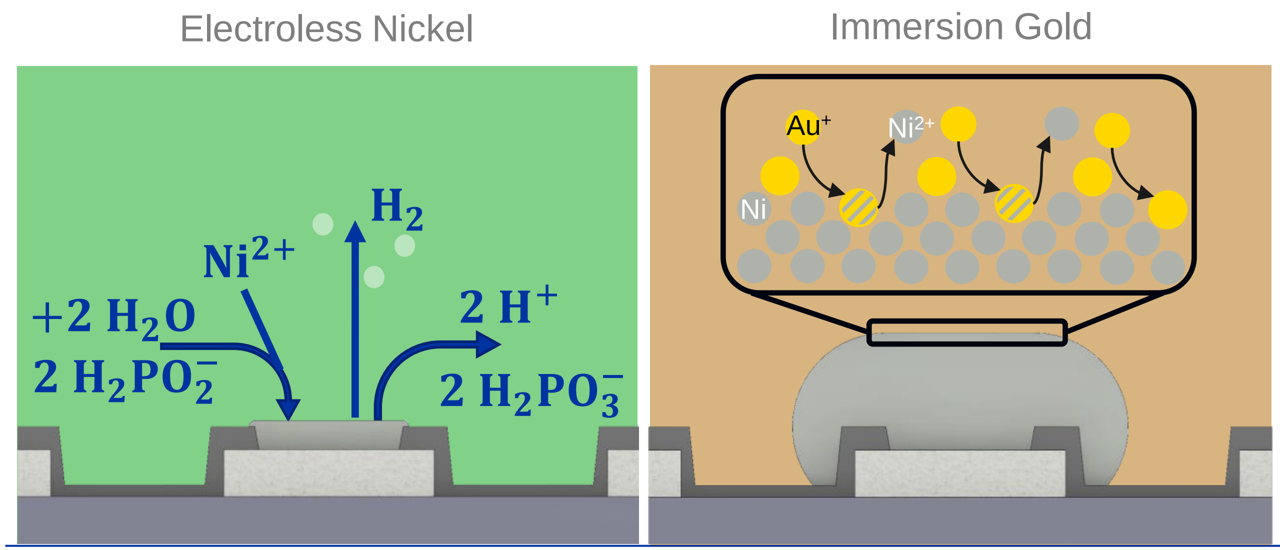


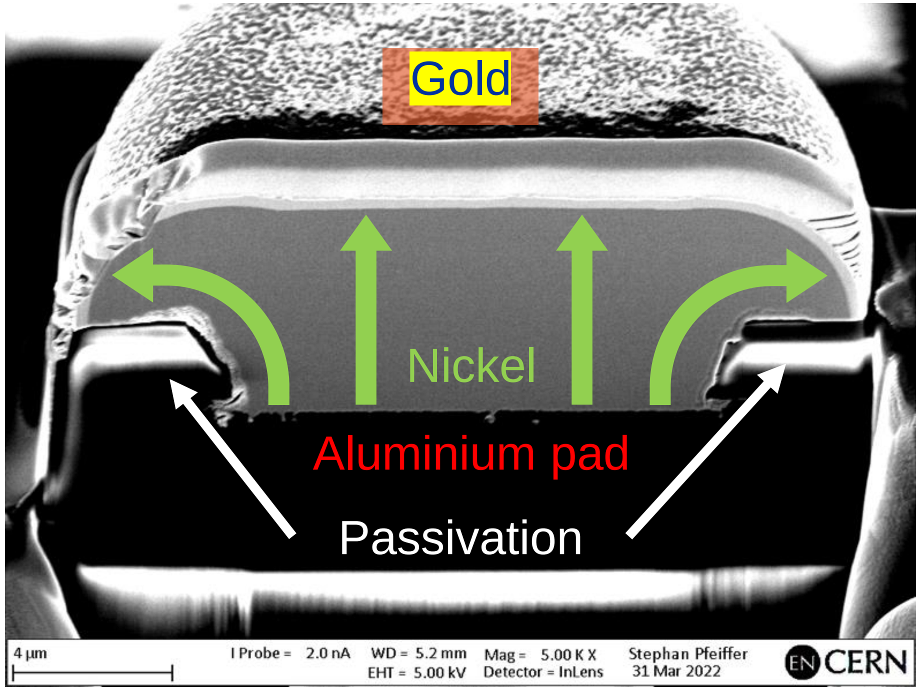
Insufficient quality from external producer

Introduction

3 main steps for Electroless Nickel Immersion Gold (ENIG) plating:

1. Pre-treatment and zincation of the aluminium pad
2. Electroless Nickel deposition (creation of the bump)
   - Self-catalytic reaction on pad surface
3. Immersion Gold
   - Corrosion protection, bondable surface, very thin layer (< 1 µm)

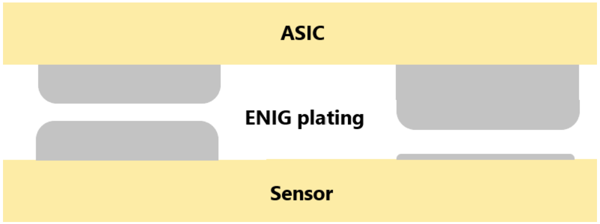


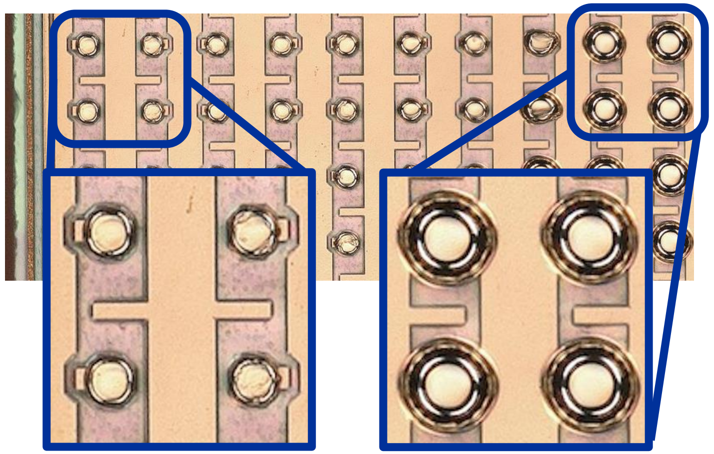


FIB cross-section of an ENIG bump on an aluminium pad

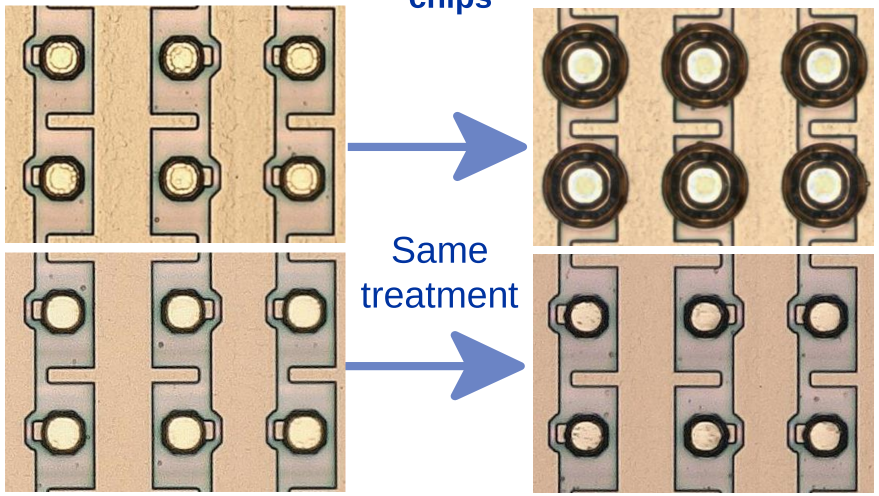
Challenges of initial platings

Uniformity of nickel bump height across the chips (especially at the edge of the chip)

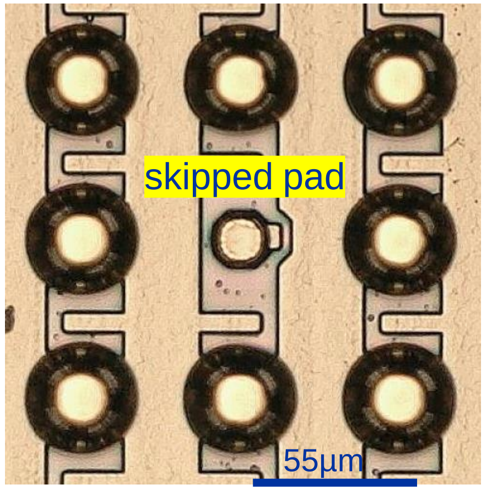




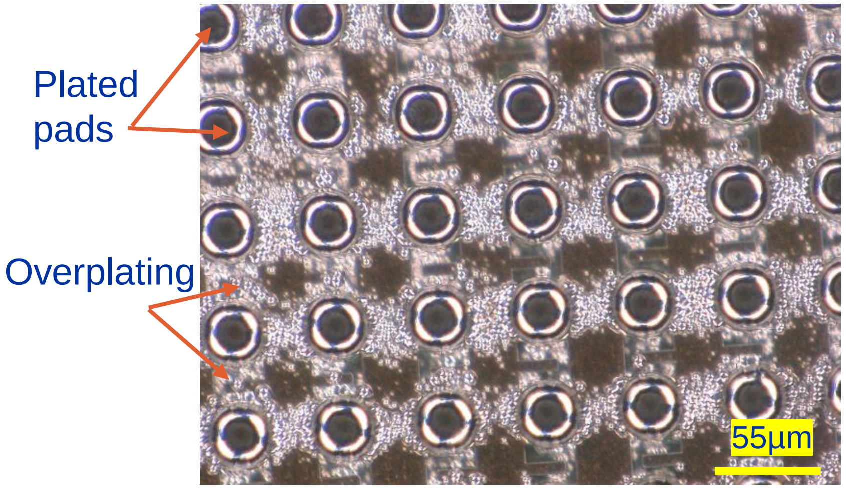
Deposition reproducibility on different chips



Non-plated or skipped pads/areas



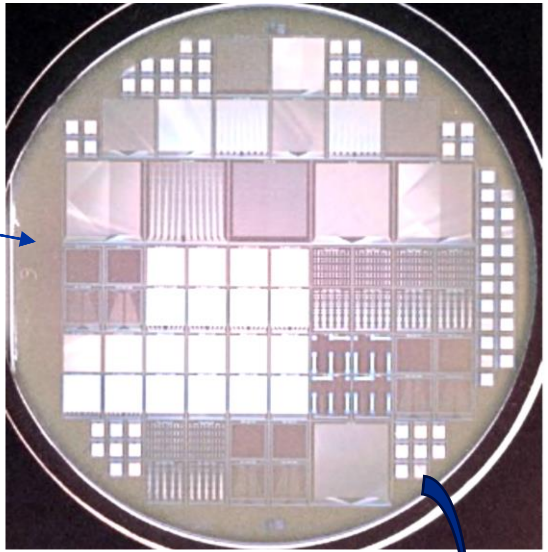
Overplating (plating on areas that should not be plated)



Achieve ENIG plating on high connection density chips (ex: CLICpix2, 12µm pads; 25µm pitch) !!

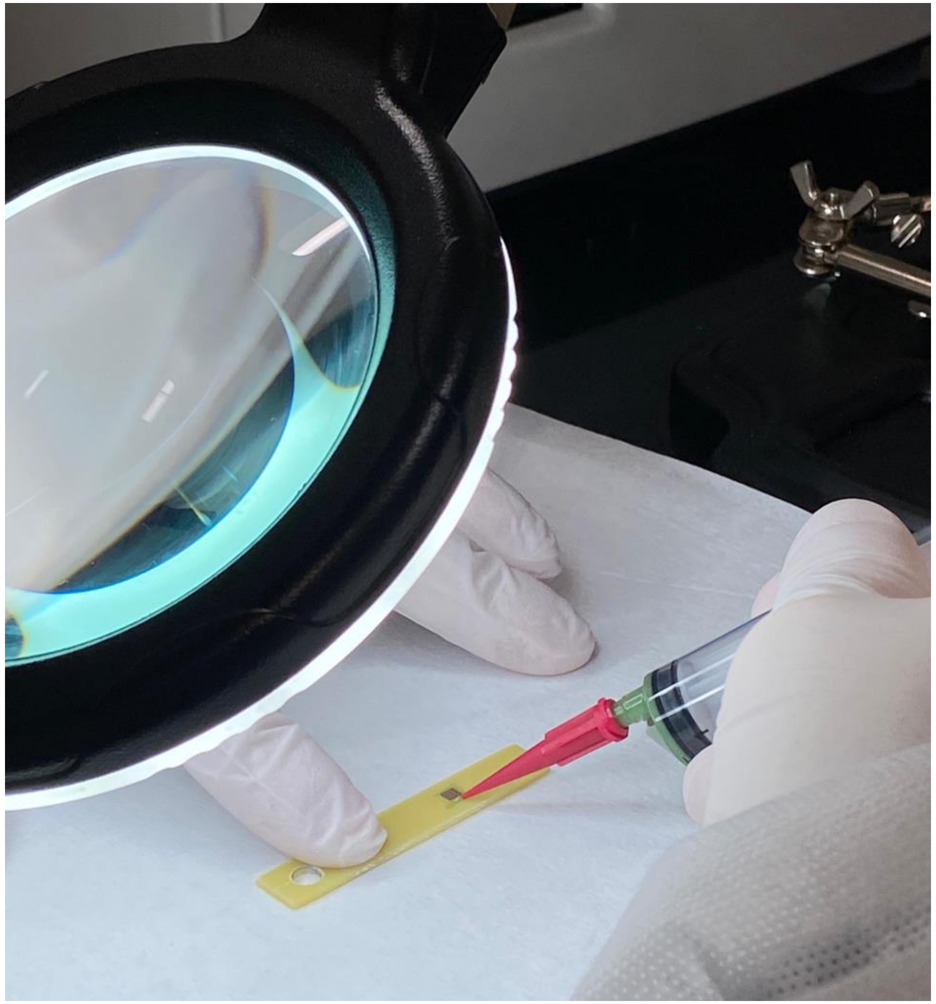
Sample preparation

Daisy chain devices (glass wafer)

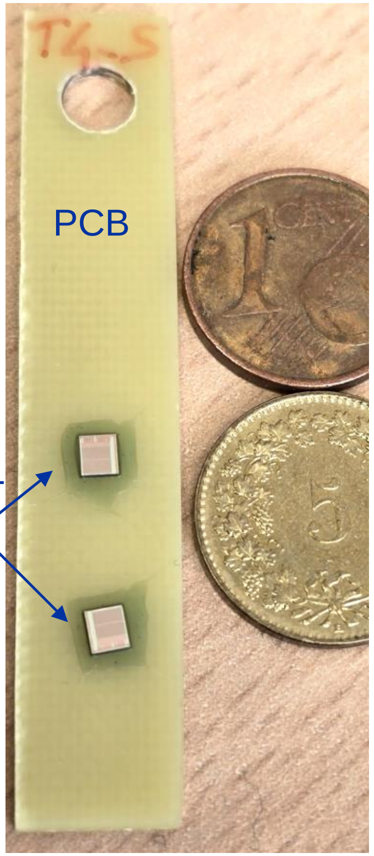


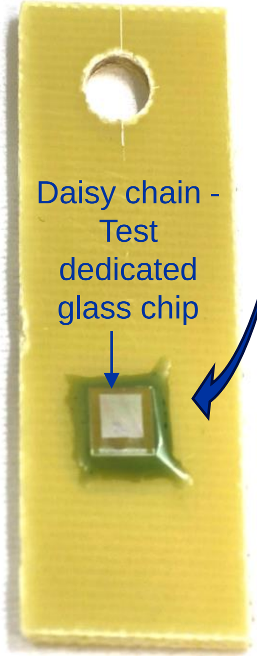
Samples preparation steps:

- Cut PCB (FR4) pieces
- Drill PCB
- Clean PCB
- Glue the Chip on the PCB



TIMESPOT chips

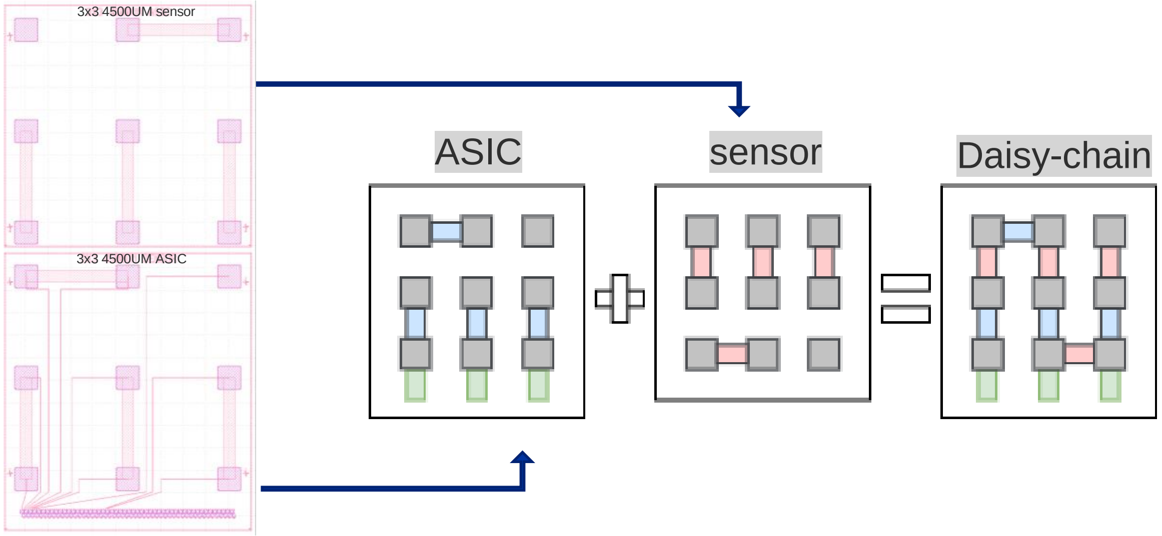




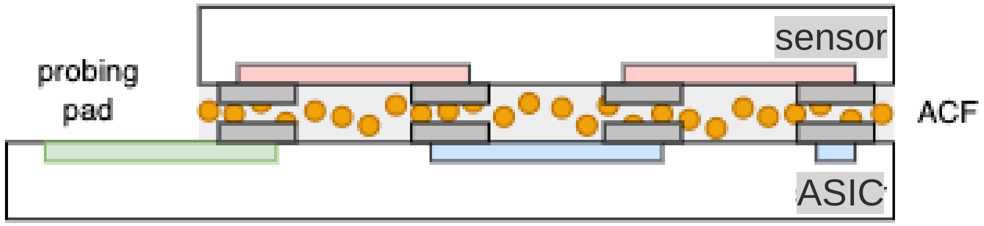
Preparation: Daisy-chain devices

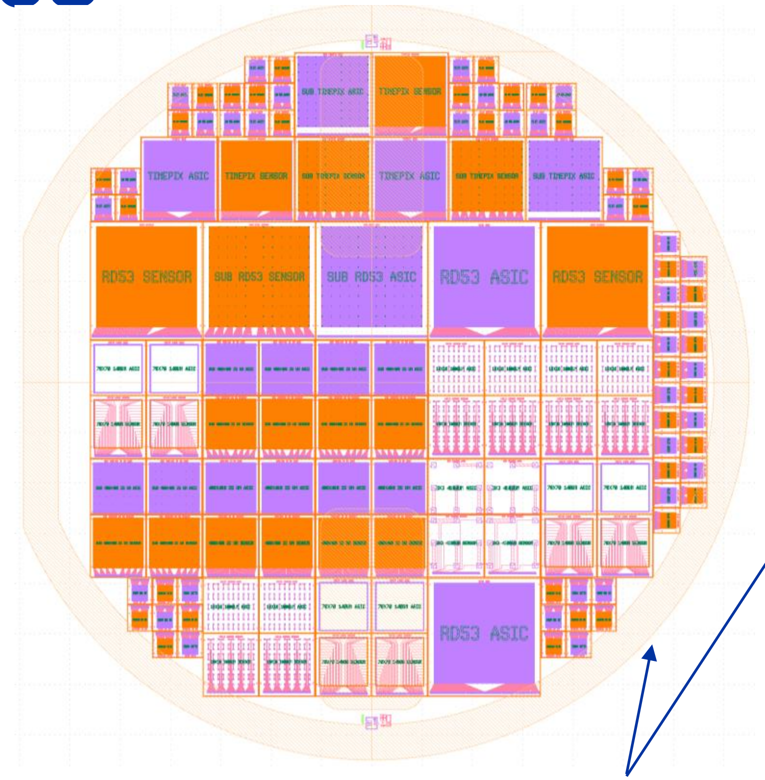
Top view

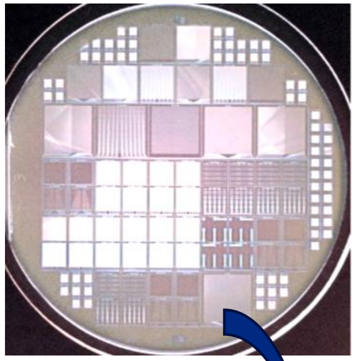
3x3, pitch 4500um, diceable

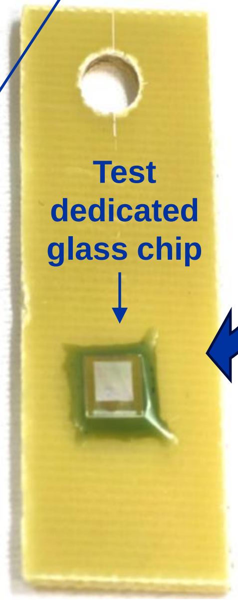


Side view









Test dedicated glass chip

Daisy chain devices produced at FBK

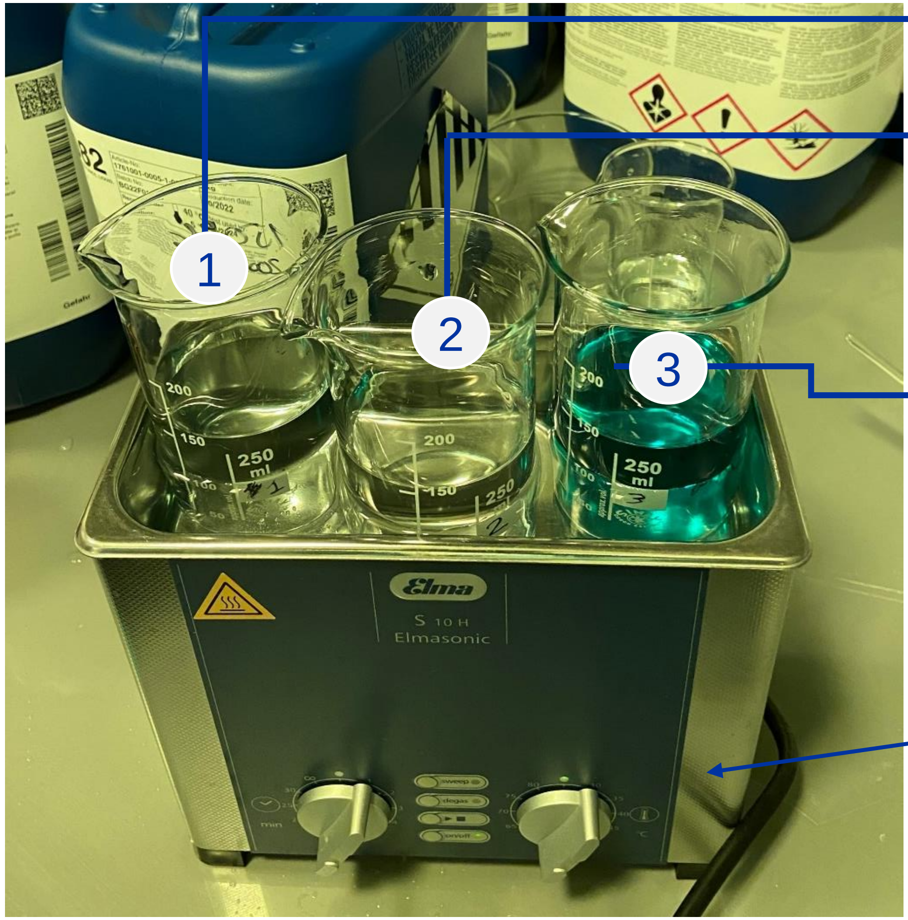
Designed to validate interconnect yield, electrical resistance, thermo-mechanical stress

- 6” glass wafers, up to 650µm thick
- Varying Bonding area, pad size and pitch, matching different target applications

LPNHE PARIS
FONDAZIONE BRUNO KESSLER
AIDA innova

Pre-treatment setup

Pre-treatment: ultrasound + manual movements (previously static)



Conditioner

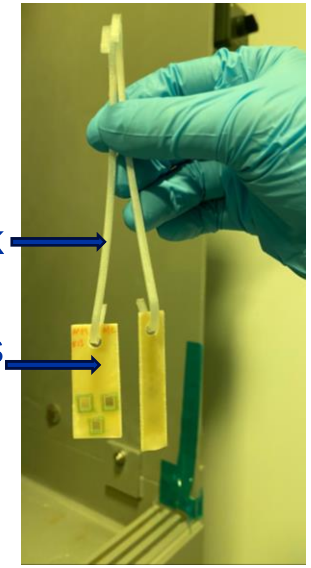
Al Etch

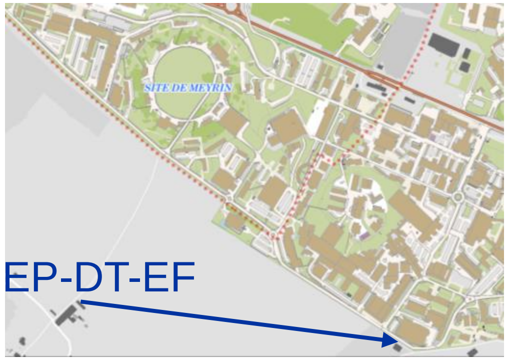
Zincate

Ultrasonic bath

Hook

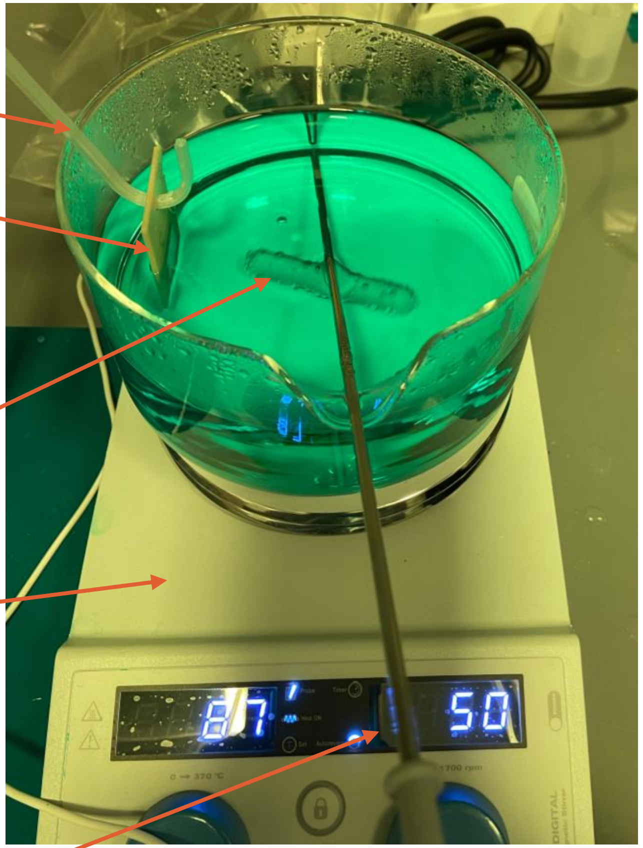
Samples



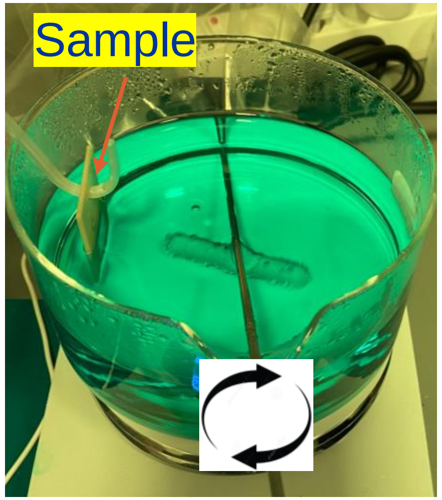


Setup at EP-DT-EF lab B107

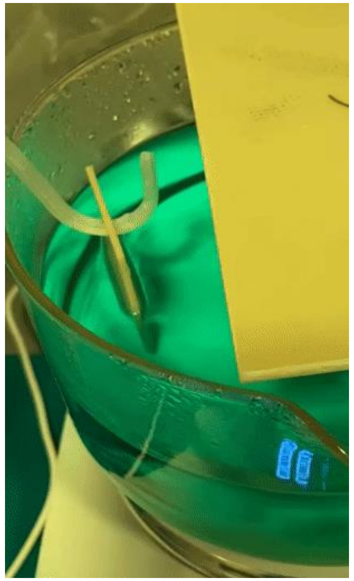
Nickel Plating setup



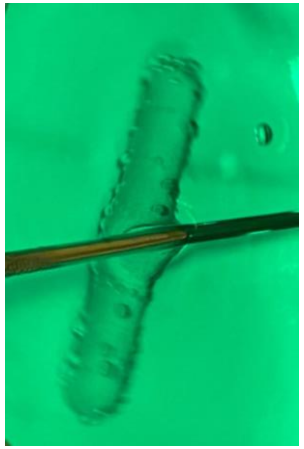
Stirring optimisation



Swing movements



Bubbles removal from surface of chip



Frequent calibration

- pH metre
- Temperature probe
- Micropipette

Avoiding cross-contaminations

Characterisation of ENIG plating

Keyence optical microscope
(CERN EP-ESE, B14)

NEW (at Campus Biotech)

Optical
profilometer

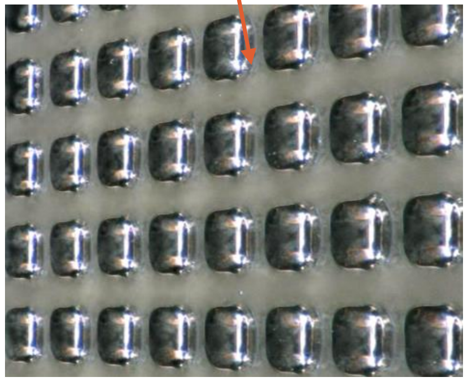
Bruker Contour

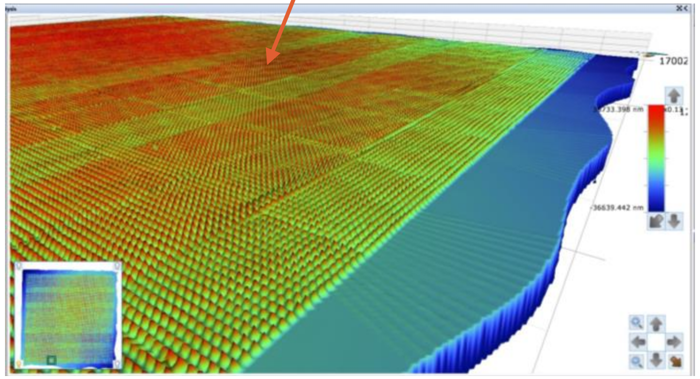
Mechanical
profilometer

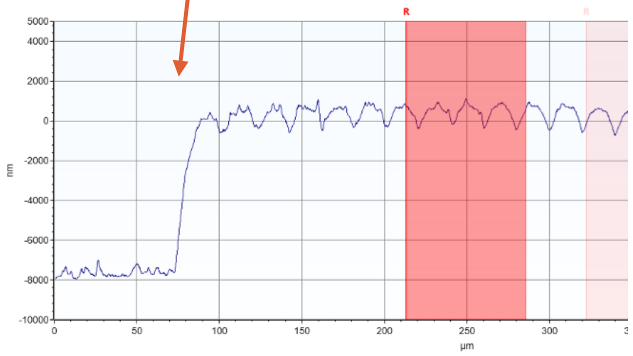
Bruker Dektat XT Stylus

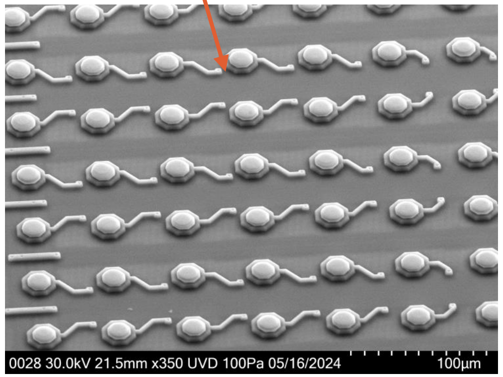
SEM

Hitachi SU5000





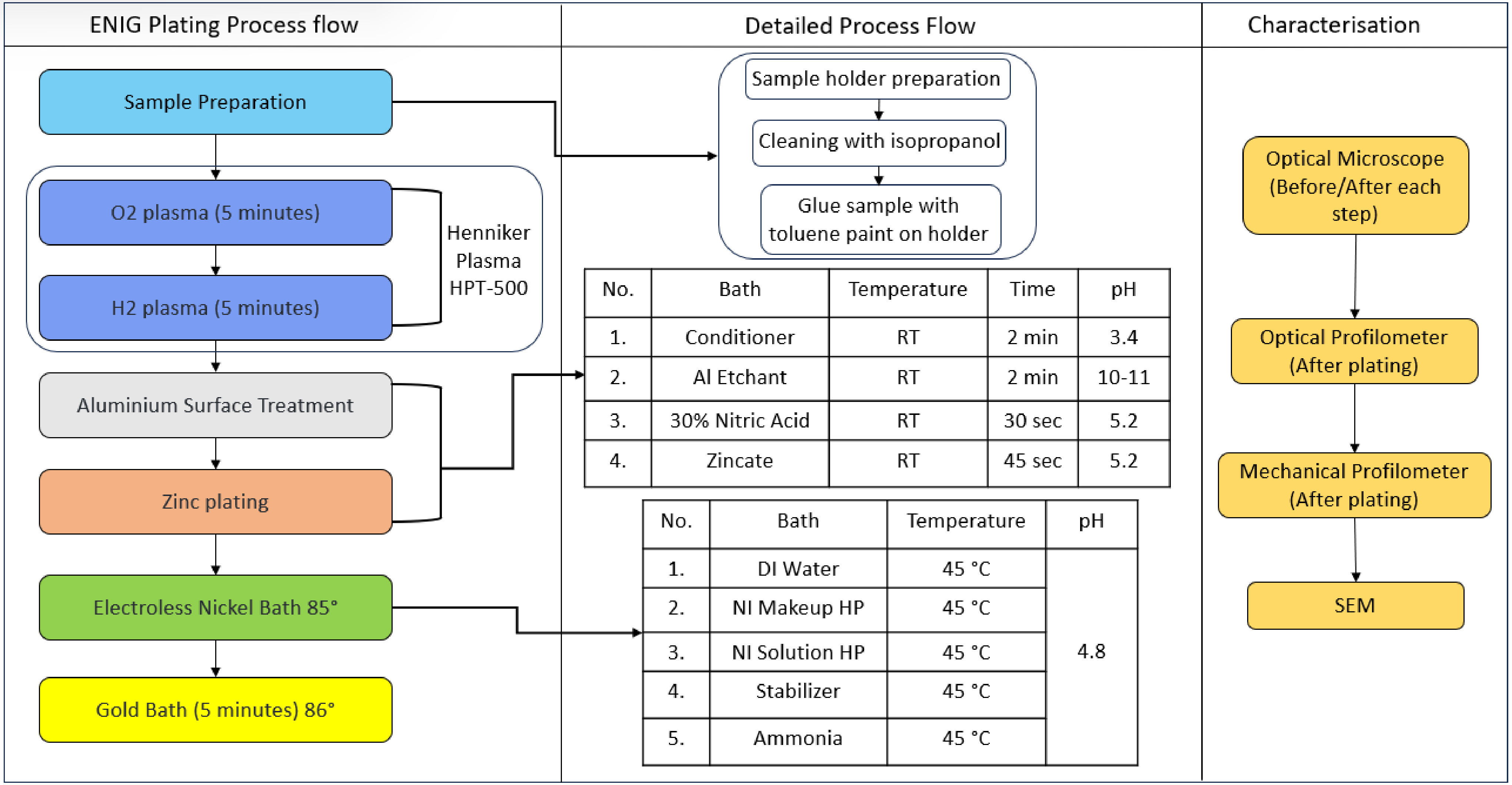




Process flow documentation

Systematic studies:

- Process flow
- Experimental design
- Detailed reports
- …



No.	Bath	Temperature	Time	pH
1.	Conditioner	RT	2 min	3.4
2.	Al Etchant	RT	2 min	10-11
3.	30% Nitric Acid	RT	30 sec	5.2
4.	Zincate	RT	45 sec	5.2

No.	Bath	Temperature	pH
1.	DI Water	45 °C	4.8
2.	NI Makeup HP	45 °C	
3.	NI Solution HP	45 °C	
4.	Stabilizer	45 °C	
5.	Ammonia	45 °C	

Results

Timepix3 type daisy-chain test structures

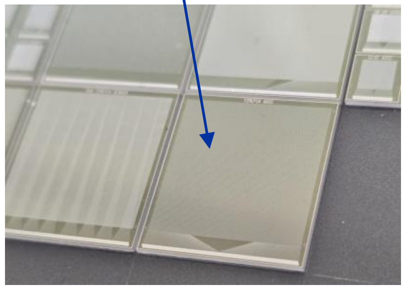
Good ENIG results on 22µm pads and 55µm pitch:

- No overplating
- No skipped pad or area
- Good pad homogeneity

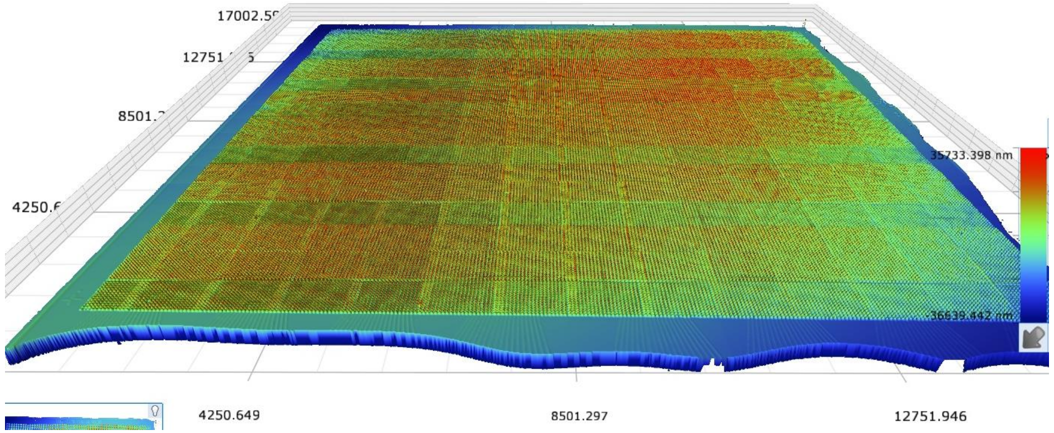
- 99% of pads correctly plated

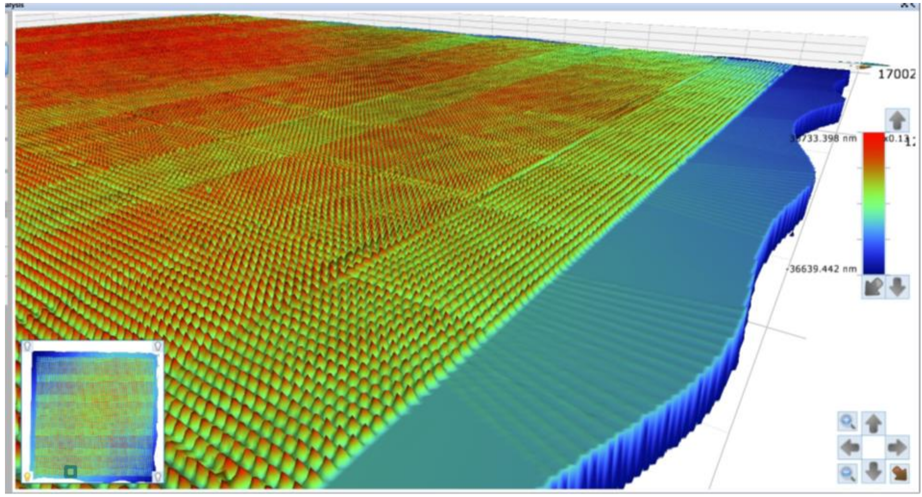
- Pads height: 10 µm (+/- 0.5µm) 55min deposition

Timepix 3 type daisy-chain device test structure (14x14mm)

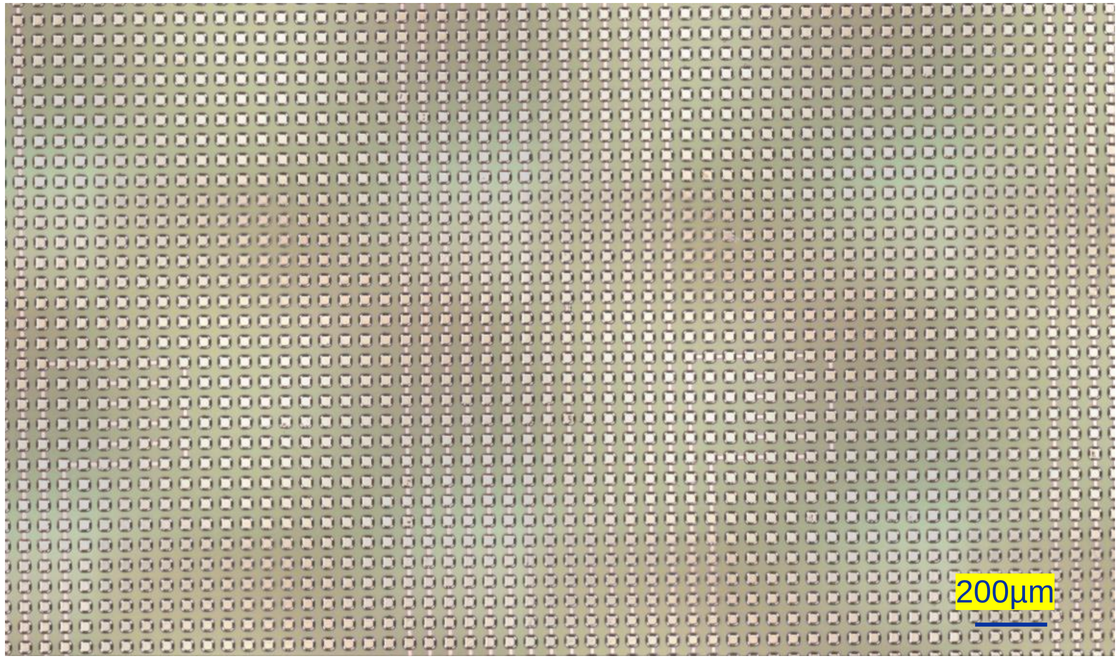


Optical profilometry after ENIG plating

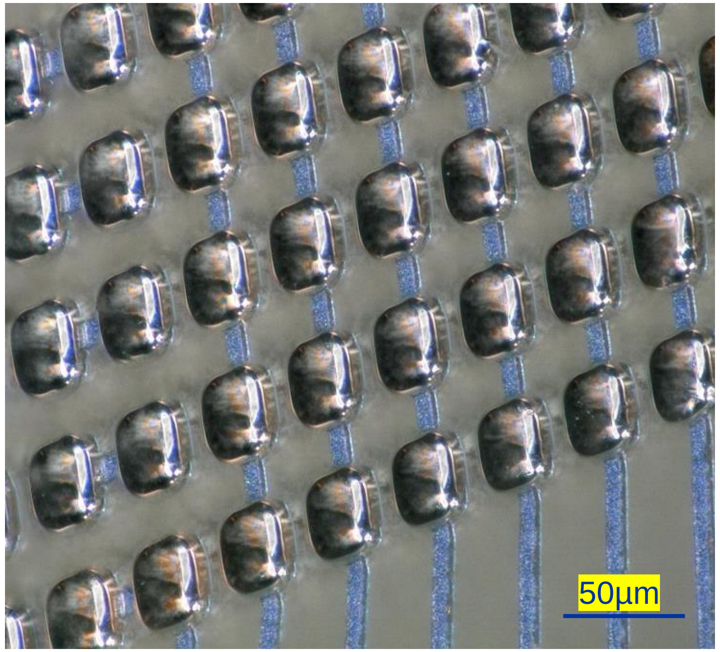




Optical microscopy after ENIG plating



Optical microscope, 45° tilt



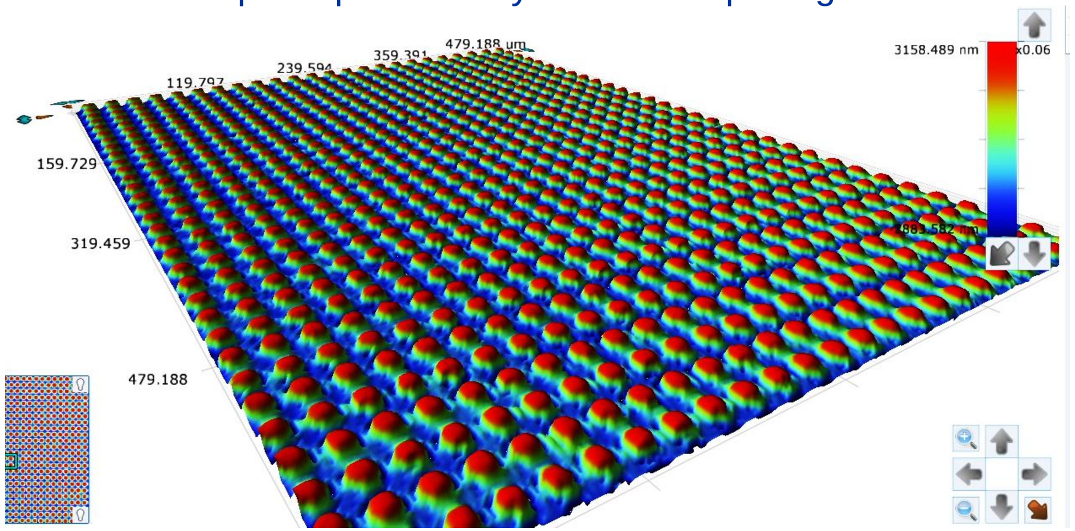
Results

“CLICpix2” type daisy-chain test structures, <u>20µm pitch, 10x8µm rectangular pad size</u> (High connection density)

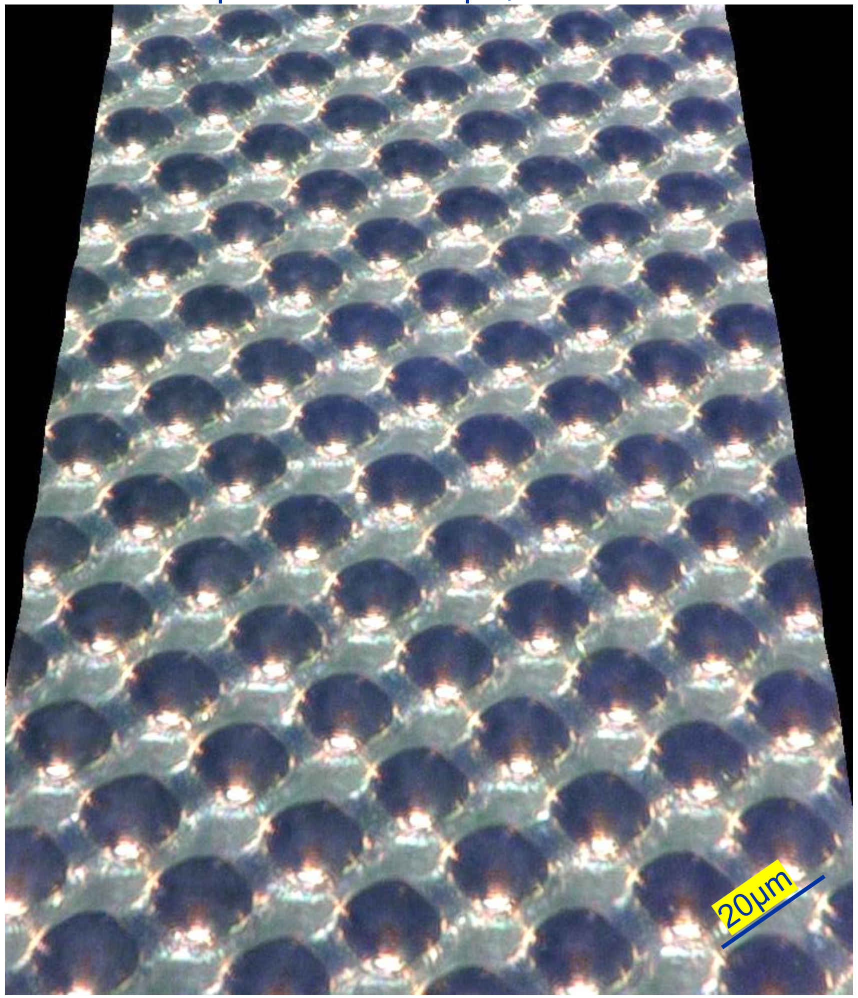
Excellent ENIG results:

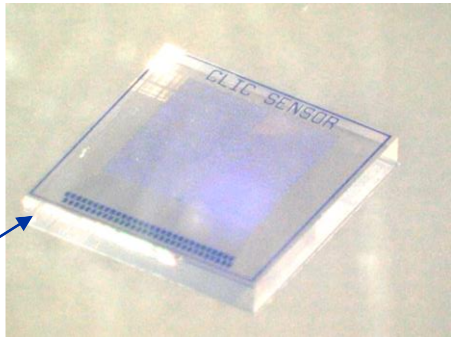
- Good results, in line with our objectives
- >99% of pads correctly plated (16384 pads)
- Pads height: 4.5 µm (25min deposition)

Optical profilometry after ENIG plating

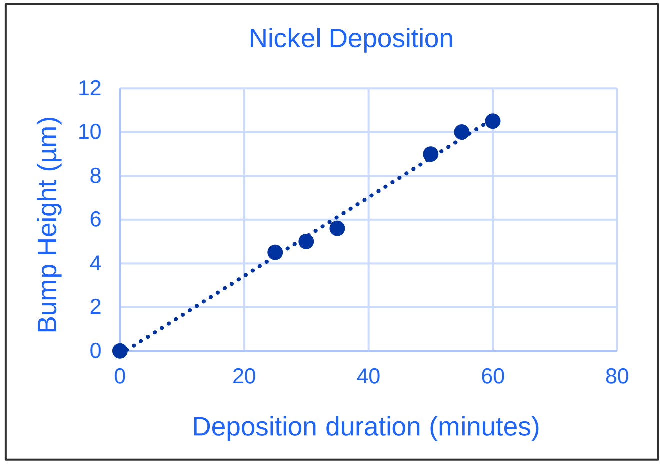


Optical microscope, 45° tilt





CLICpix2 type daisy-chain test structures (3.2x3.2mm)



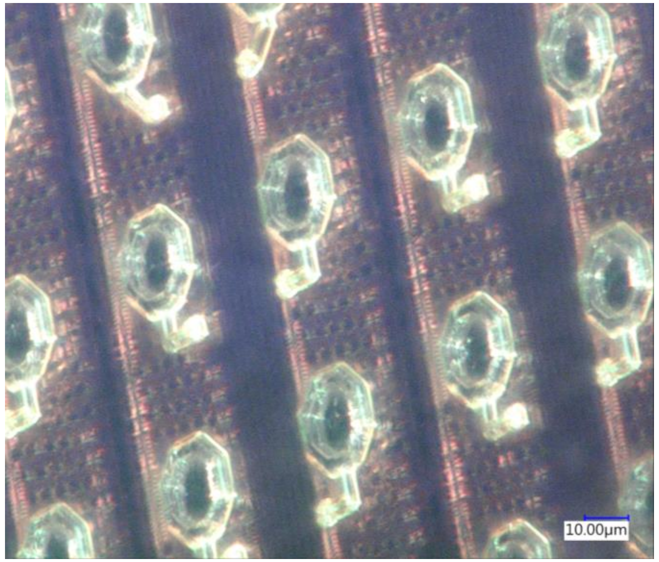
Results

TimeSpot ASIC
Functional chip
55µm pitch, 19µm pads

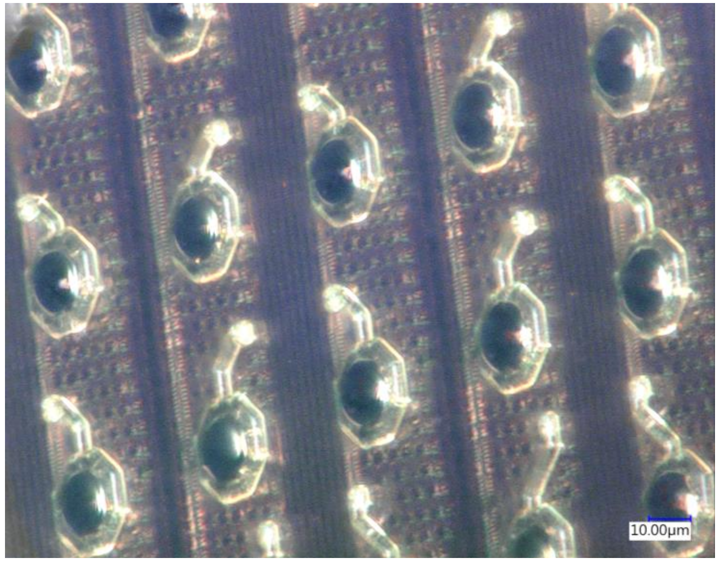
Excellent ENIG results:

- 99.93% of pads correctly plated (1184 pads, 1 not correct due to particle masking)
- Pads height: 10 µm (1h deposition)

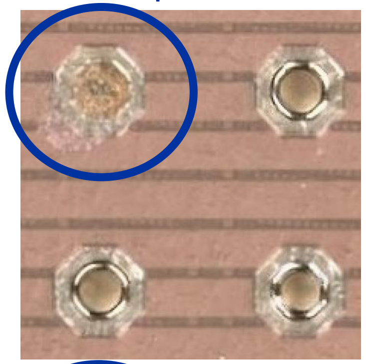
Before plating, optical microscope

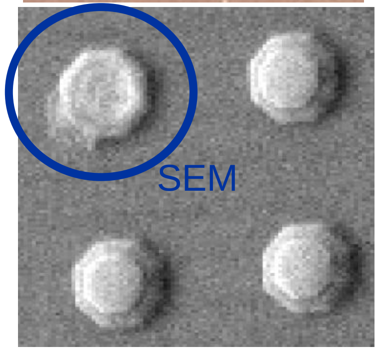


After 1h plating, optical microscope

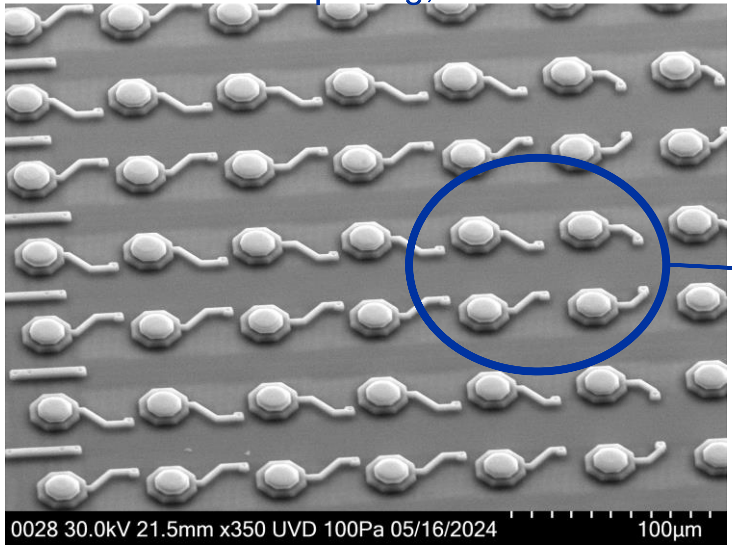


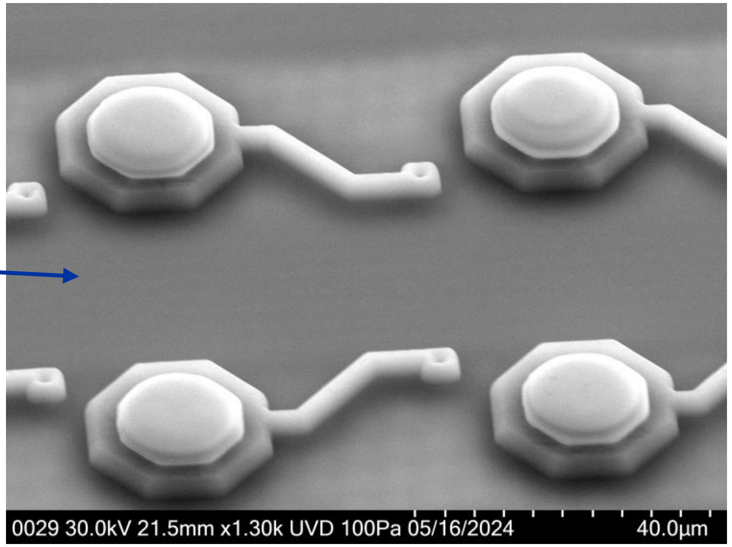
1 pad non plated due to particle





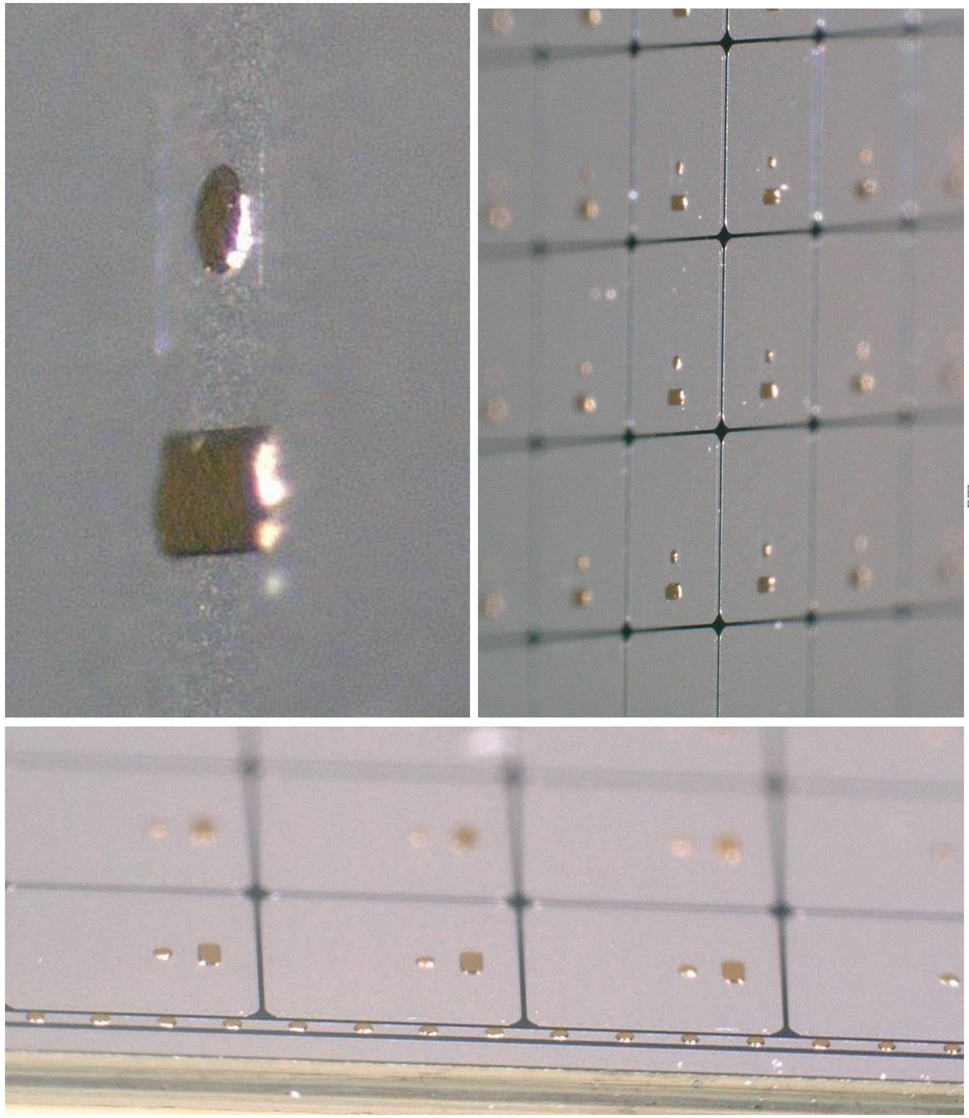
After plating, SEM



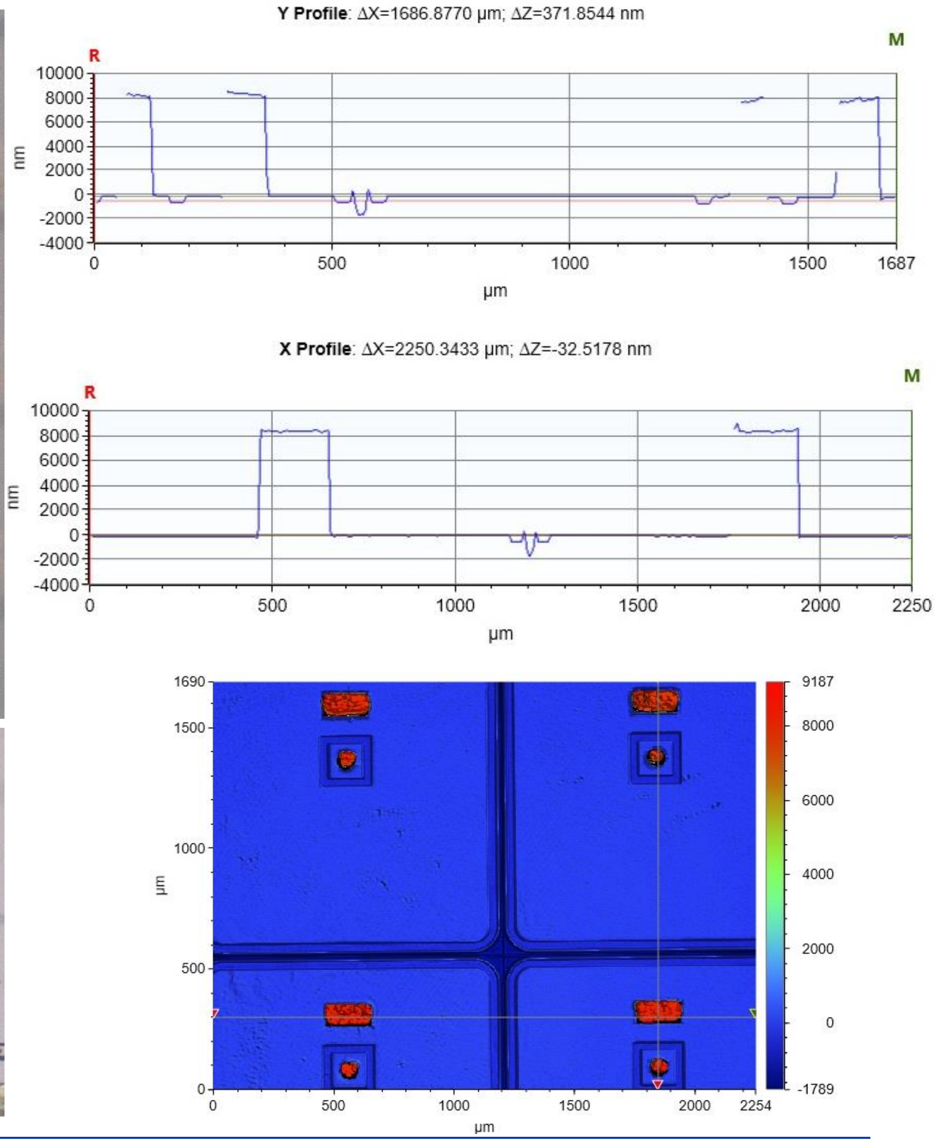


Results

Optical microscope, 62° tilt



Optical profilometry after ENIG plating



ALTIROC3 sensor
Functional chip
1.3mm pitch,
90x90µm pads

Good ENIG results:

- Homogeneity of bumps achieved with no overplating
- No skipped pads
- Pads height: 8.5 µm (1h deposition)

Conclusion

	Pad size	Pitch	ENIG height
“Timepix3” daisy-chain test structures	12-14 µm	55 µm	10 µm
TimeSpot ASIC	19 µm	55 µm	10 µm
“CLICpix2” daisy-chain test structures	10x8 μm^2 (rectangular)	20 µm	4.5 µm
ALTIROC3	90x90μm^2	1.3 mm	8.2-8.5 µm

Optimisation of ENIG plating:

- Reproducibility
- Almost no skipped pads and areas
- Almost no overplating
- Uniformity (even at the edge of the chips)

- **Adaptation of the ENIG process to high pad density (20µm pitch) and smaller pads (10µm)**
- **Adaptation of the ENIG process to lower pad density (1.3mm pitch) and large pads (90x90µm)**
- **Successful plating of functional TimeSpot ASIC and ALTIROC3 sensors**

Next steps:

- Confirmation of these results on high number of chips
- Study of the stability of the process over time (process drift)
- Apply this ENIG plating process to other functional ASICs and sensors and adjust plating parameters for each application (CLICpix2, Timepix3/4…)
- Scalability of the process (single wafer processing)