1° DRD3 Meeting on Solid State Detectors
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Technology Transfer of LGAD Sensor for Large-Volume Productions

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With the support of the UFSD Group, University and INFN of Turin

Motivations

LGADs have many applications in present and future detectors:

- MIP Timing Layer: CMS-ETL, ATLAS-HGTD
- Particle identification (Time of Flight): ALICE 3 (Run5), Belle2, Electron Ion collider (Tracking + TOF@ePIC) >2031) , and Future Lepton colliders (>2040).

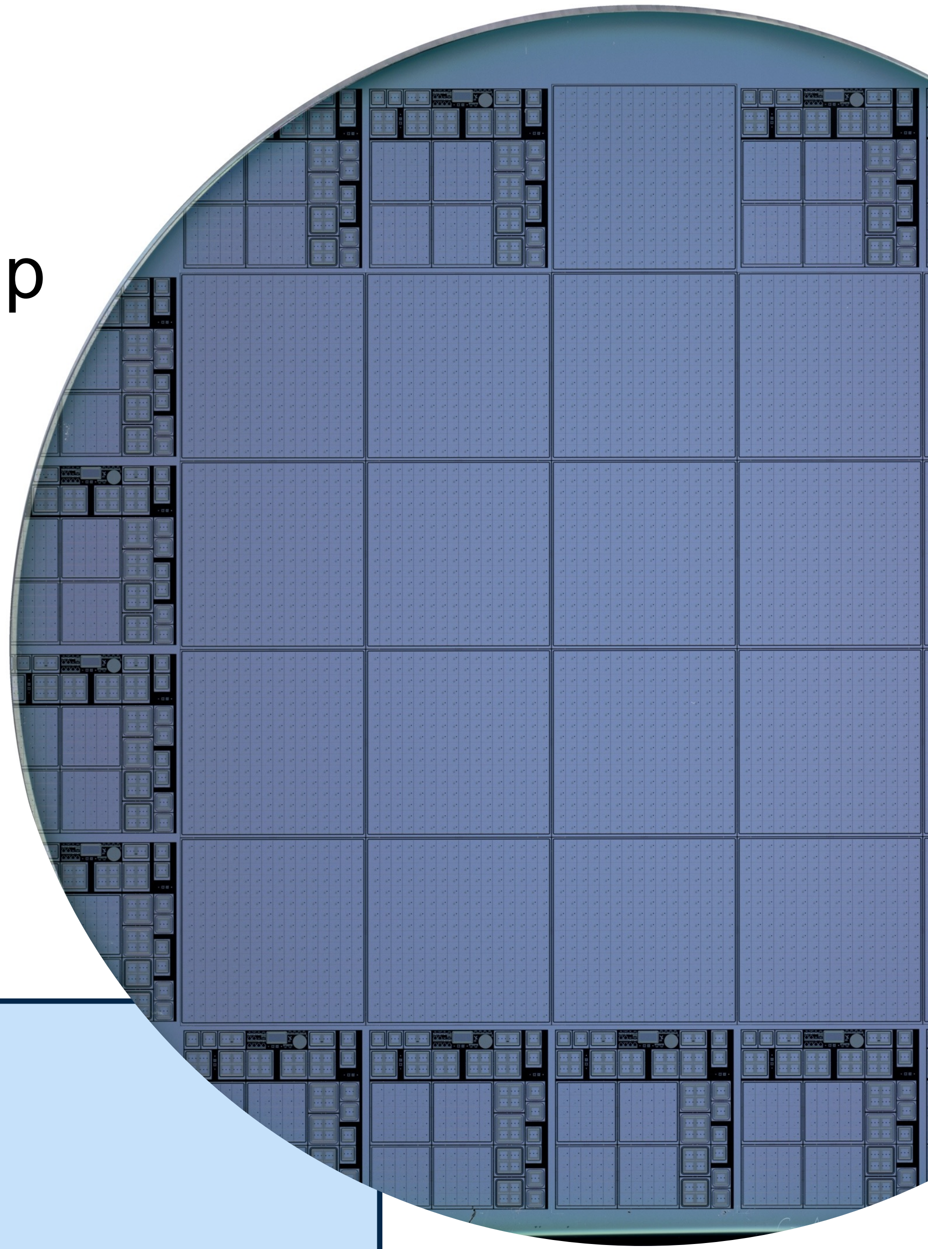
In all these cases, large surfaces (several m^2) have to be covered with LGAD Sensors

Important Aspects to be demonstrates:

- Reliability of the LGAD fabrication process
- Capability of large-area productions
- Yield, reproducibility of the process, also considering all the peculiar aspects of LGADs (i.e. Doping homogeneity -> V_{BD} and Gain uniformity)

These motivations are actually already included in WG2 research goals of DRD3

FBK-LGAD Technology



Two main LGAD technology variants developed in collaboration with the UFSD group (Torino, Trento, Perugia) for 4D-tracking:

- **Standard (Shallow) Gain Layer**
- **Deep Gain Layer**

Both of them qualified with respect to CMS and ATLAS requirements.

The deep version seems to perform slightly better at higher fluences

After the R&D Phase, FBK worked to lead this technology at a higher TRL

Many challenges faced:

- Assuring high production-yield
- Assuring high reproducibility and industry-level quality control
- Guarantee large volume production (~2000 wafers) in a short time
- Reduce the overall production costs per wafer

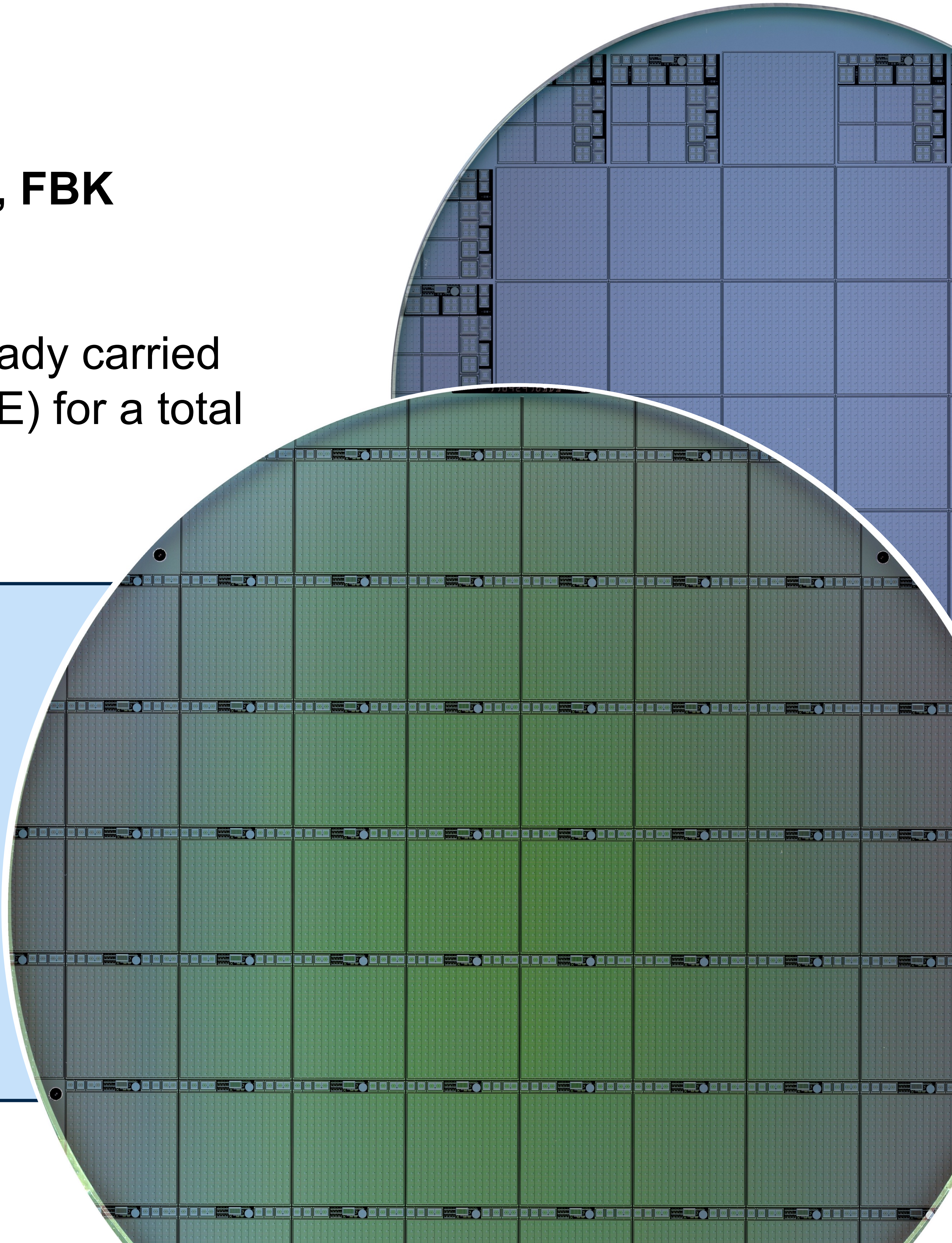
Technology Transfer

To demonstrate the scalability of the FBK-LGAD technology, FBK started a TT to an external CMOS Foundry

LFoundry was selected as a partner. In previous years, FBK already carried out TT of SiPMs to LF for large productions (DarkSide and DUNE) for a total of >2000 wafers produced with exceptional results

Expected Advantages:

- Scaling to 8’’ (double the area, taking almost the same production costs)
- Possible high-volume productions (LF has a capacity of 40.000 wafers/month)
- Industry-standard process quality



Technology Transfer

Custom process

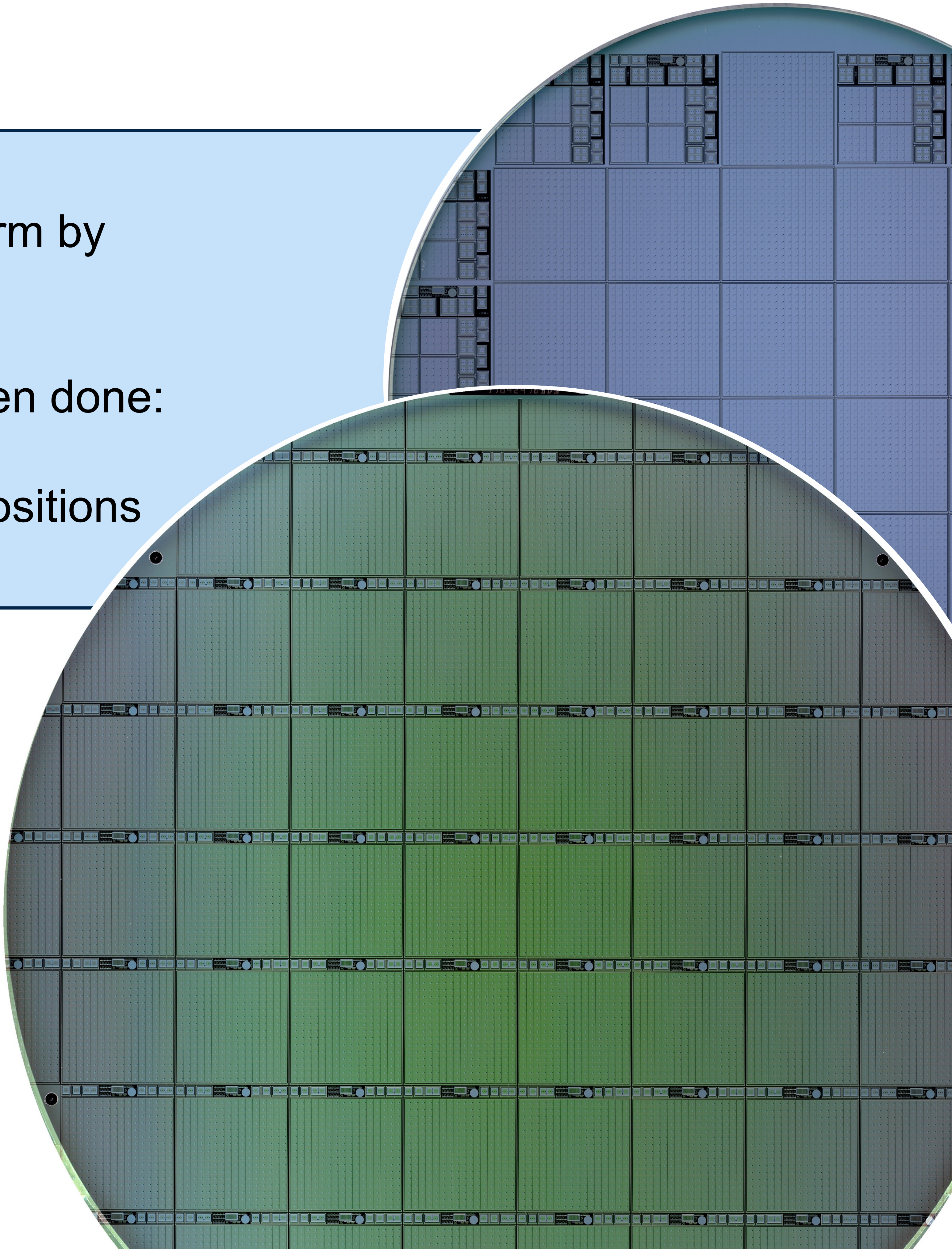
The production is not based on a CMOS Technology Platform by LFoundry (i.e. LF110 or LF150).

It is a fully customized process.

A one-to-one transfer of the single production steps has been done:

- oxidation/annealing recipes
- Same depositions materials and thicknesses (same depositions
- Ion implantation parameters

Dec 2023	**Starting of the TT activities**
Jan-Feb 2024	Prodcution of Short Loops to qualify some single process steps
March – May 2024	Production of 1st Batch (Learning Cycle 1)
May-June 2024	Wafer-level Characterization of LC1
June-Sep	Test beam and irradiation of LC1
Sept 2024	Production of 2nd Batch (LC2)



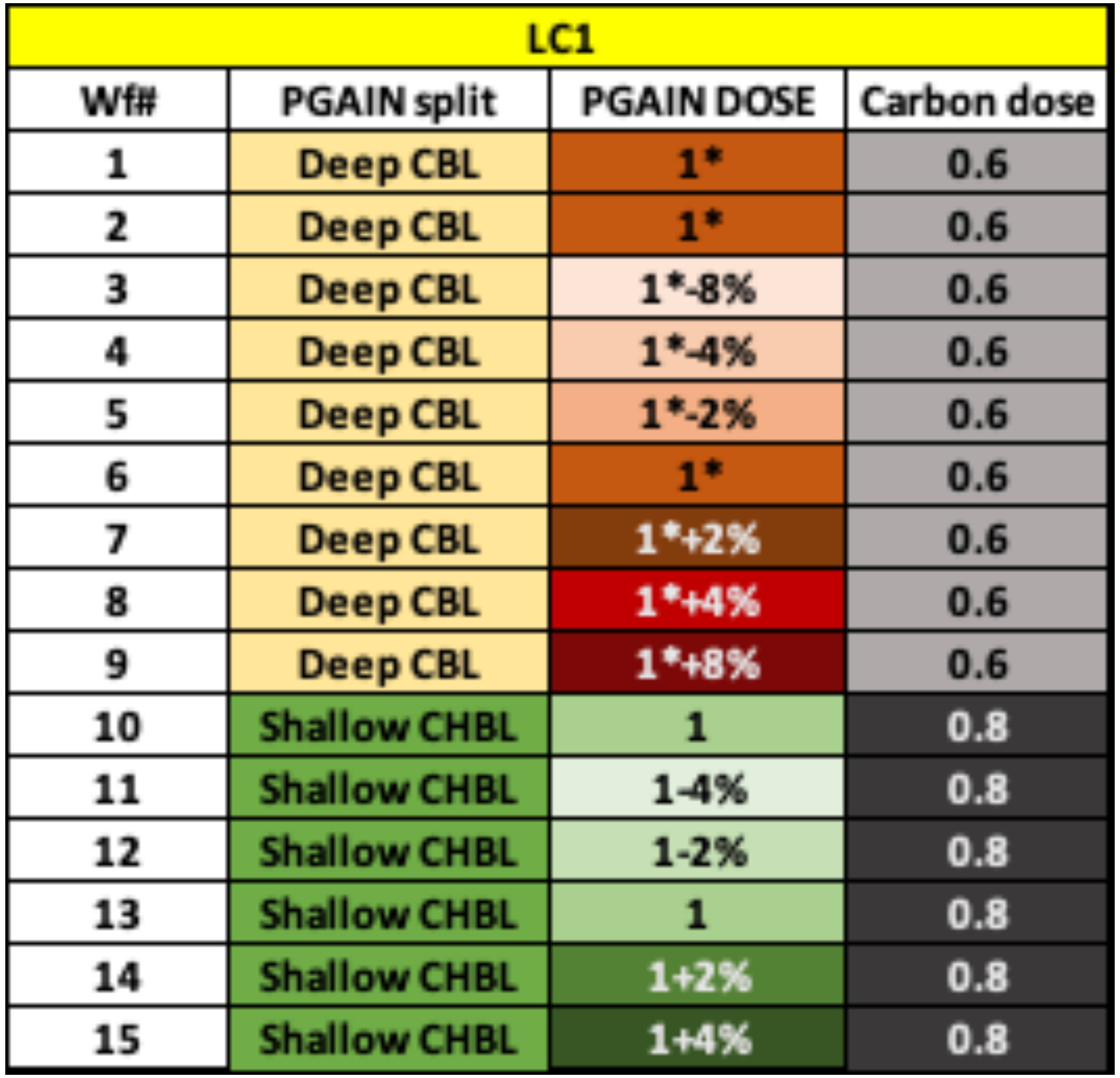
First Learning Cycle: Split Table

- Two main splits:
DEEP Gain Layer
Shallow Gain Layer

- PGAIN Dose variations:
-8% +8% for DEEP
-4% 4% for Shallow

- Carbon co-implantation on all the wafers

Split Table



LC1			
Wf#	PGAIN split	PGAIN DOSE	Carbon dose
1	Deep CBL	1*	0.6
2	Deep CBL	1*	0.6
3	Deep CBL	1*-8%	0.6
4	Deep CBL	1*-4%	0.6
5	Deep CBL	1*-2%	0.6
6	Deep CBL	1*	0.6
7	Deep CBL	1*+2%	0.6
8	Deep CBL	1*+4%	0.6
9	Deep CBL	1*+8%	0.6
10	Shallow CHBL	1	0.8
11	Shallow CHBL	1-4%	0.8
12	Shallow CHBL	1-2%	0.8
13	Shallow CHBL	1	0.8
14	Shallow CHBL	1+2%	0.8
15	Shallow CHBL	1+4%	0.8

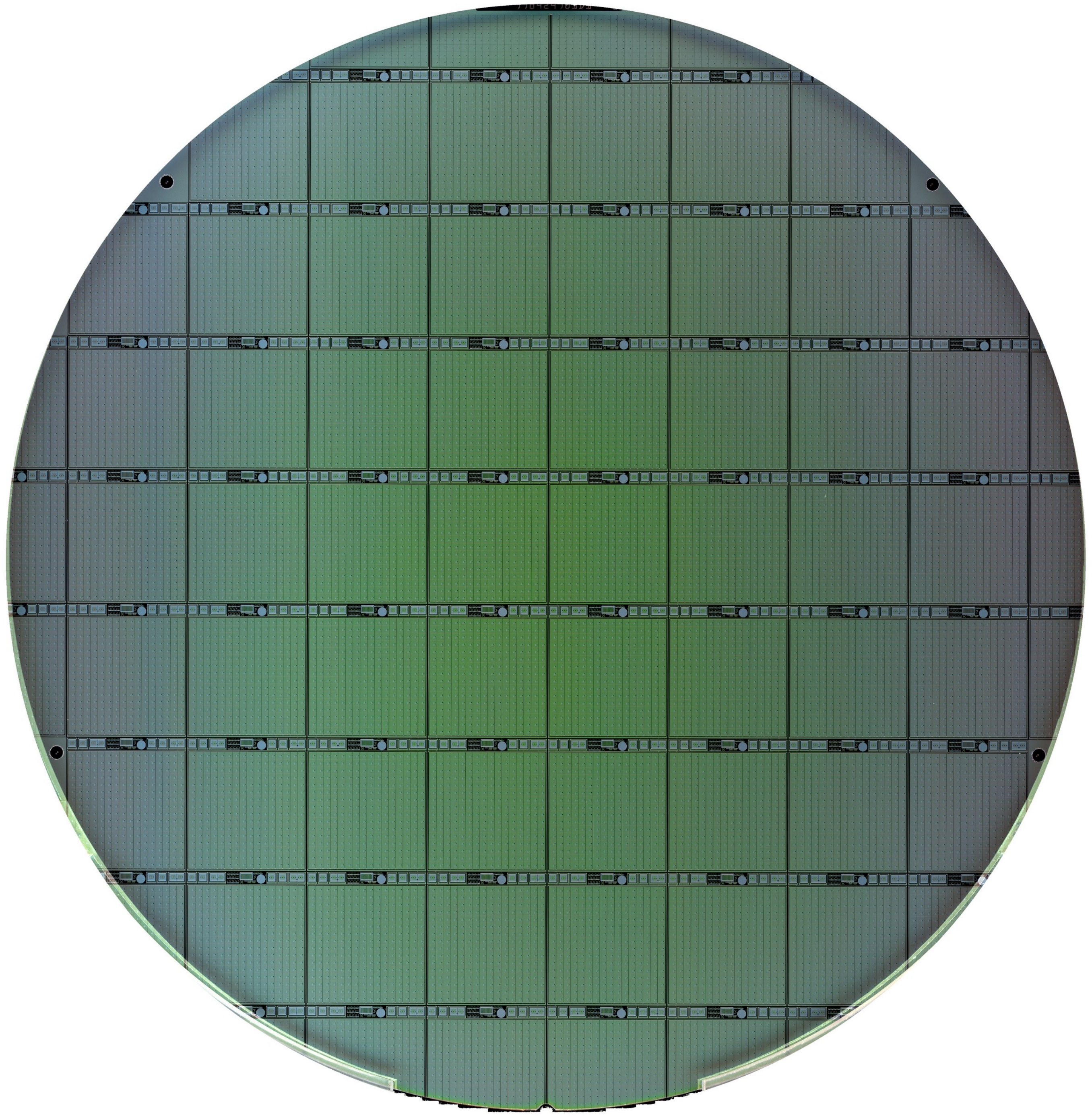
Set-up wafers

Dose split

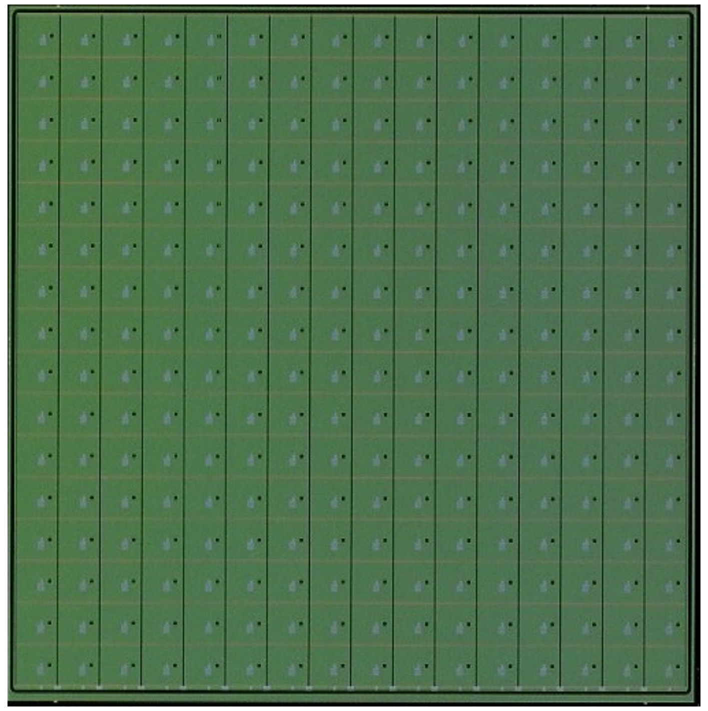
Set-up wafer

Dose Split

First Learning Cycle: **Layout**



16x16 CMS Sensor (2x2 cm^2)



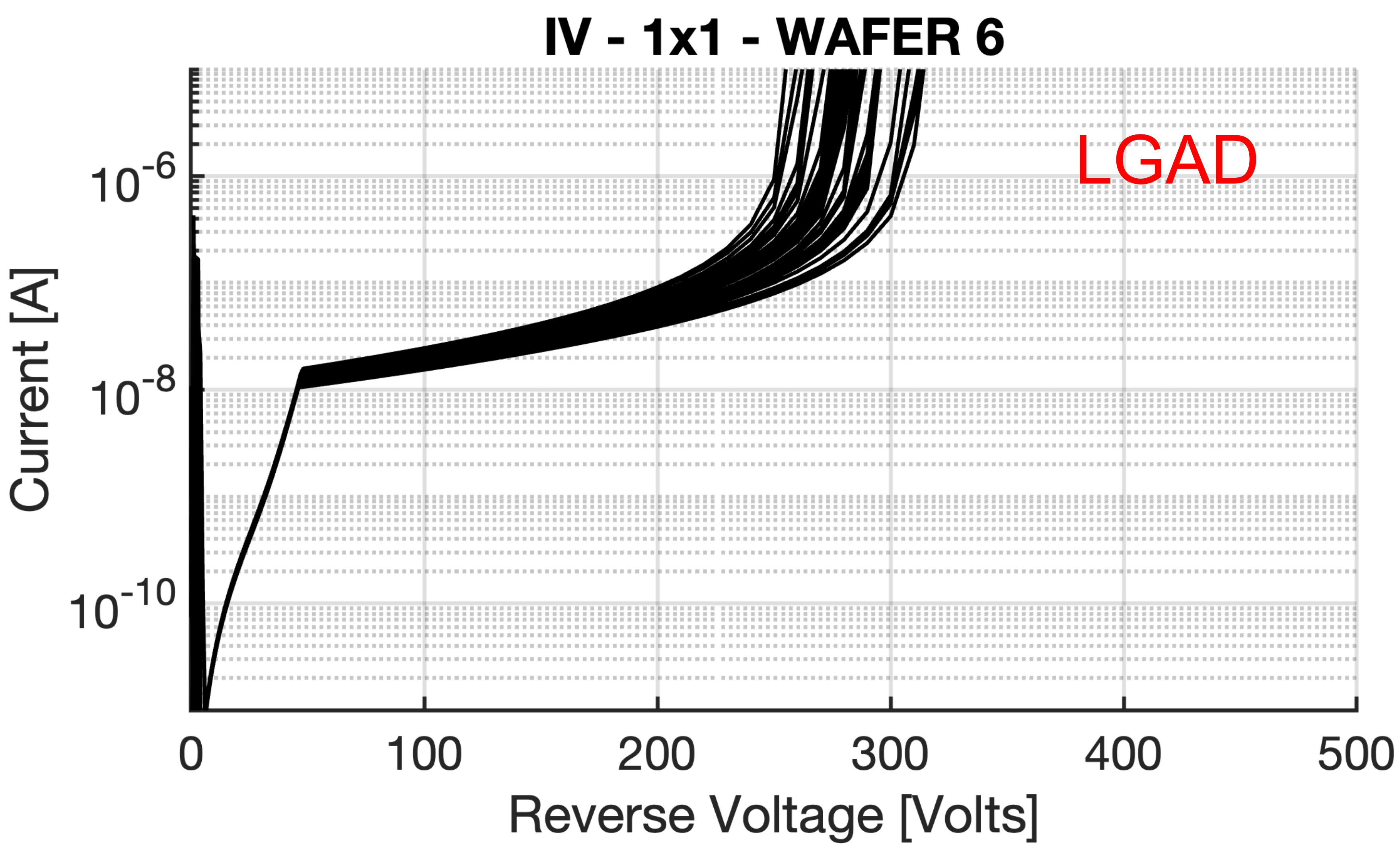
- Type 9 (double p-stop)
- GR 300 um
- 44 Full Devices/wafer

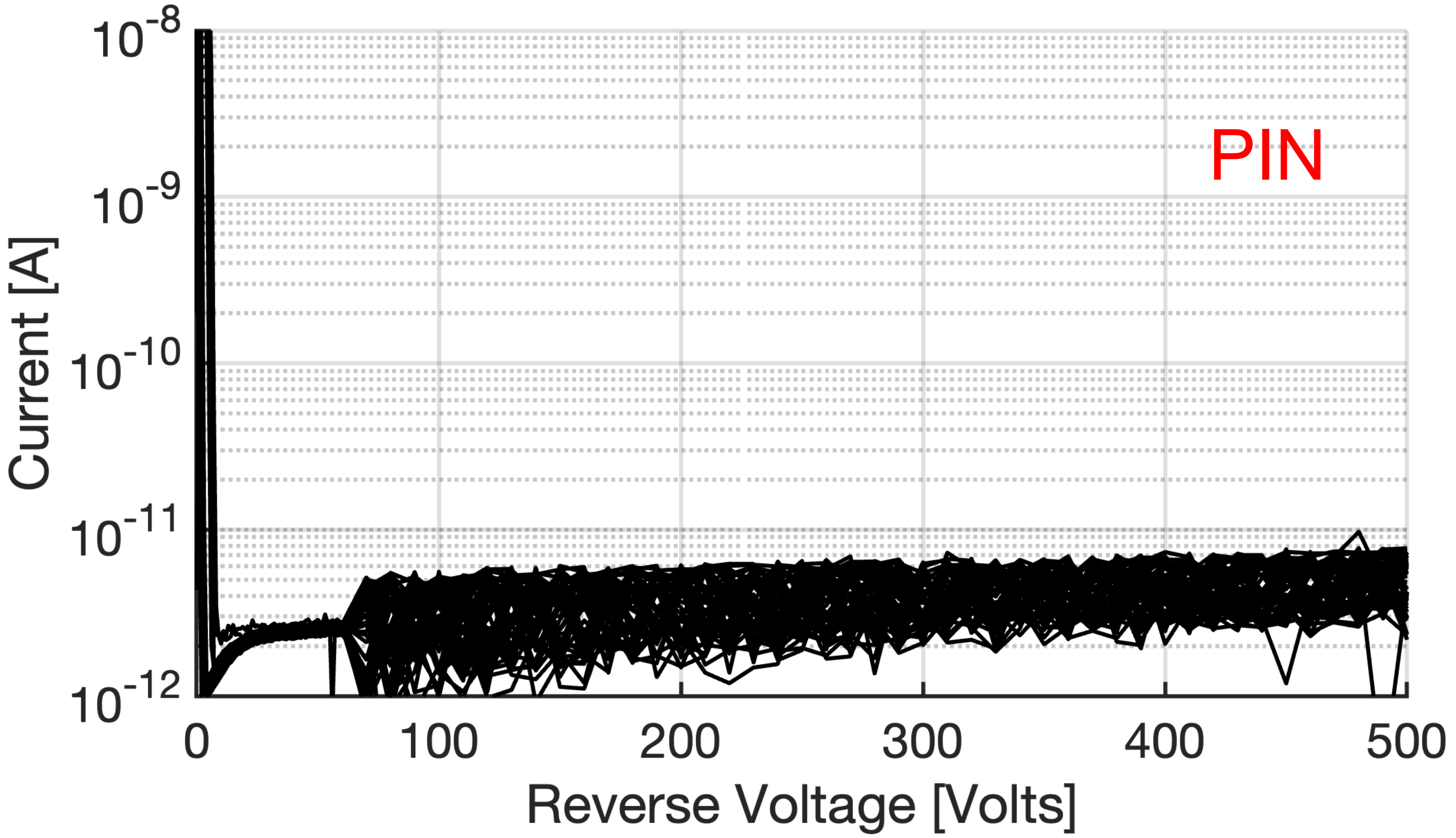
PCM and Test Structure (0.2x2 cm^2)

- 1.3x1.3 mm^2 PAD and PIN
- 1x2 pixels for inter-gap characterization
- PCM: 4PK for contact resistance; VDP for implant sheet resistance; CAP for dielectric thicknesses; others…

Wafer Level Characterization: PAD/PIN DARK IV

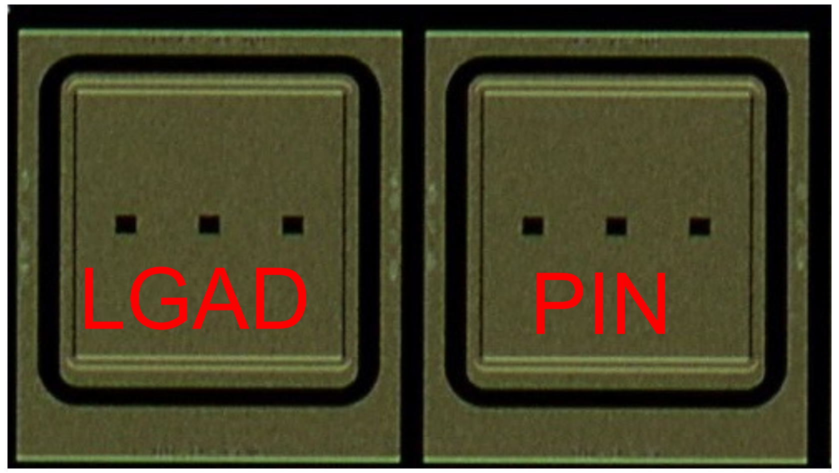
WAFER 6: DEEP PGAIN DOSE = 1.0





- All samples working
- Low PIN current
- Uniform IV

1.3x1.3 mm^2 PAD/PIN



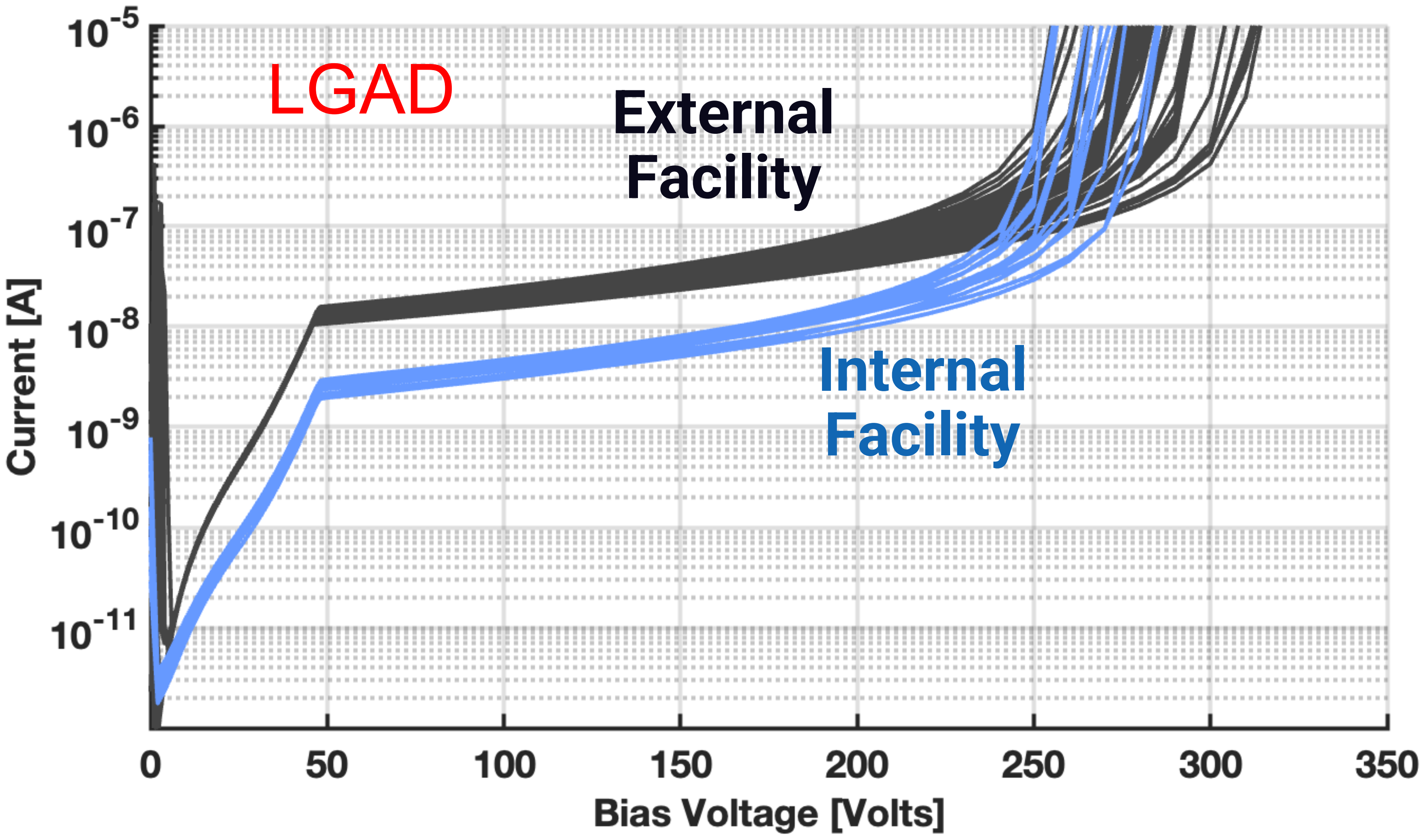
PAD/PIN from all the 52 Test structures on the 8'' wafer

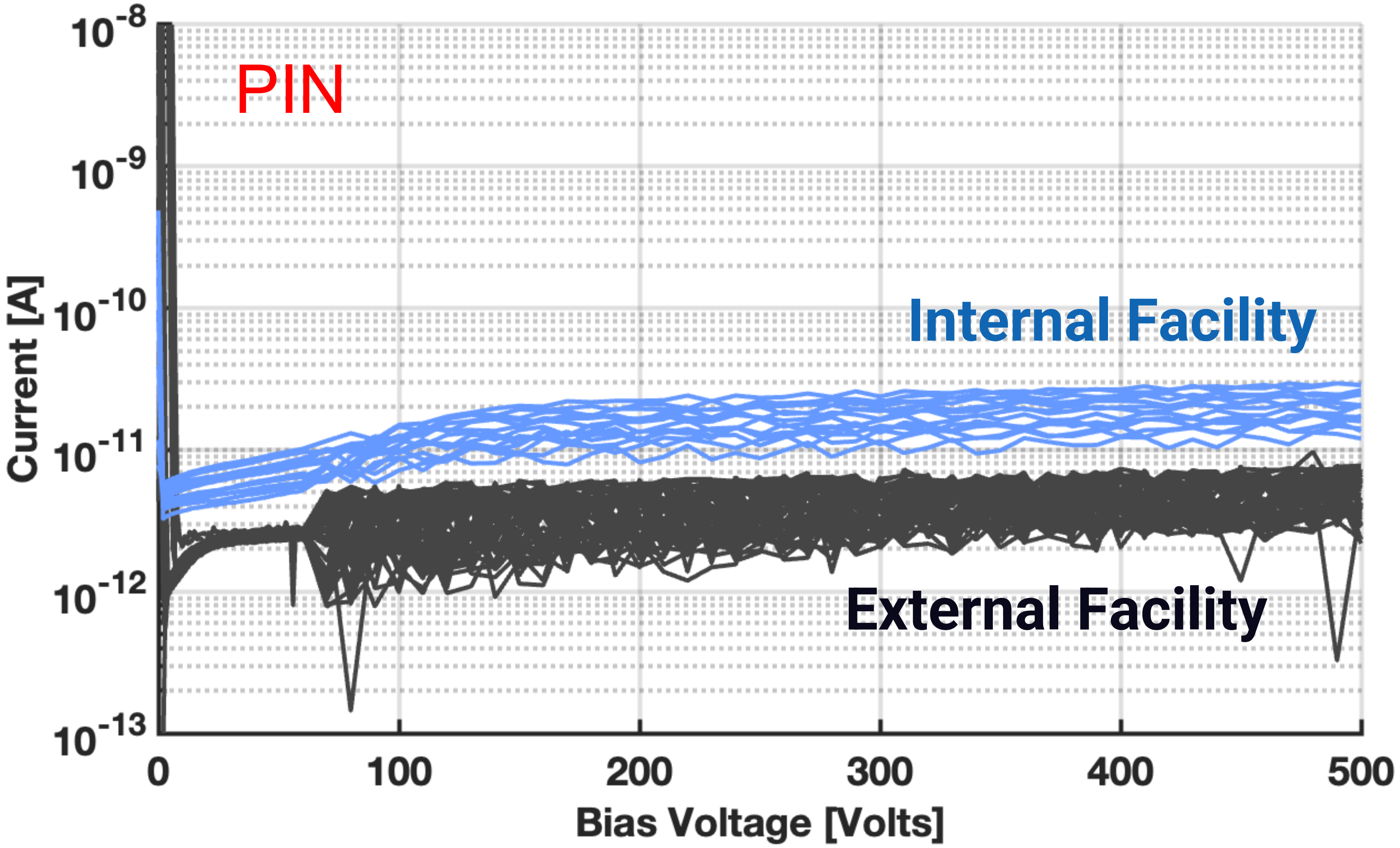
Meas. conditions:

- 1-60 Volts Step 1 V
- 60-500 Volts – Step 10 V

PIN/PAD Characterization: comparison External vs Internal Facility

IV comparison of single PAD/PIN
2 wafers from the same Technological Split: DEEP PGAIN – Dose 1.0 – Carbon 0.6

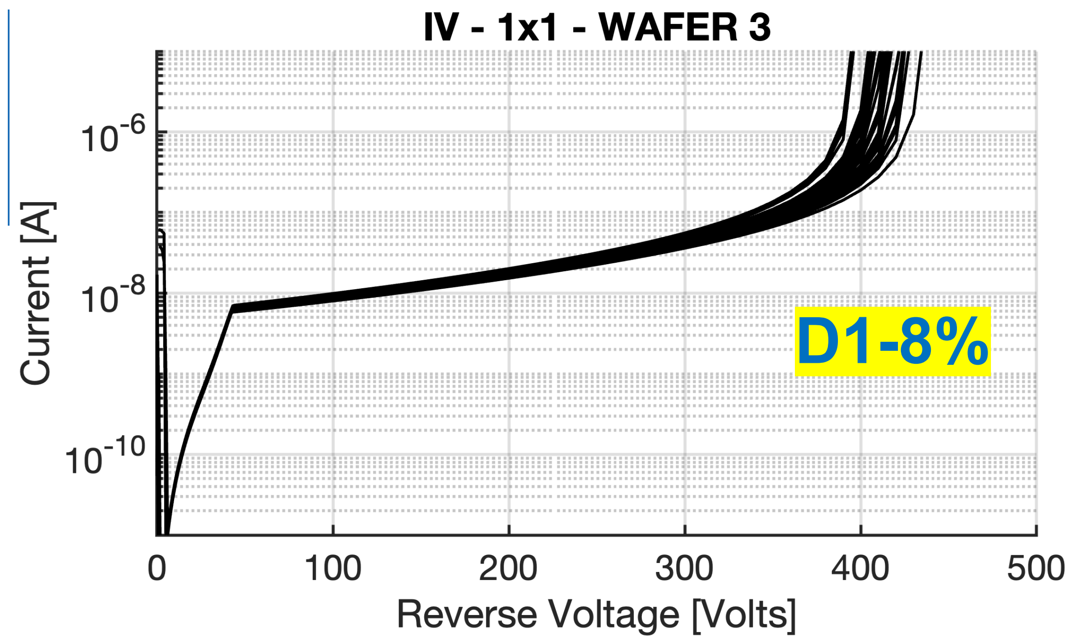


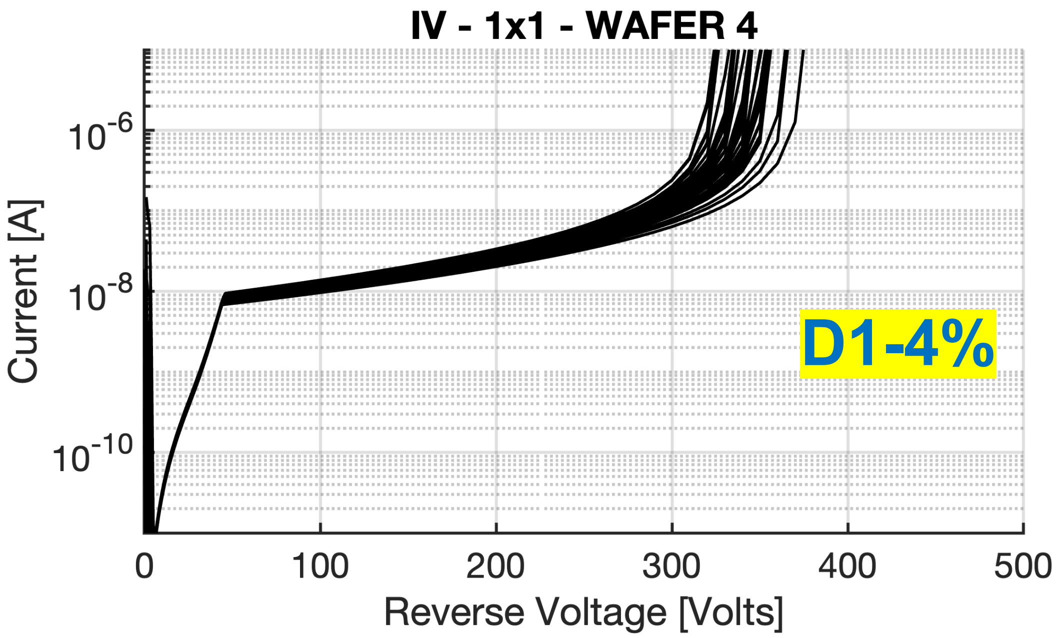


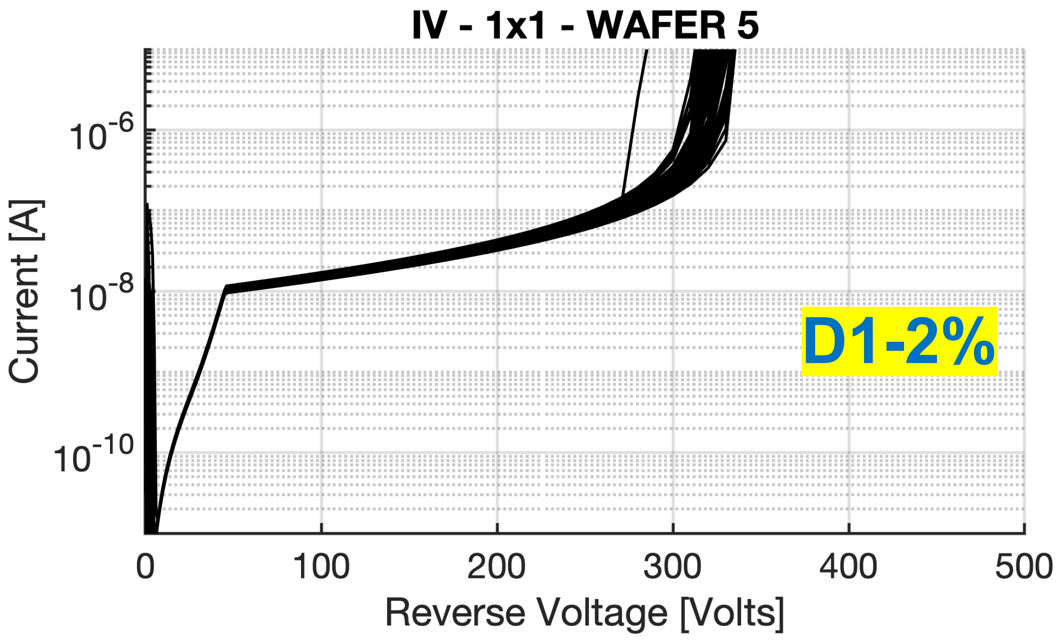
Internal Facility:
UFSD4-CMS W18

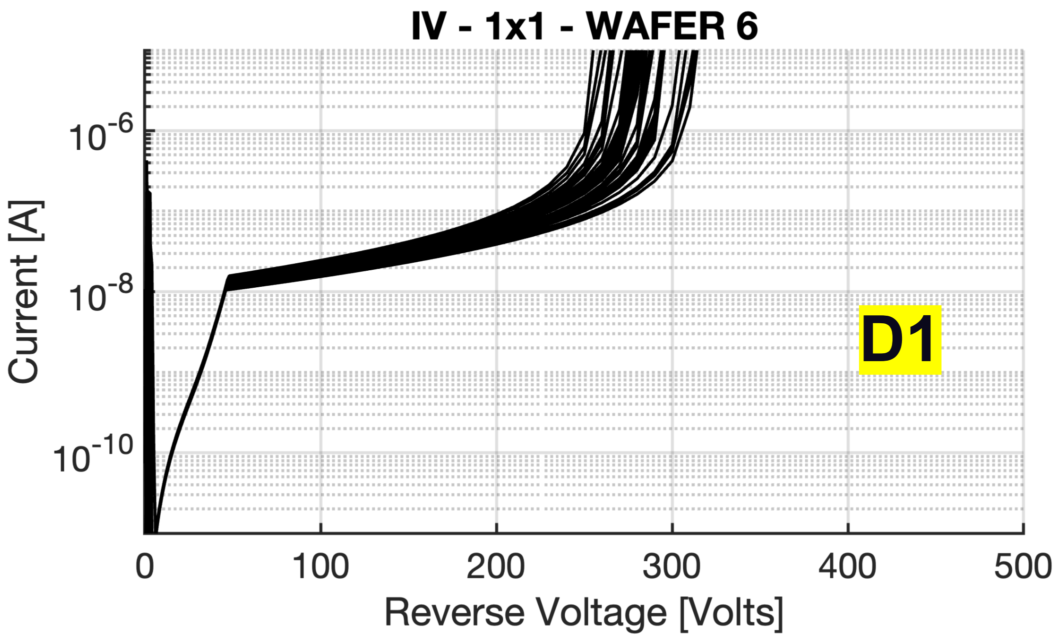
- ✓ Similar performance in terms of Dark Current
- ✓ Same full-depletion voltage
- ✓ Similar Breakdown Voltages

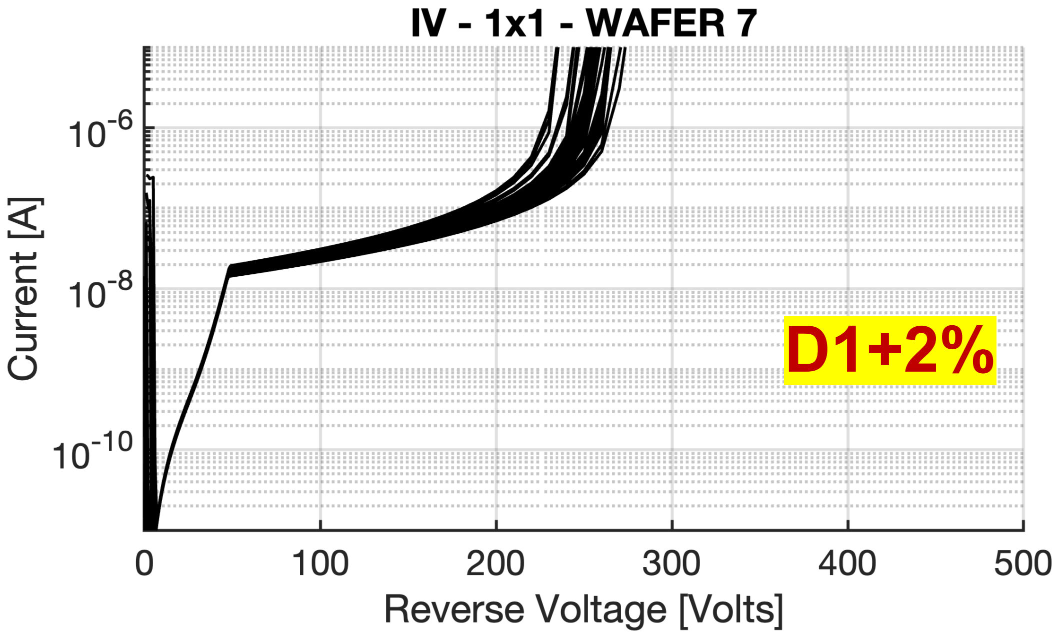
PAD Characterization: DARK IV (DEEP Split)

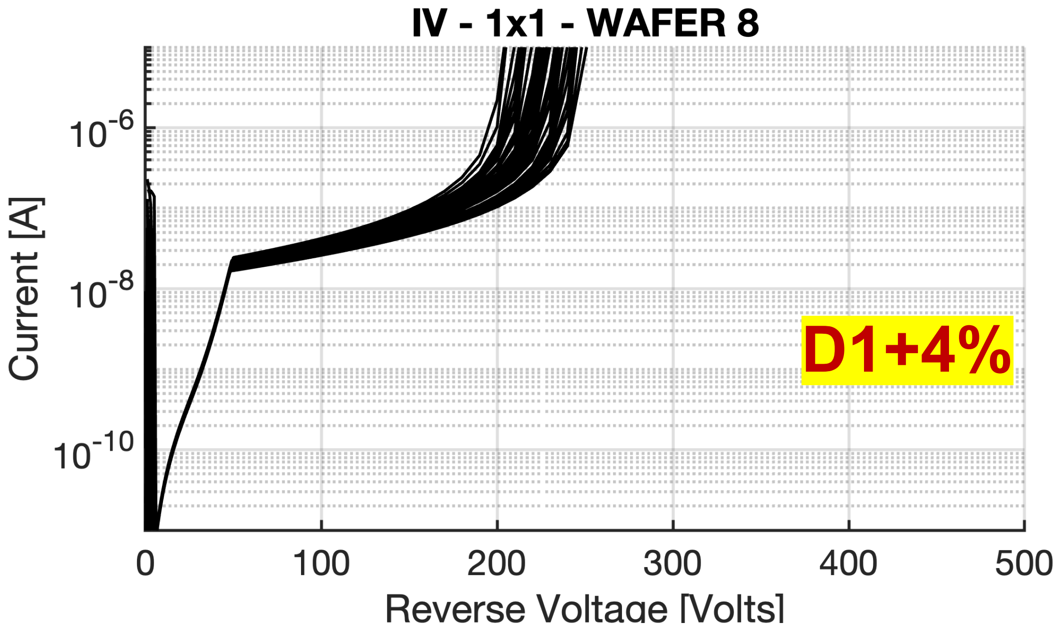




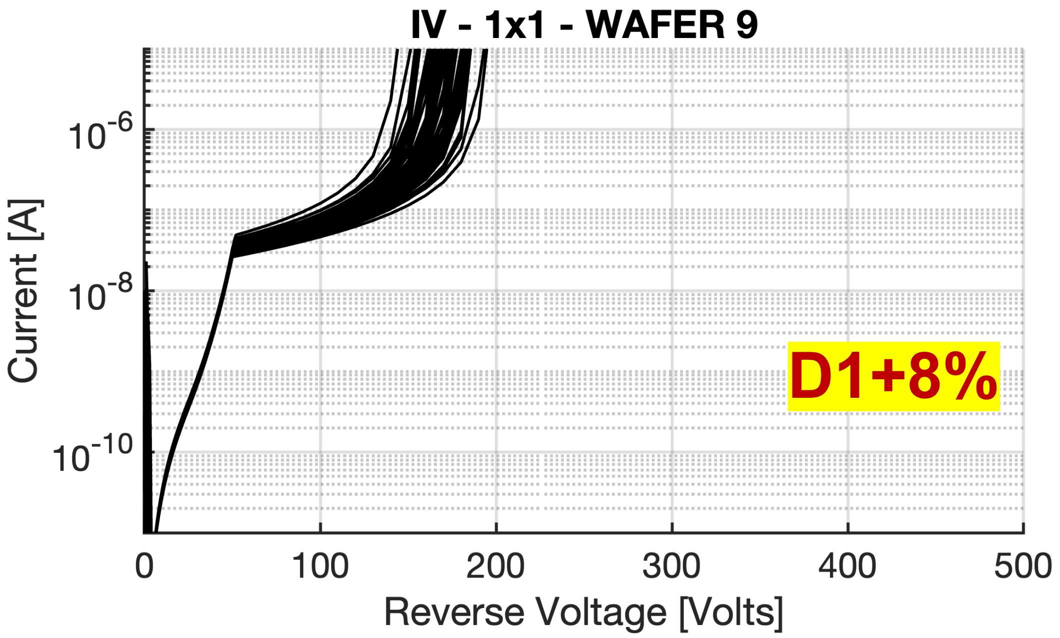




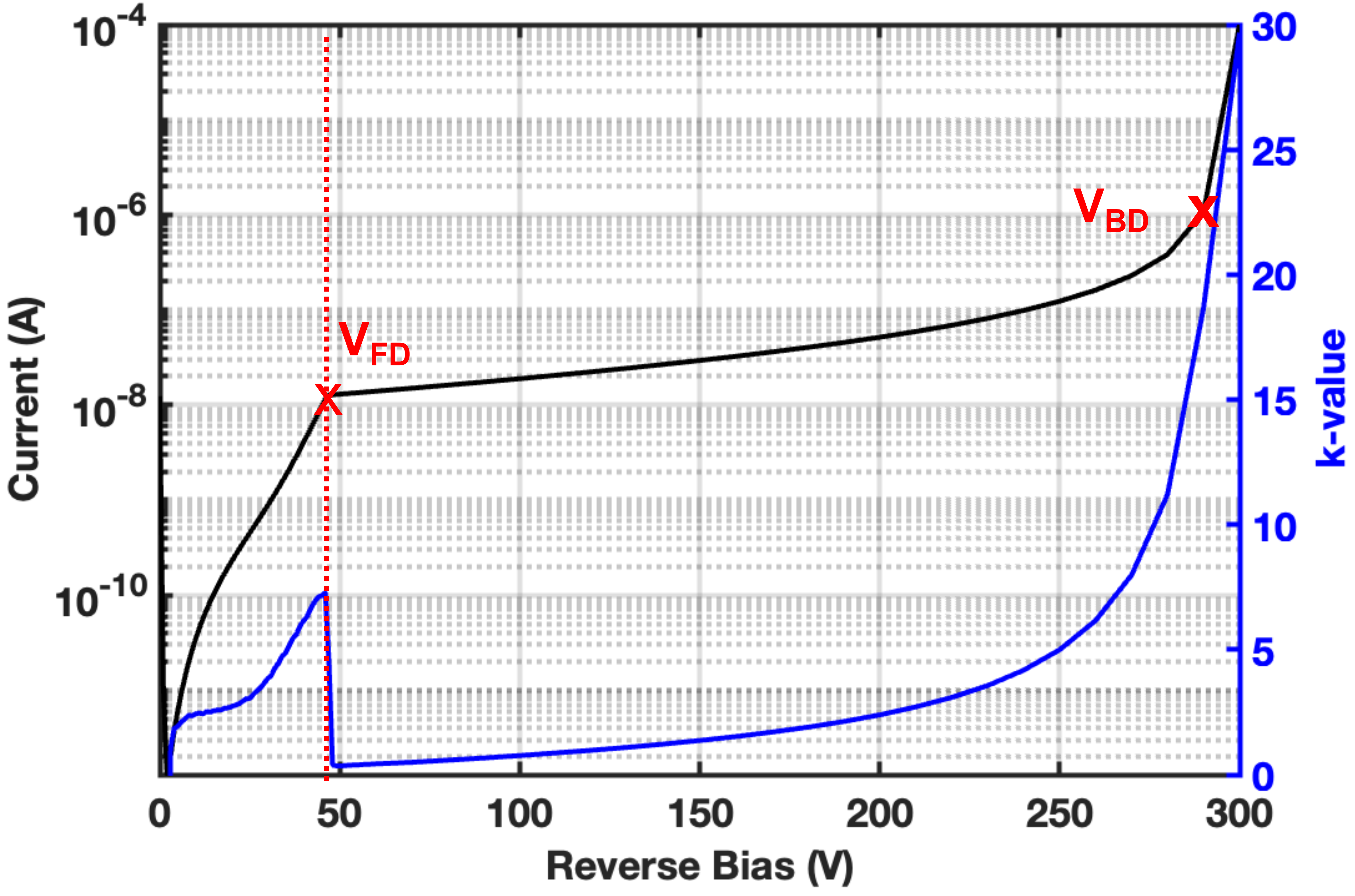




Increasing dose



Characterization Methods: **IV Analysis**



Breakdown was calculated from the k-curve [M. Fernandez, TREDI 2021]

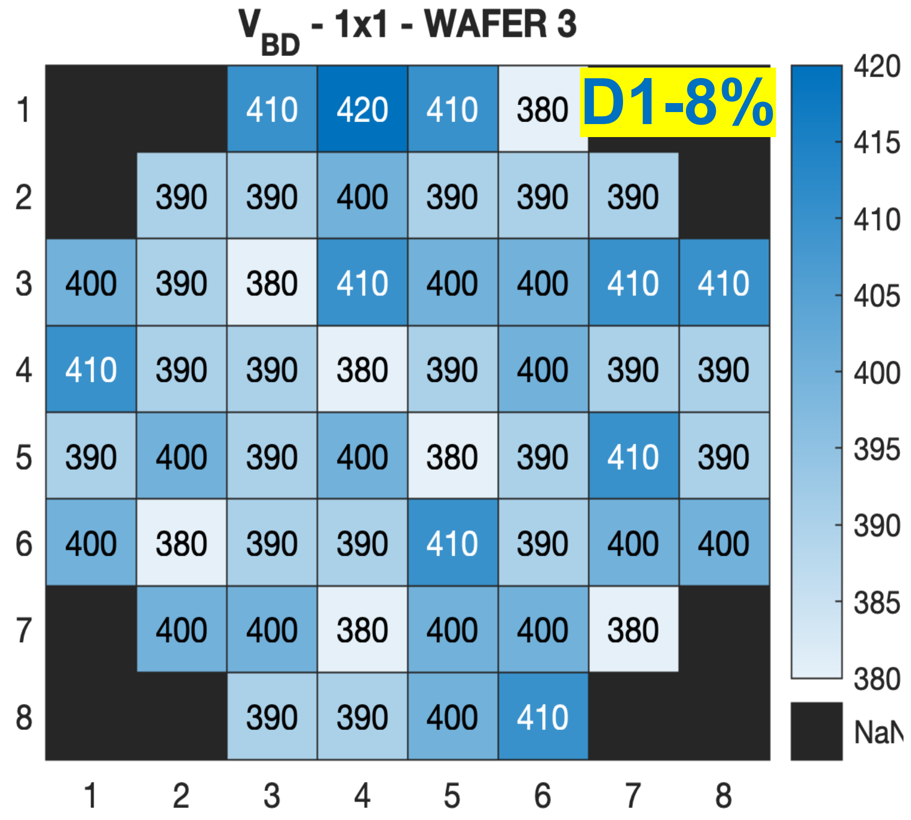
$$K(I,V)=\frac{\Delta I}{\Delta V}\frac{V}{I}$$

V_{BD} = Defined as the last bias point at with K< 20

Gain layer depletion Voltage cannot be not clearly detected by k-method in LGADs with Carbon

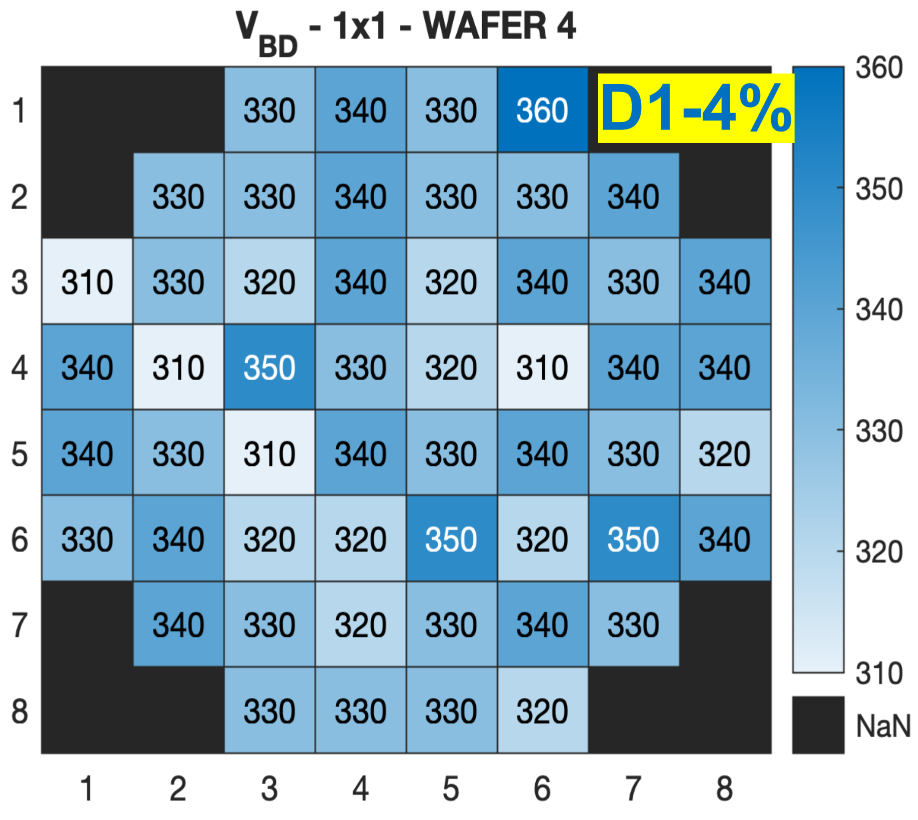
V_{FD} = Defined as the Voltage where K is max in the range 1-60 V (provided that k>5)

PAD IV Analysis : V_{BD} MAPS (DEEP Split)


V_{BD} - 1x1 - WAFER 3

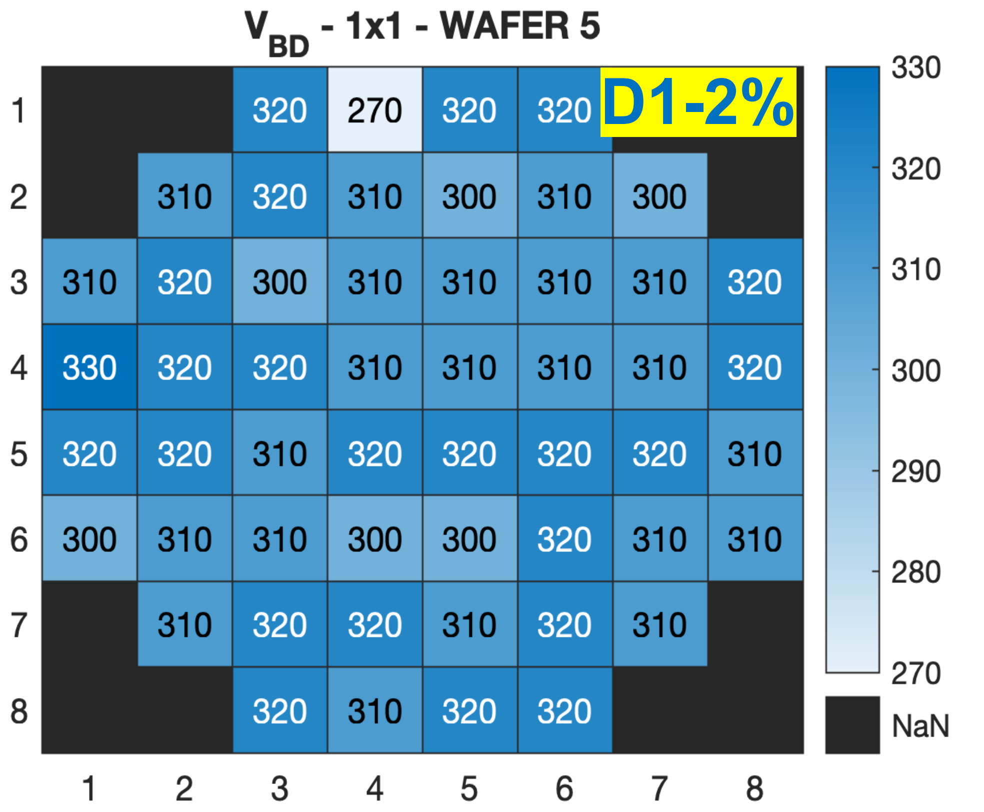
D1-8%

	1	2	3	4	5	6	7	8
1			410	420	410	380		
2		390	390	400	390	390	390	
3	400	390	380	410	400	400	410	410
4	410	390	390	380	390	400	390	390
5	390	400	390	400	380	390	410	390
6	400	380	390	390	410	390	400	400
7		400	400	380	400	400	380	
8			390	390	400	410		


V_{BD} - 1x1 - WAFER 4

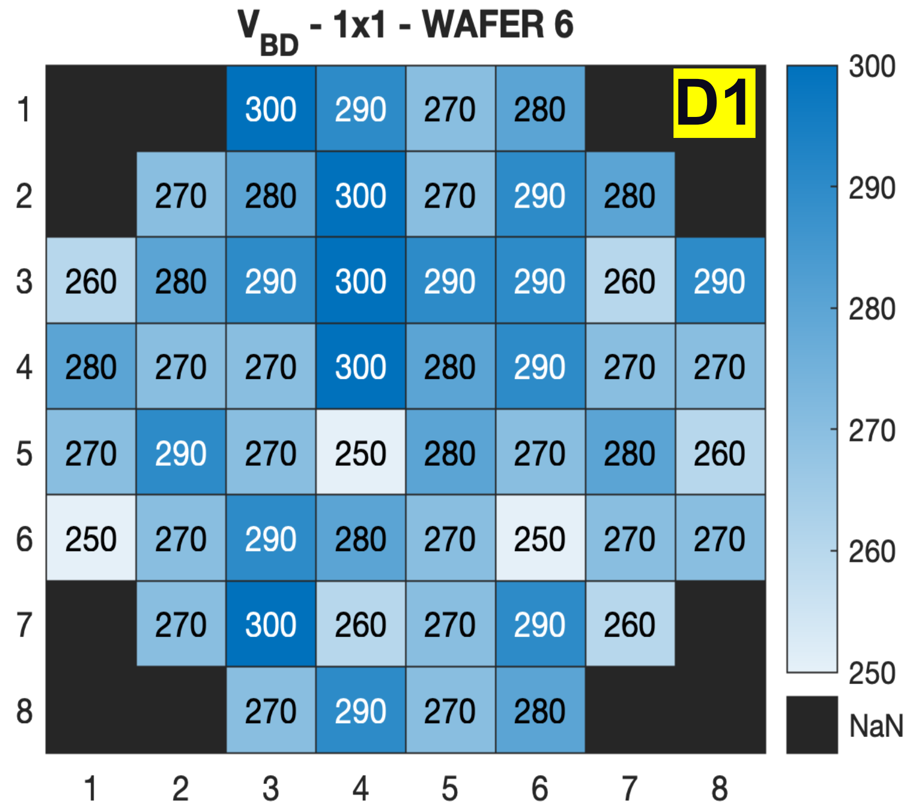
D1-4%

	1	2	3	4	5	6	7	8
1			330	340	330	360		
2		330	330	340	330	330	340	
3	310	330	320	340	320	340	330	340
4	340	310	350	330	320	310	340	340
5	340	330	310	340	330	340	330	320
6	330	340	320	320	350	320	350	340
7		340	330	320	330	340	330	
8			330	330	330	320		


V_{BD} - 1x1 - WAFER 5

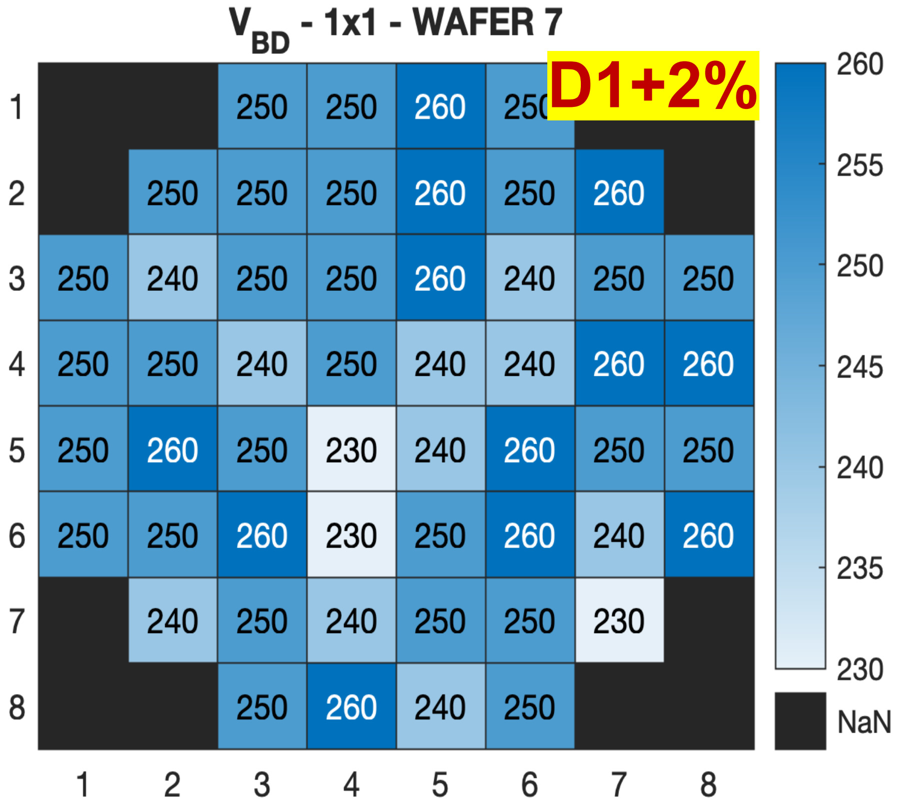
D1-2%

	1	2	3	4	5	6	7	8
1			320	270	320	320		
2		310	320	310	300	310	300	
3	310	320	300	310	310	310	310	320
4	330	320	320	310	310	310	310	320
5	320	320	310	320	320	320	320	310
6	300	310	310	300	300	320	310	310
7		310	320	320	310	320	310	
8			320	310	320	320		


V_{BD} - 1x1 - WAFER 6

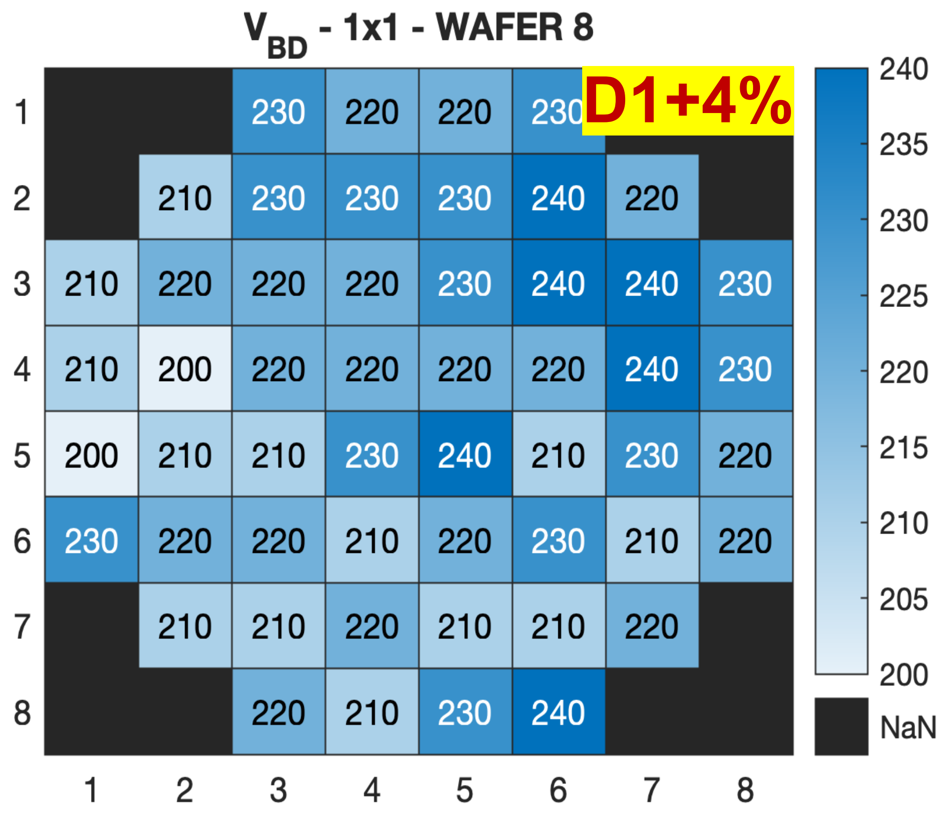
D1

	1	2	3	4	5	6	7	8
1			300	290	270	280		
2		270	280	300	270	290	280	
3	260	280	290	300	290	290	260	290
4	280	270	270	300	280	290	270	270
5	270	290	270	250	280	270	280	260
6	250	270	290	280	270	250	270	270
7		270	300	260	270	290	260	
8			270	290	270	280		


V_{BD} - 1x1 - WAFER 7

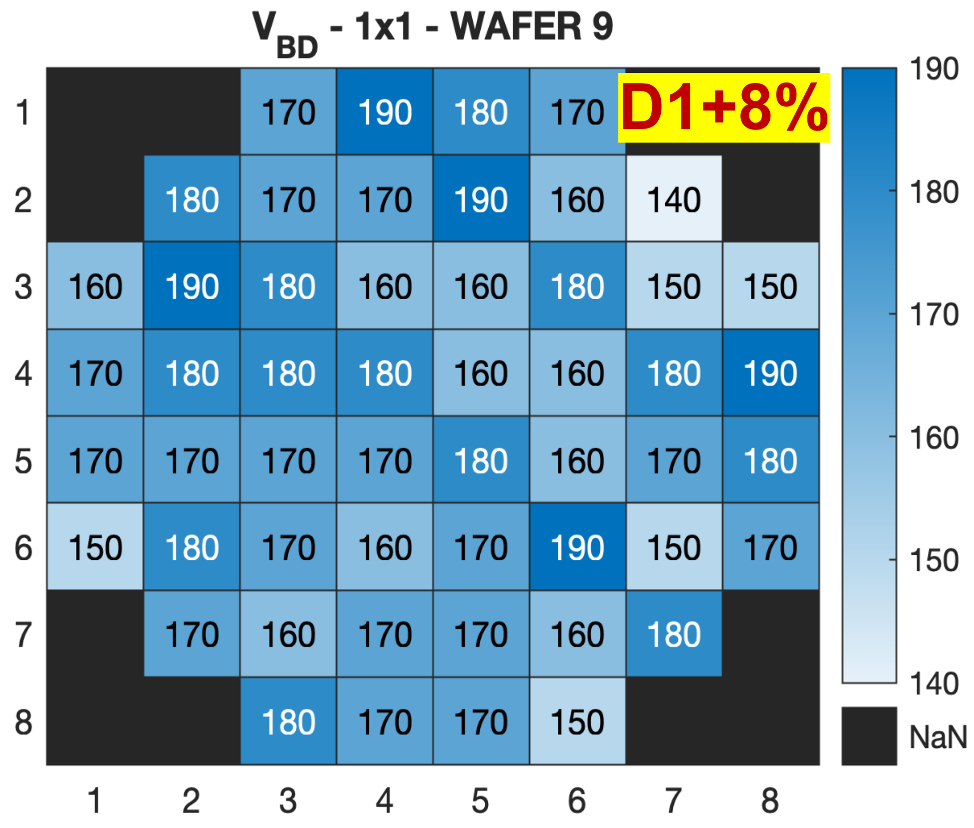
D1+2%

	1	2	3	4	5	6	7	8
1			250	250	260	250		
2		250	250	250	260	250	260	
3	250	240	250	250	260	240	250	250
4	250	250	240	250	240	240	260	260
5	250	260	250	230	240	260	250	250
6	250	250	260	230	250	260	240	260
7		240	250	240	250	250	230	
8			250	260	240	250		


V_{BD} - 1x1 - WAFER 8

D1+4%

	1	2	3	4	5	6	7	8
1			230	220	220	230		
2		210	230	230	230	240	220	
3	210	220	220	220	230	240	240	230
4	210	200	220	220	220	220	240	230
5	200	210	210	230	240	210	230	220
6	230	220	220	210	220	230	210	220
7		210	210	220	210	210	220	
8			220	210	230	240		

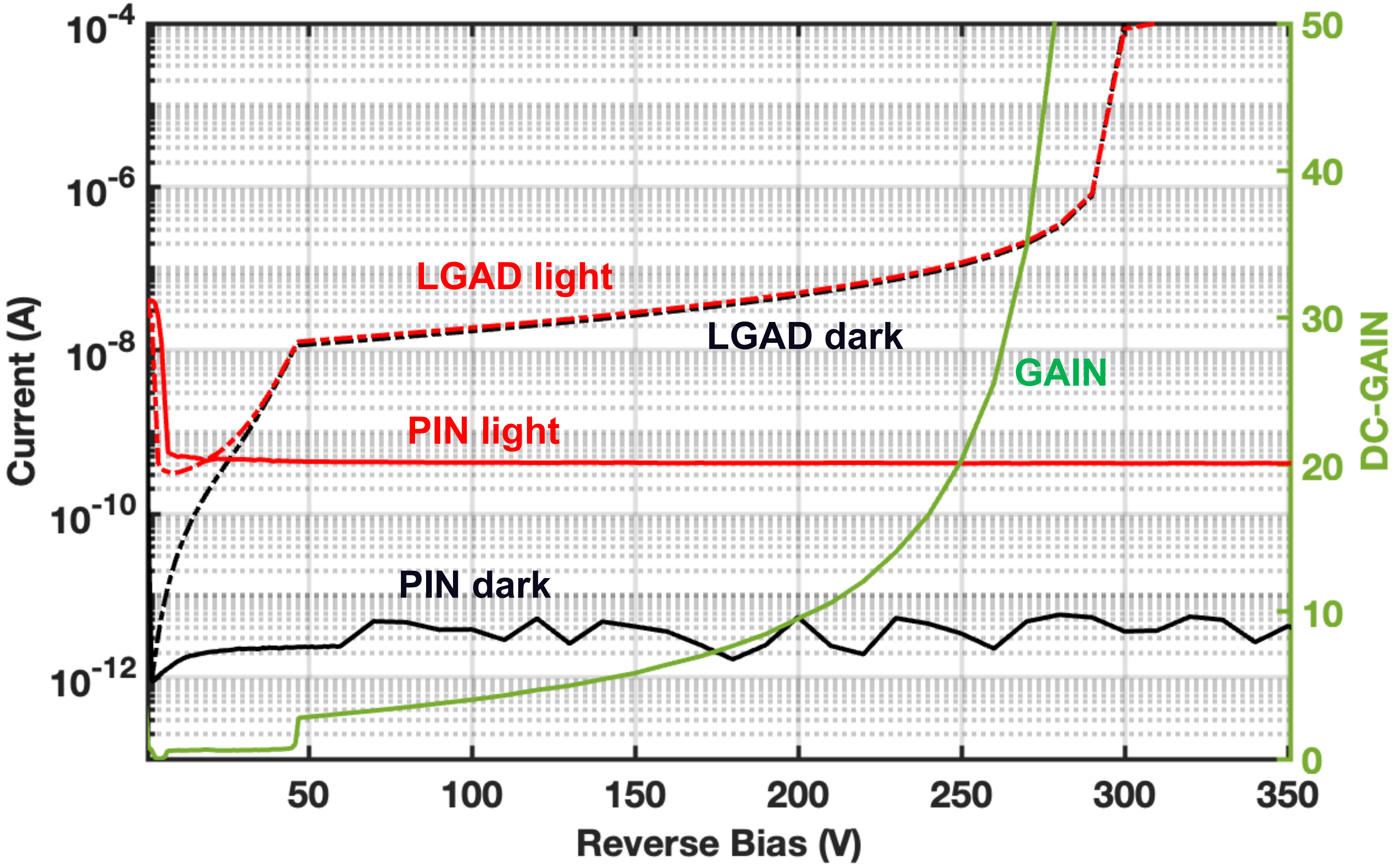

V_{BD} - 1x1 - WAFER 9

D1+8%

	1	2	3	4	5	6	7	8
1			170	190	180	170		
2		180	170	170	190	160	140	
3	160	190	180	160	160	180	150	150
4	170	180	180	180	160	160	180	190
5	170	170	170	170	180	160	170	180
6	150	180	170	160	170	190	150	170
7		170	160	170	170	160	180	
8			180	170	170	150		

The V_{BD} distribution at wafer level seems quite random without any visible and reproducible pattern

Characterization Methods: **DC-GAIN**



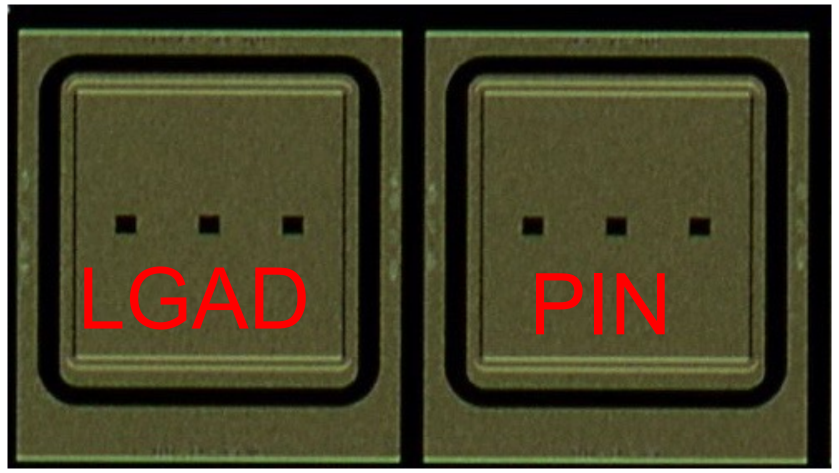
The 1x1 PIN/PAD have been measured with automatic prober under DC-illumination with a NIR LED at 950 nm.

$$G^{DC} = \frac{I_{LGAD}^{Ill} - I_{LGAD}^{Dark}}{I_{PIN}^{Ill} - I_{PIN}^{Dark}}$$

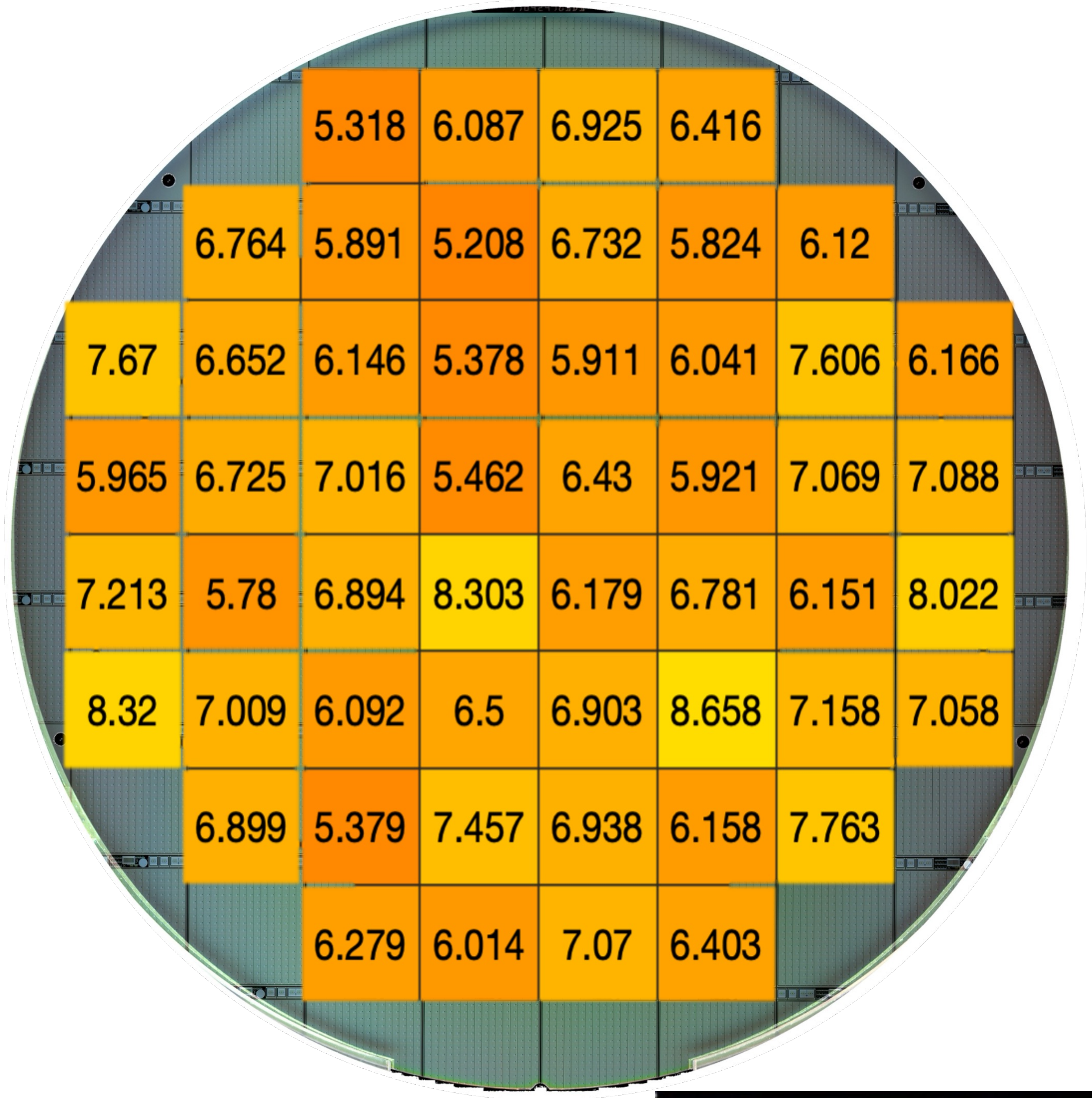
DC-Gain of the LGAD PAD is calculated considering the adjacent PIN and corrected by Dark

Low-level photogeneration (corresponds to ~ 20 mips/μm^2/sec) to avoid charge-screening

Illumination through 3 holes in the metal



Characterization Methods: **DC-GAIN**



		5.318	6.087	6.925	6.416		
	6.764	5.891	5.208	6.732	5.824	6.12	
7.67	6.652	6.146	5.378	5.911	6.041	7.606	6.166
5.965	6.725	7.016	5.462	6.43	5.921	7.069	7.088
7.213	5.78	6.894	8.303	6.179	6.781	6.151	8.022
8.32	7.009	6.092	6.5	6.903	8.658	7.158	7.058
	6.899	5.379	7.457	6.938	6.158	7.763	
		6.279	6.014	7.07	6.403		

Wafer-level GAIN MAP

Each square is a shot.
1 PIN/PAD couple measured per each shot

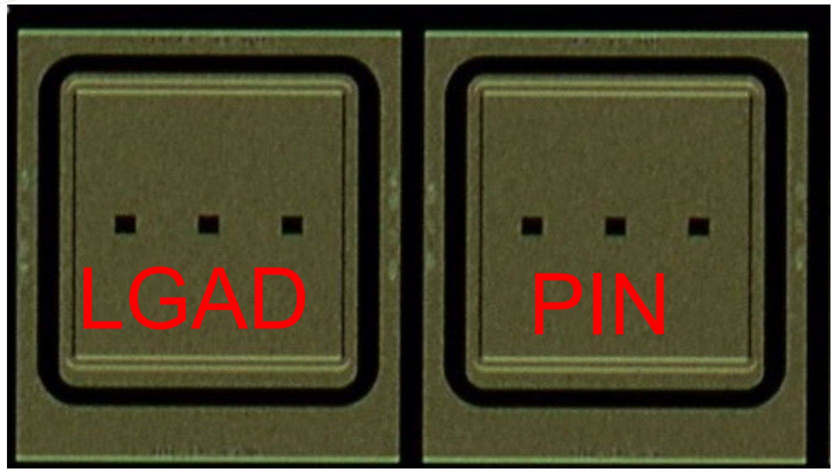
The 1x1 PIN/PAD have been measured with automatic prober under DC-illumination with

$$D - I_{LGAD}^{Dark}$$
$$- I_{PIN}^{Dark}$$

DC-Gain of the LGAD PAD is calculated considering the adjacent PIN and corrected by Dark

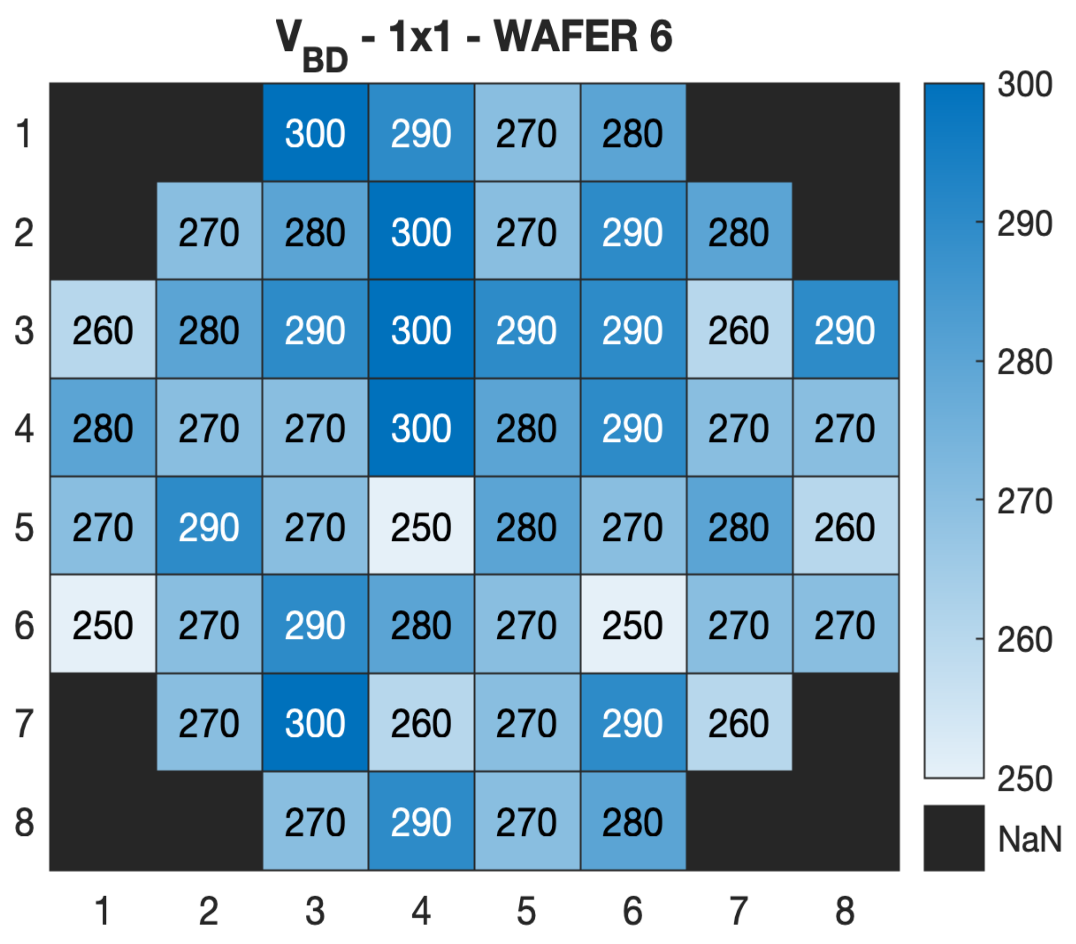
Low-level photogeneration (corresponds to ~ 20 mips/µm^2/sec) to avoid charge-screening

Illumination through 3 holes in the metal



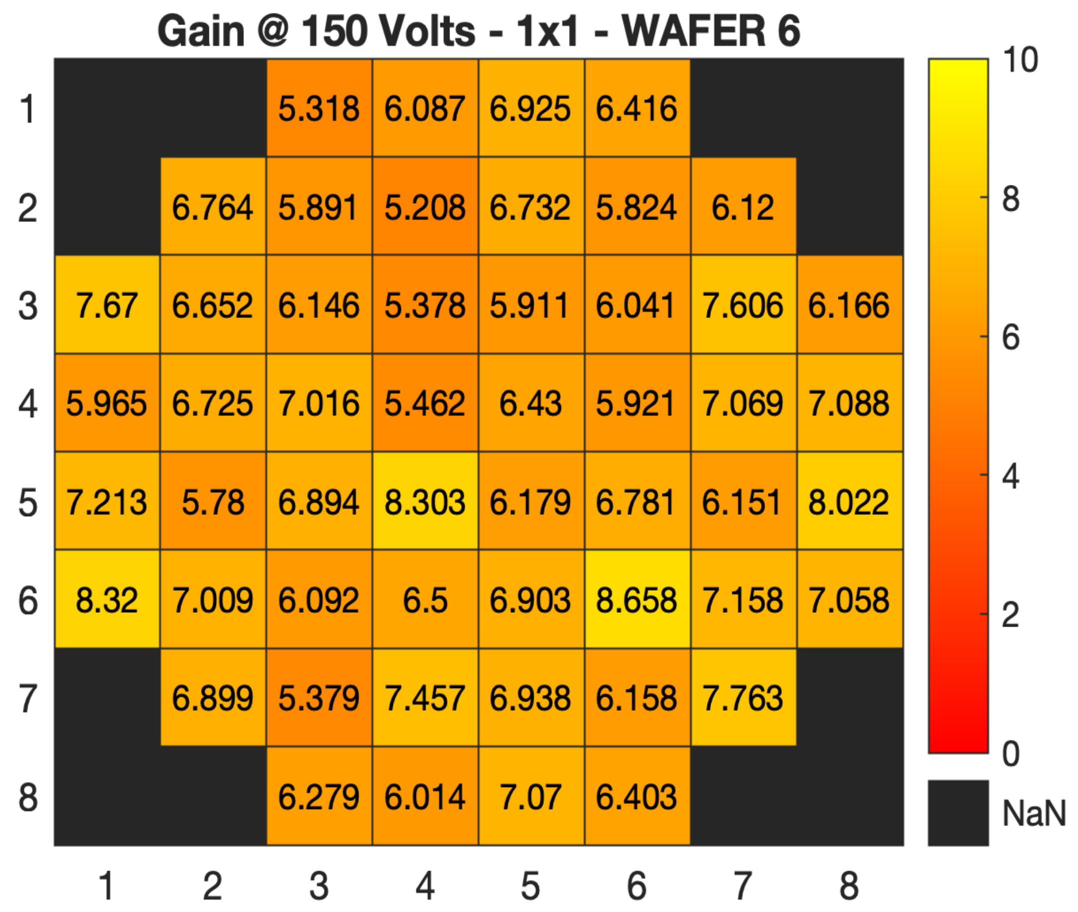
PAD IV Analysis : BD & VGL MAP

WAFER 6: DEEP PGAIN DOSE = 1.0



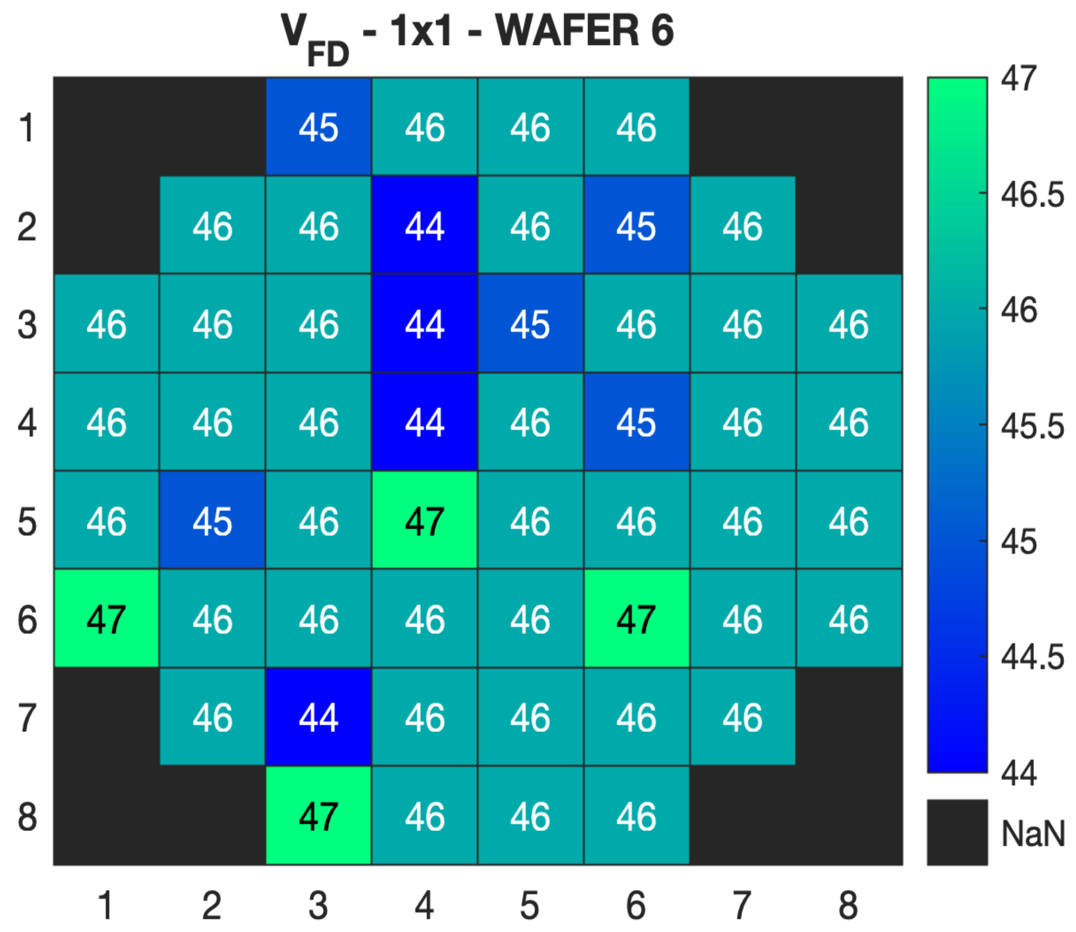
V_{BD} - 1x1 - WAFER 6

	1	2	3	4	5	6	7	8
1			300	290	270	280		
2		270	280	300	270	290	280	
3	260	280	290	300	290	290	260	290
4	280	270	270	300	280	290	270	270
5	270	290	270	250	280	270	280	260
6	250	270	290	280	270	250	270	270
7		270	300	260	270	290	260	
8			270	290	270	280		



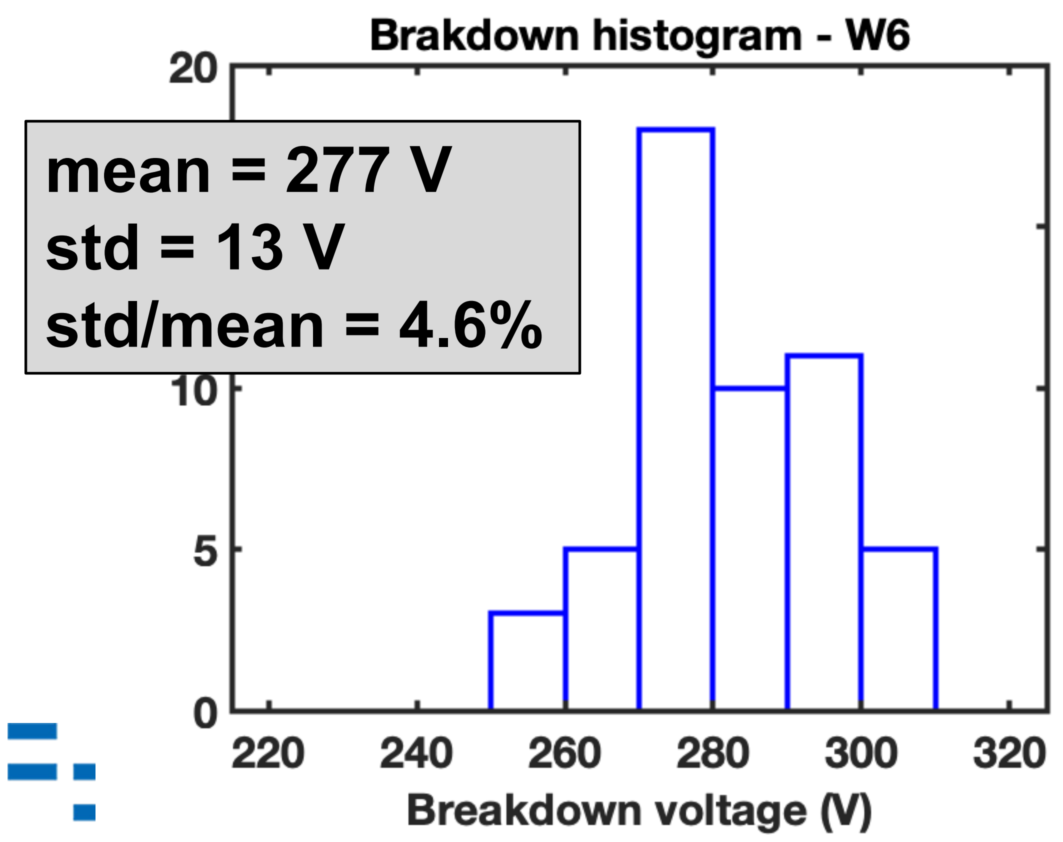
Gain @ 150 Volts - 1x1 - WAFER 6

	1	2	3	4	5	6	7	8
1			5.318	6.087	6.925	6.416		
2		6.764	5.891	5.208	6.732	5.824	6.12	
3	7.67	6.652	6.146	5.378	5.911	6.041	7.606	6.166
4	5.965	6.725	7.016	5.462	6.43	5.921	7.069	7.088
5	7.213	5.78	6.894	8.303	6.179	6.781	6.151	8.022
6	8.32	7.009	6.092	6.5	6.903	8.658	7.158	7.058
7		6.899	5.379	7.457	6.938	6.158	7.763	
8			6.279	6.014	7.07	6.403		



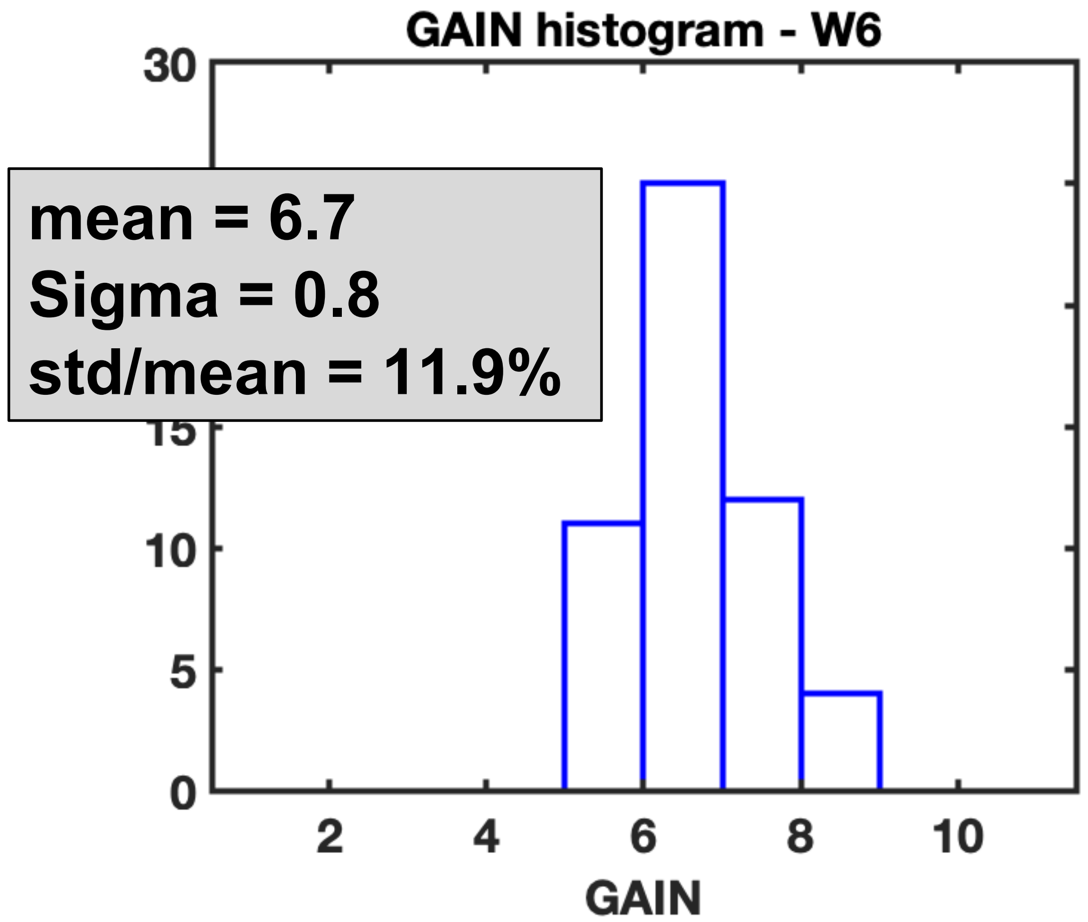
V_{FD} - 1x1 - WAFER 6

	1	2	3	4	5	6	7	8
1			45	46	46	46		
2		46	46	44	46	45	46	
3	46	46	46	44	45	46	46	46
4	46	46	46	44	46	45	46	46
5	46	45	46	47	46	46	46	46
6	47	46	46	46	46	47	46	46
7		46	44	46	46	46	46	
8			47	46	46	46		



Brakdown histogram - W6

mean = 277 V
std = 13 V
std/mean = 4.6%



GAIN histogram - W6

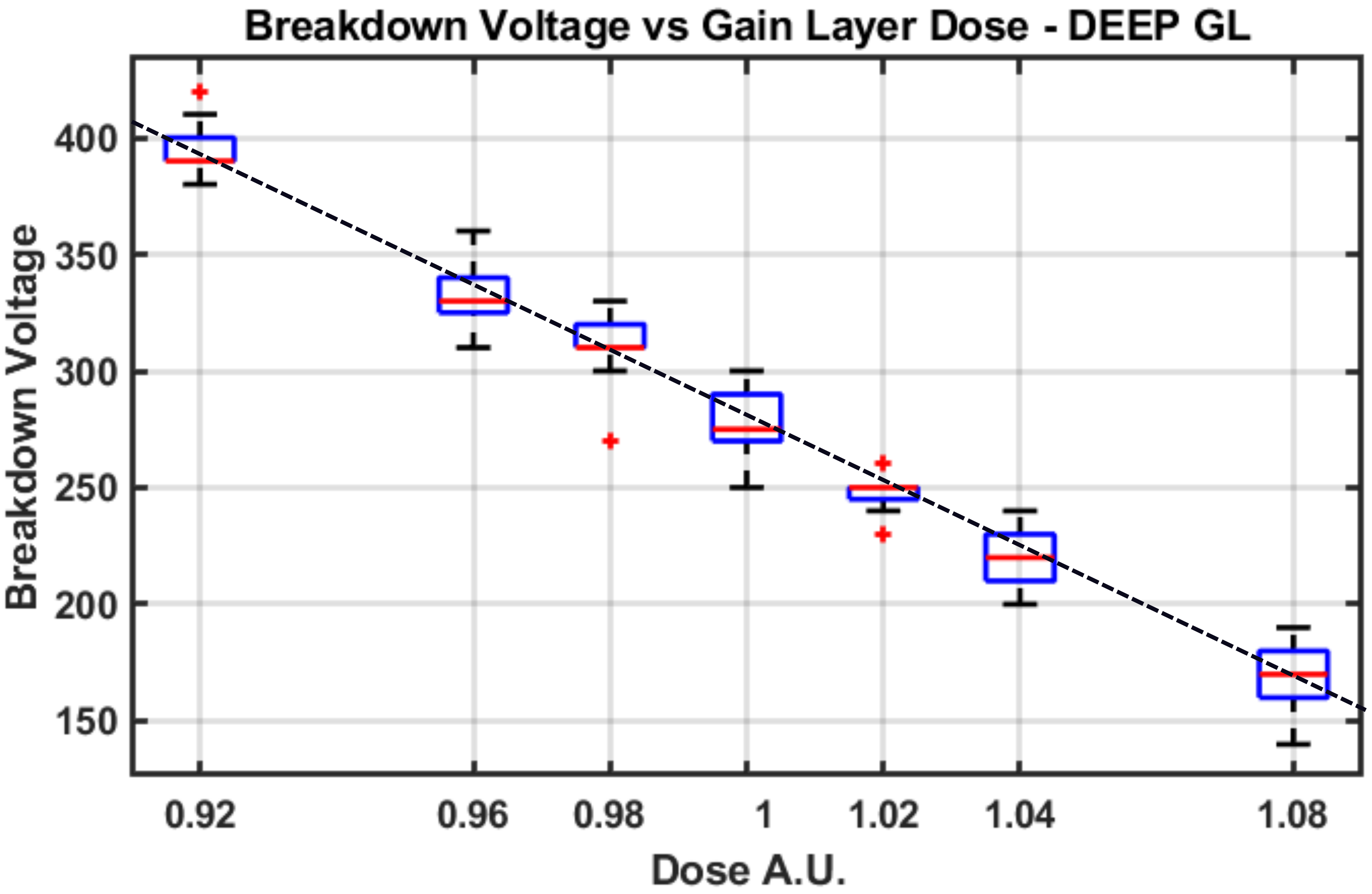
mean = 6.7
Sigma = 0.8
std/mean = 11.9%

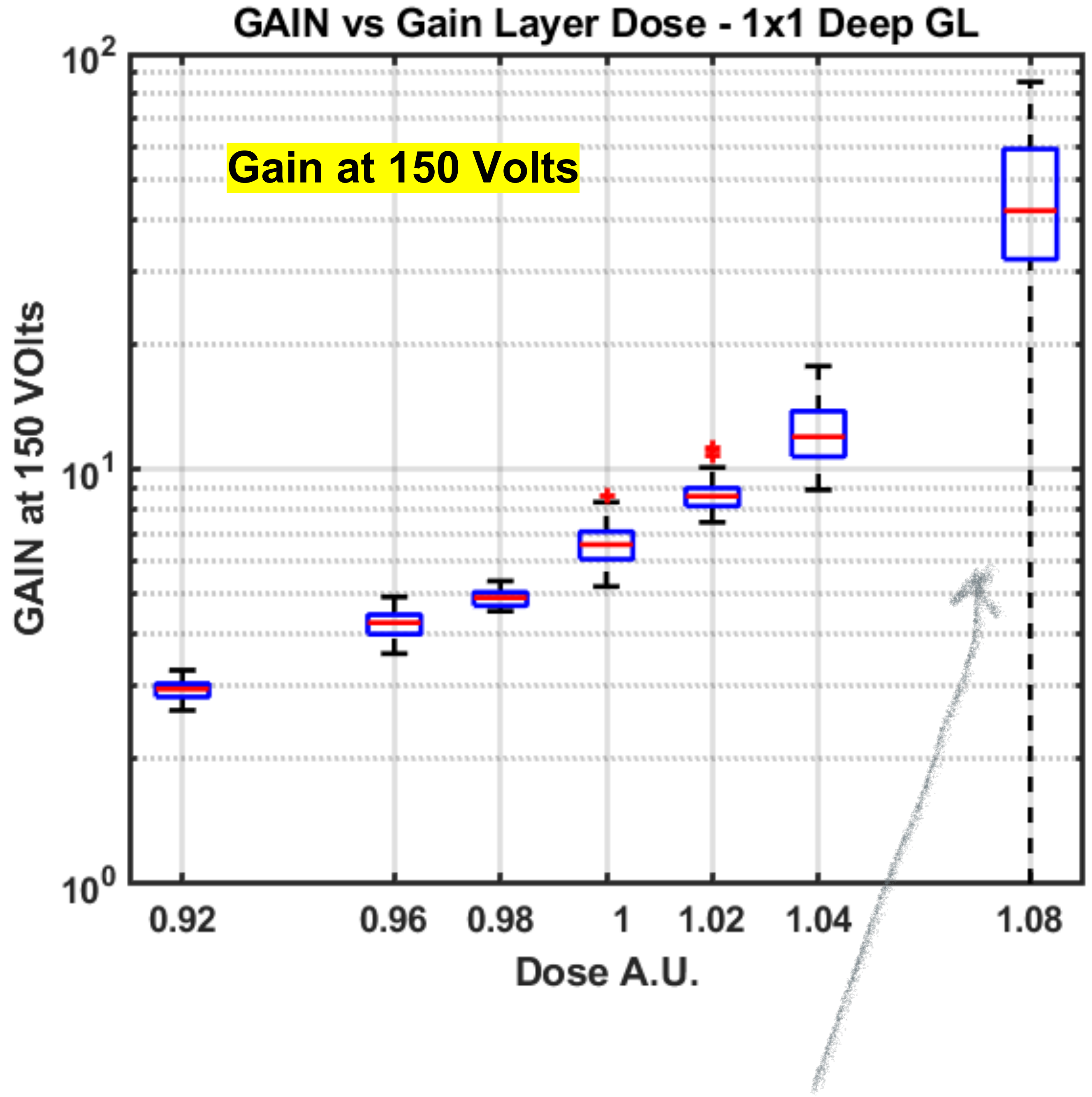
20% Tails exclusion

80% Devices **V_{BD}** in the range **260-293 Volts**

80% devices **Gain** in the range **5.7 – 7.7**

PAD IV Analysis : V_{BD} and GAIN vs PGAIN Dose (DEEP Split)

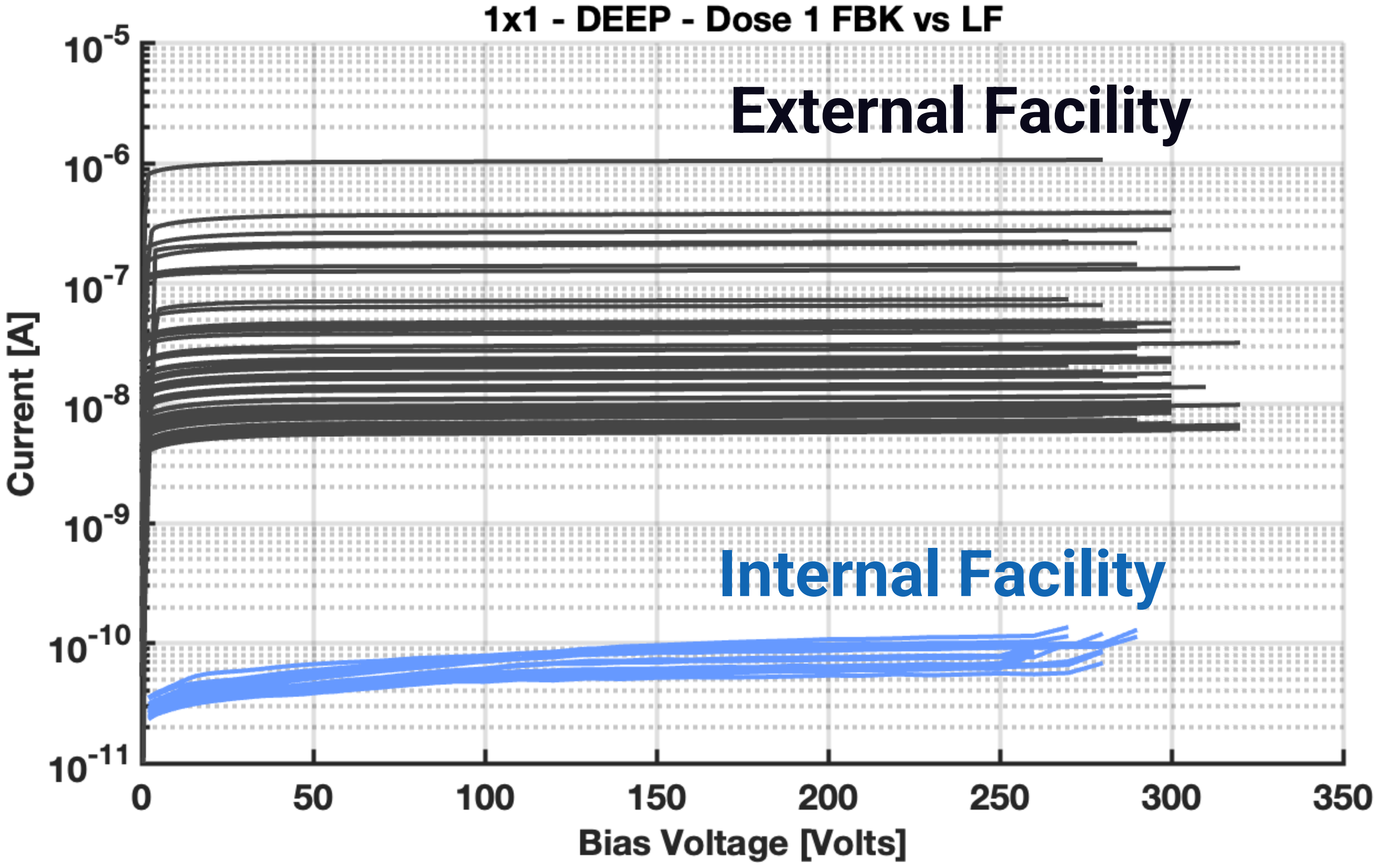




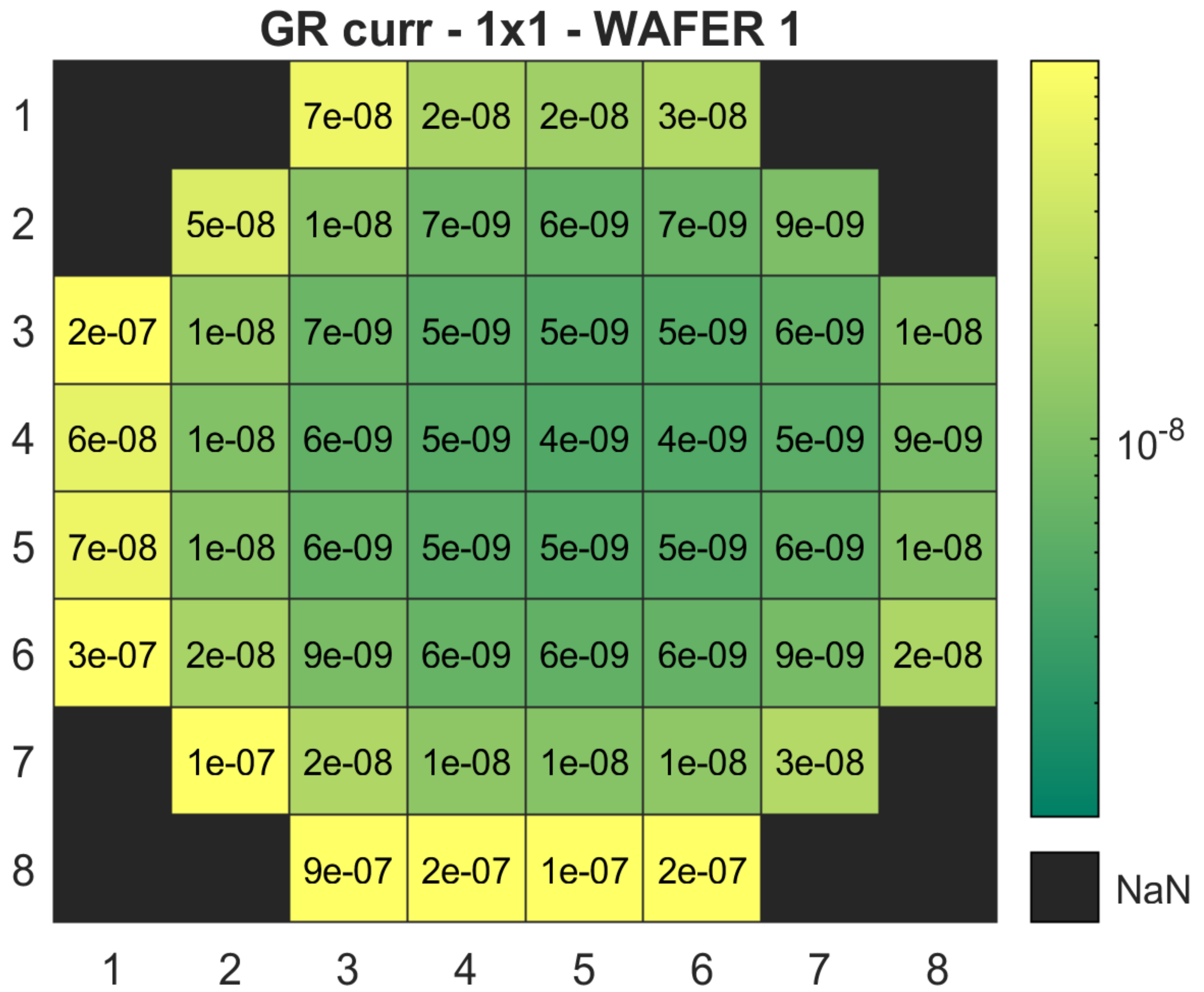
BDV very close to 150 V
(bad gain estimation)

- BDV almost linear with Dose (~ 15 Volts / 1% Dose variation)
- Gain more than exponential with Dose

PAD IV Analysis : Guard Ring Current



GR curr - 1x1 - WAFER 1

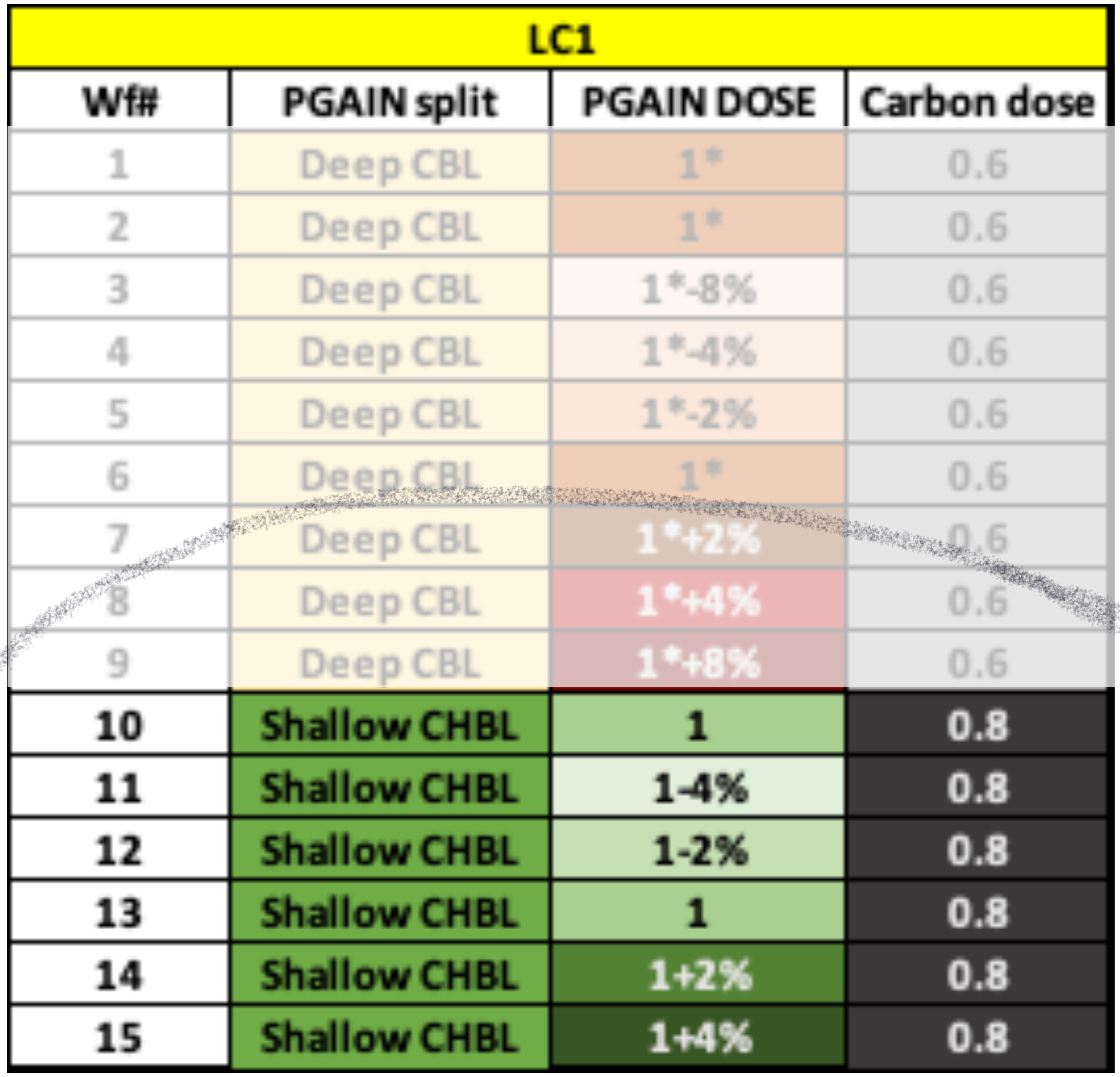


	1	2	3	4	5	6	7	8
1			7e-08	2e-08	2e-08	3e-08		
2		5e-08	1e-08	7e-09	6e-09	7e-09	9e-09	
3	2e-07	1e-08	7e-09	5e-09	5e-09	5e-09	6e-09	1e-08
4	6e-08	1e-08	6e-09	5e-09	4e-09	4e-09	5e-09	9e-09
5	7e-08	1e-08	6e-09	5e-09	5e-09	5e-09	6e-09	1e-08
6	3e-07	2e-08	9e-09	6e-09	6e-09	6e-09	9e-09	2e-08
7		1e-07	2e-08	1e-08	1e-08	1e-08	3e-08	
8			9e-07	2e-07	1e-07	2e-07		

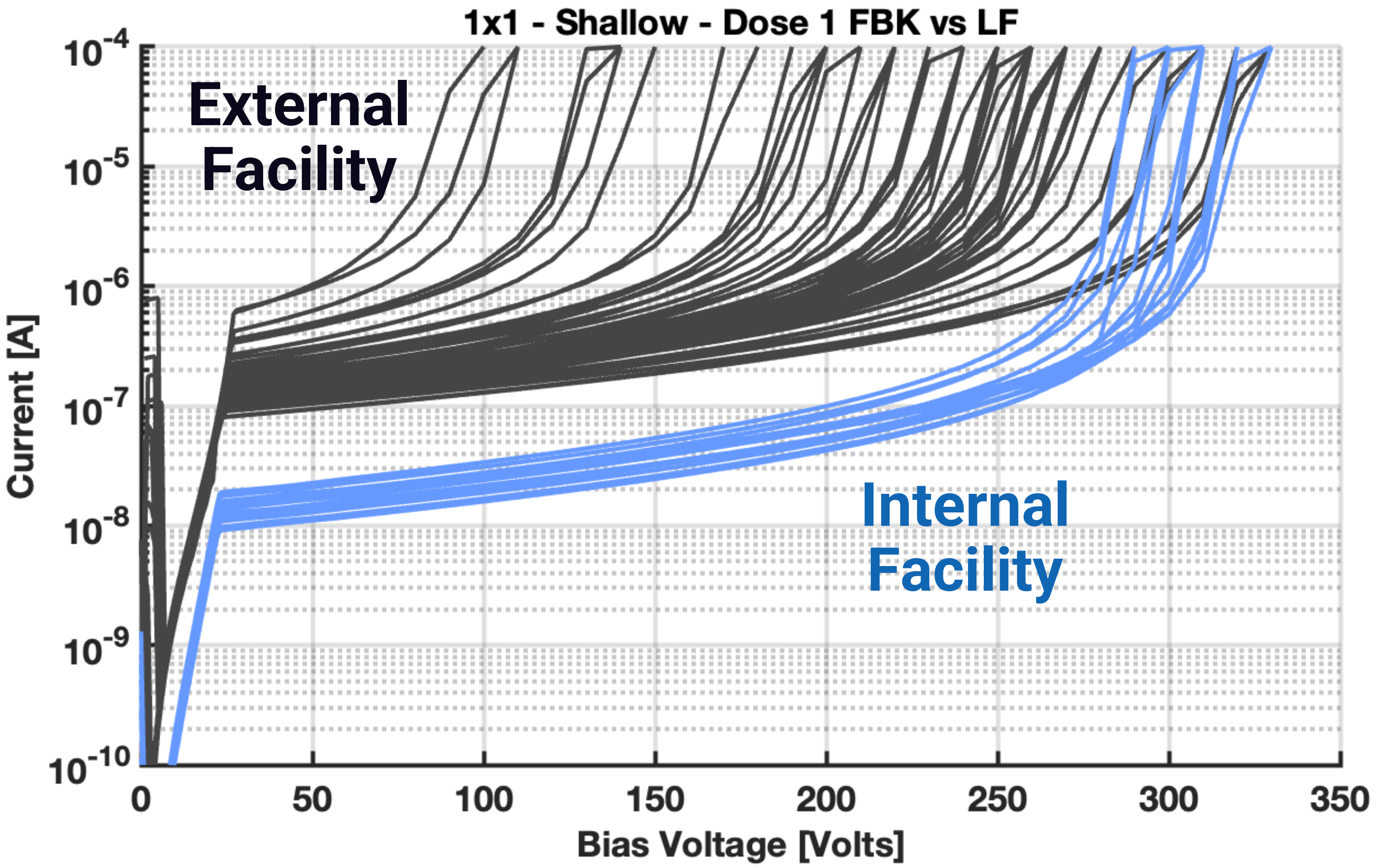
GR Current much larger than expected

- Large spread of GR current on wafer level (higher at the border)
- This effect already occurred in the past in internal productions at FBK and explained with type inversion of the HR epi layer
- It should be solved by increasing the doping level the starting material

PAD IV Analysis : Standard (Shallow) Gain Layer



LC1			
Wf#	**PGAIN split**	**PGAIN DOSE**	**Carbon dose**
1	Deep CBL	1*	0.6
2	Deep CBL	1*	0.6
3	Deep CBL	1*-8%	0.6
4	Deep CBL	1*-4%	0.6
5	Deep CBL	1*-2%	0.6
6	Deep CBL	1*	0.6
7	Deep CBL	1*+2%	0.6
8	Deep CBL	1*+4%	0.6
9	Deep CBL	1*+8%	0.6
10	Shallow CHBL	1	0.8
11	Shallow CHBL	1-4%	0.8
12	Shallow CHBL	1-2%	0.8
13	Shallow CHBL	1	0.8
14	Shallow CHBL	1+2%	0.8
15	Shallow CHBL	1+4%	0.8



Shallow PGAIN showed some issues already not-explained:

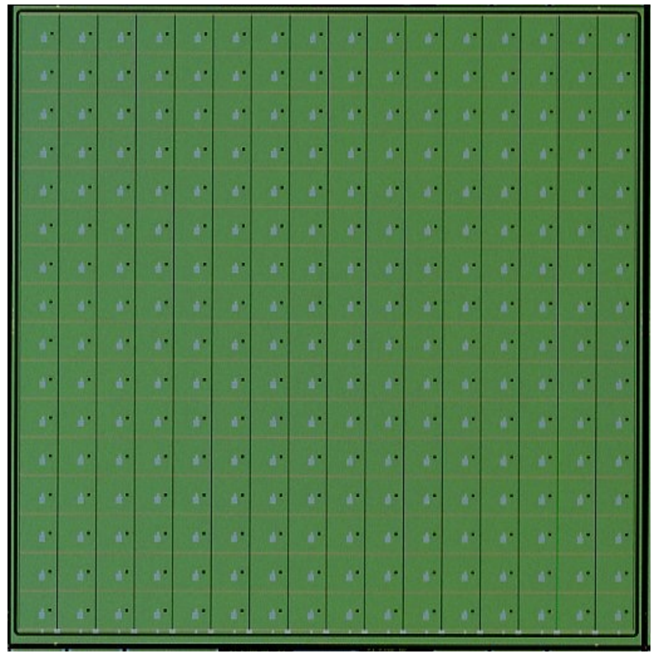
- Higher Dark Current
- Large spread of V_{BD} and Gain on the wafer

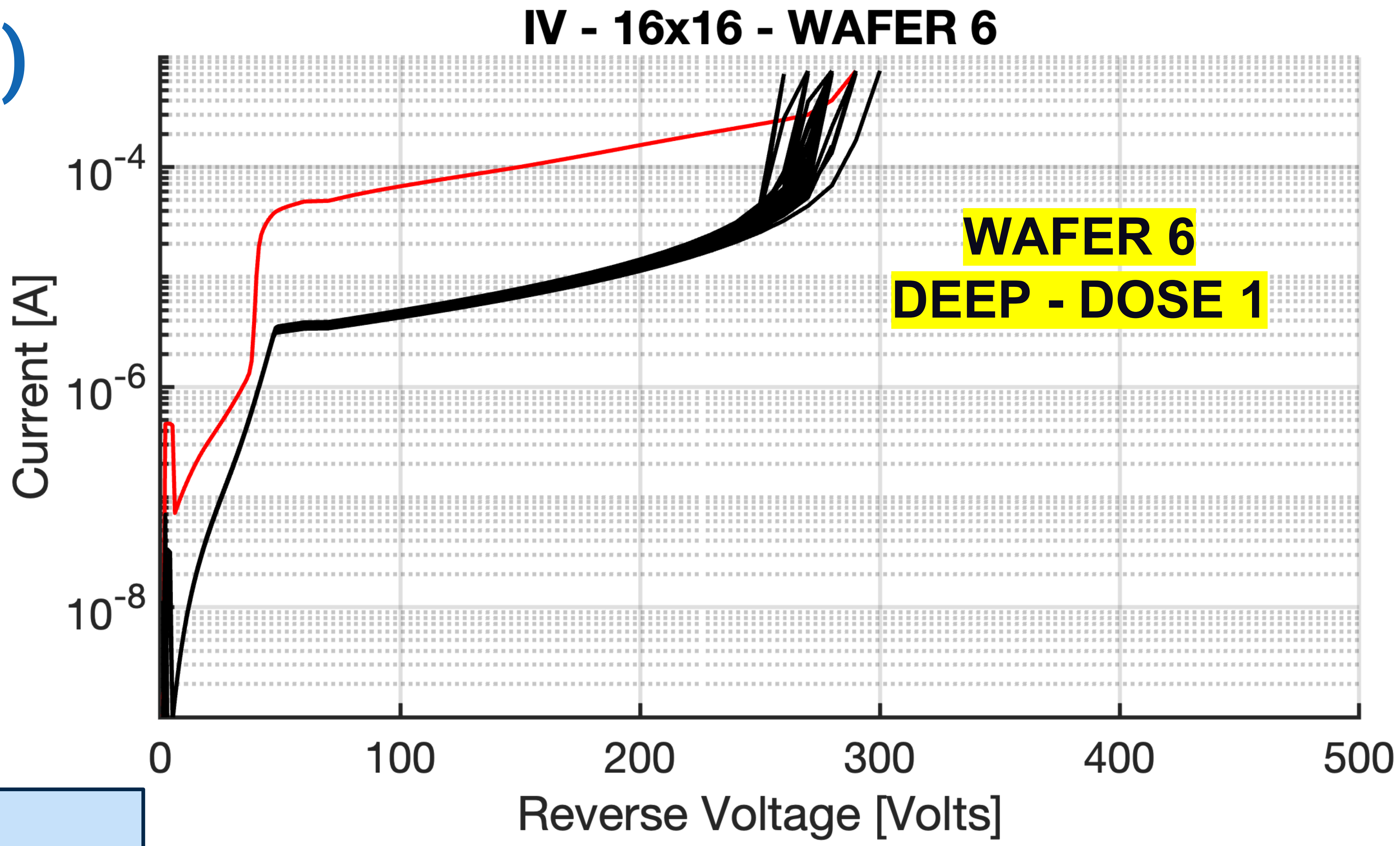
Analysis of the measurements and cross-check of the process still ongoing

16x16 Sensors (DEEP Split)

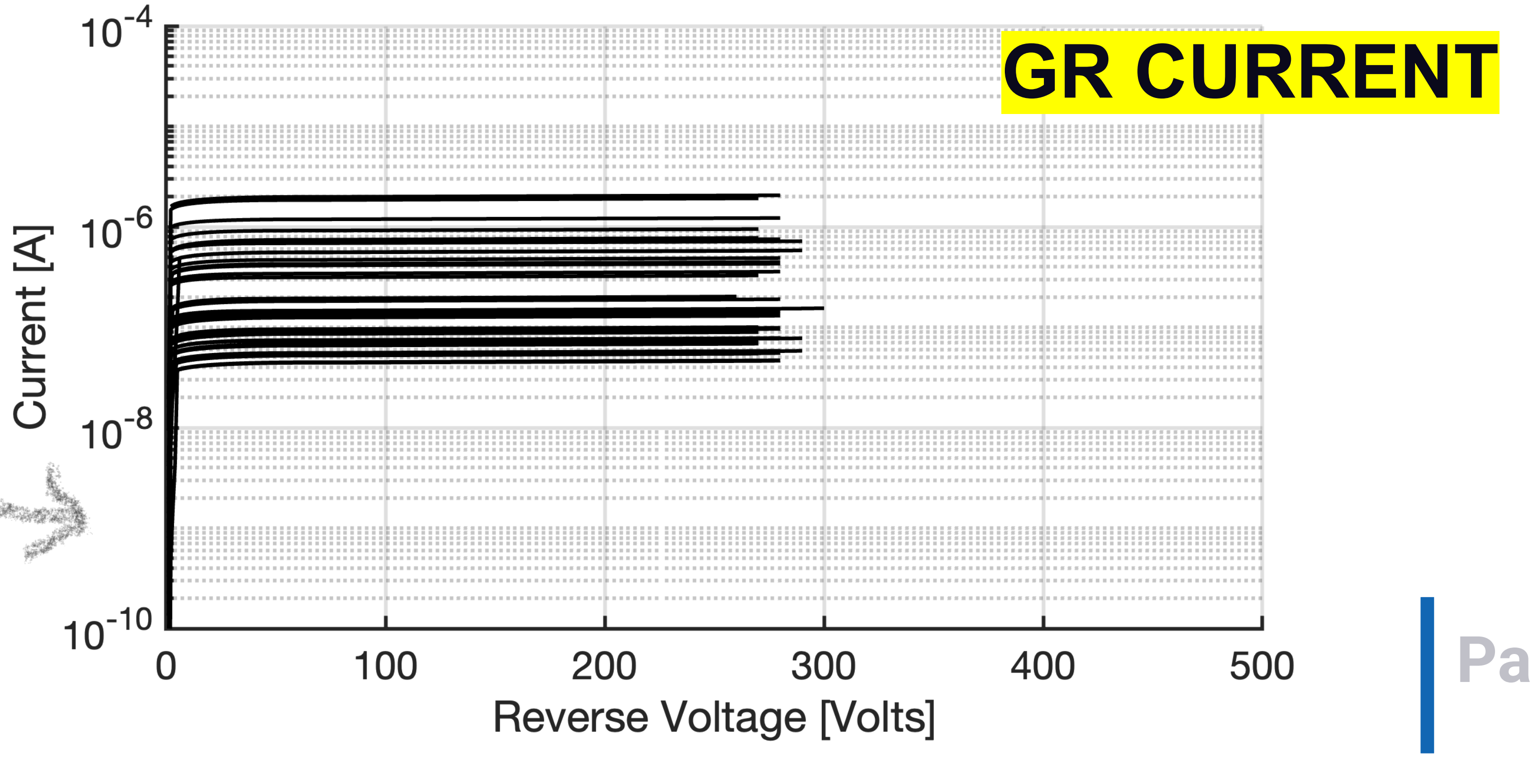
Measurement conditions

- All the 256 pixels shorted to a single channel
- GR on a separate channel
- Bias form the Wafer backside

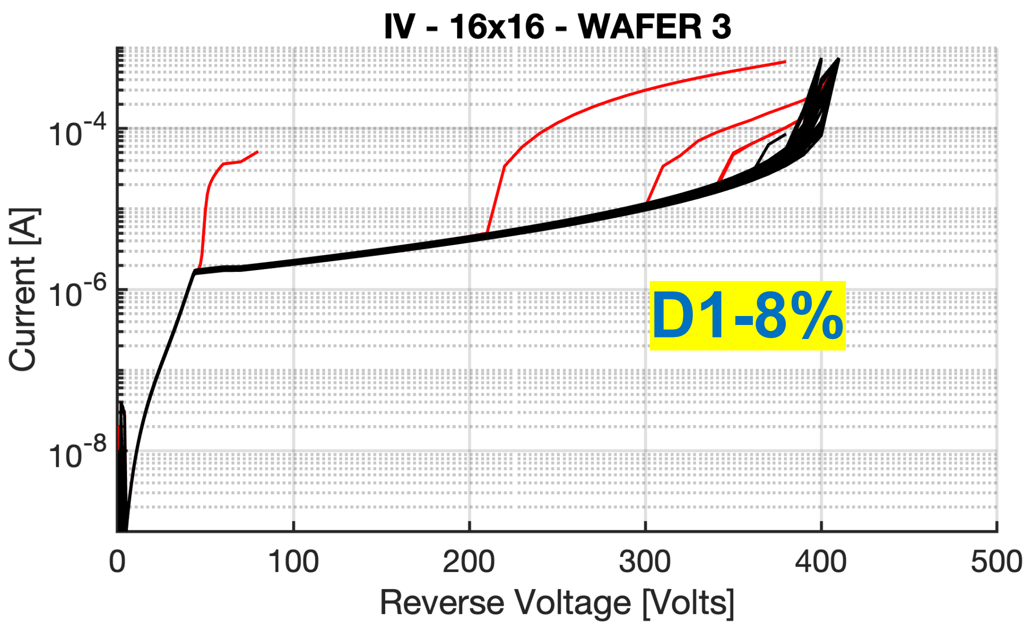


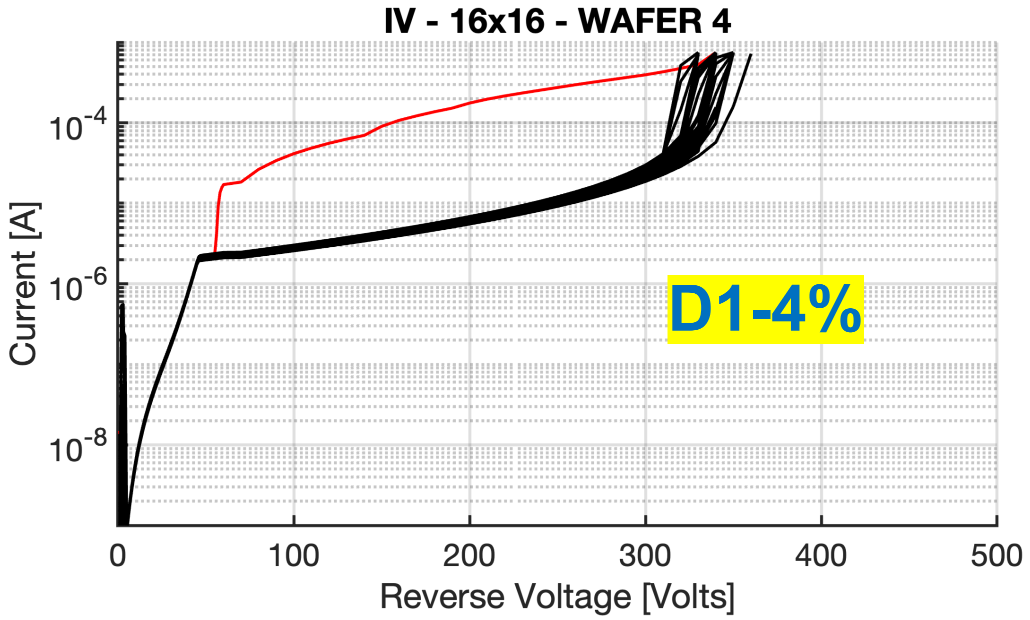


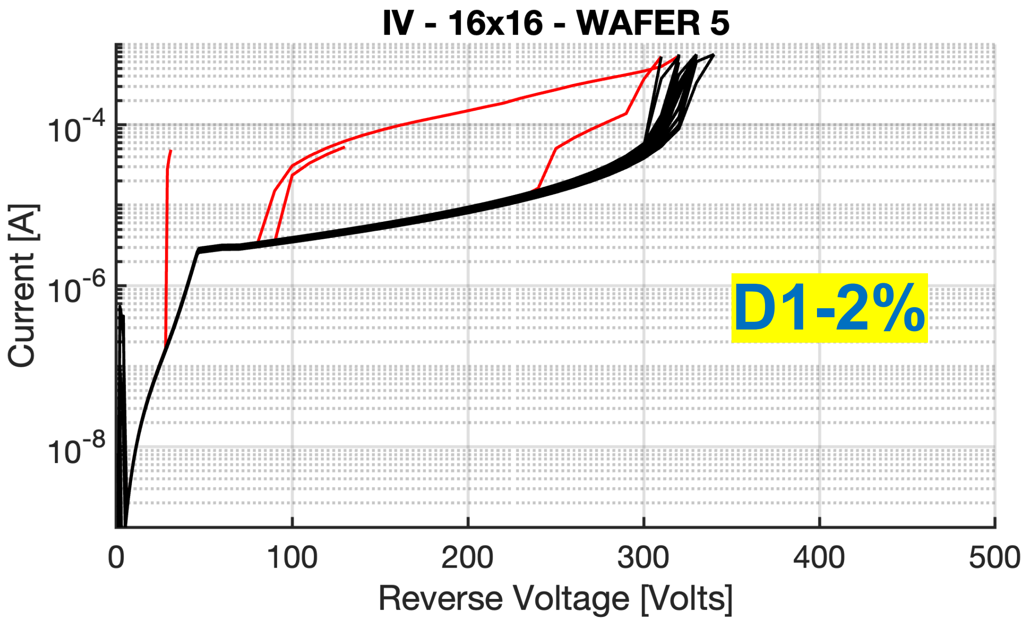
- Each curve represents a single device
- Total current ~1e-5A consistent with the sum of the single PADs (single pad ~ 1e-7 A)
- Dark = Good ones
- Red ones = Bad ones (manually selected)
- GR also shows high current level

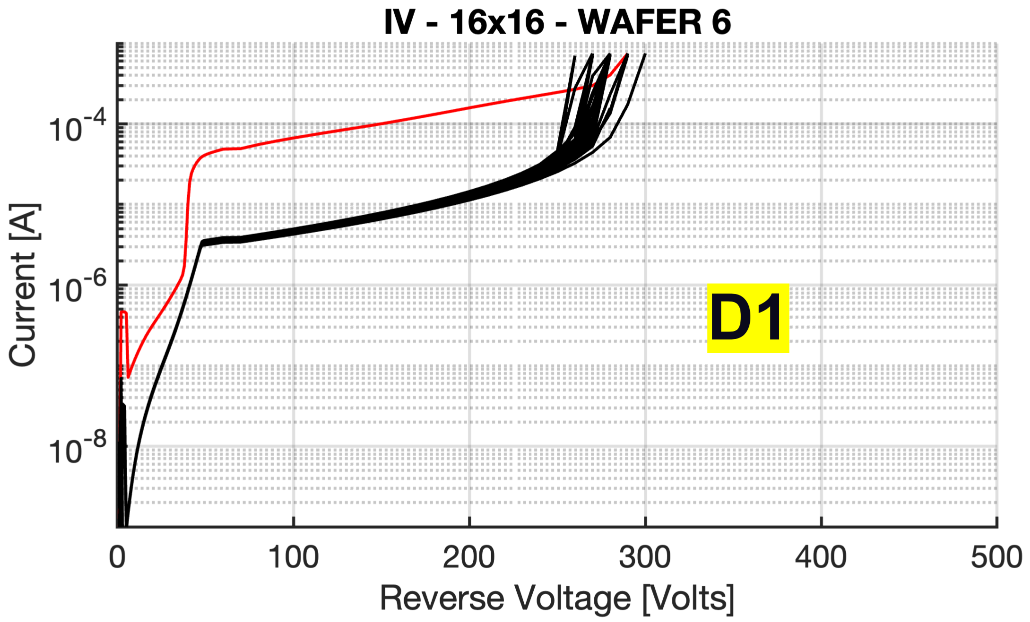


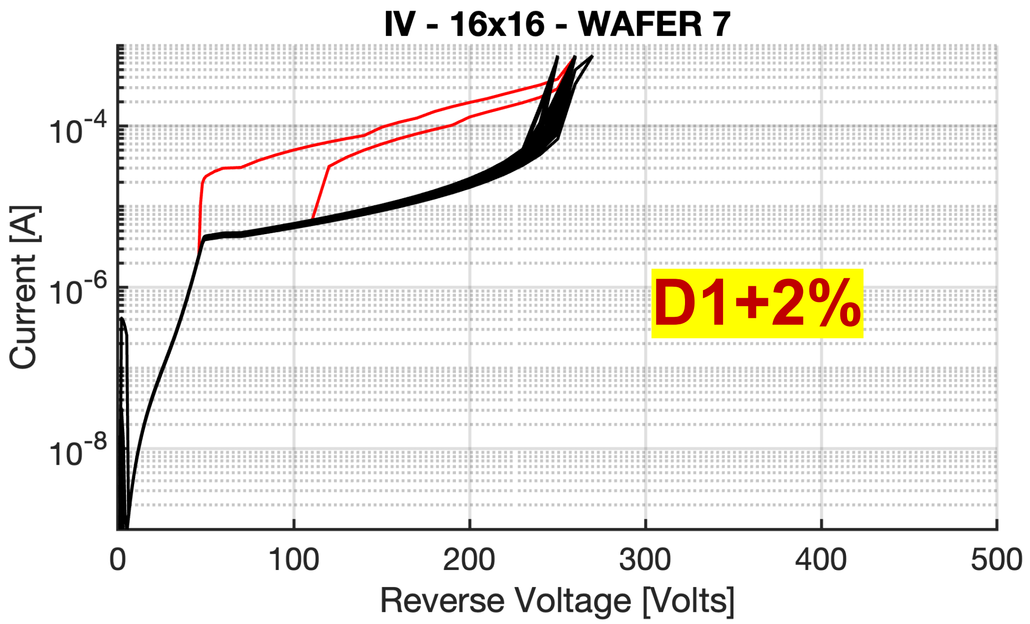
16x16 Sensors Characterization: DARK IV (DEEP Split)

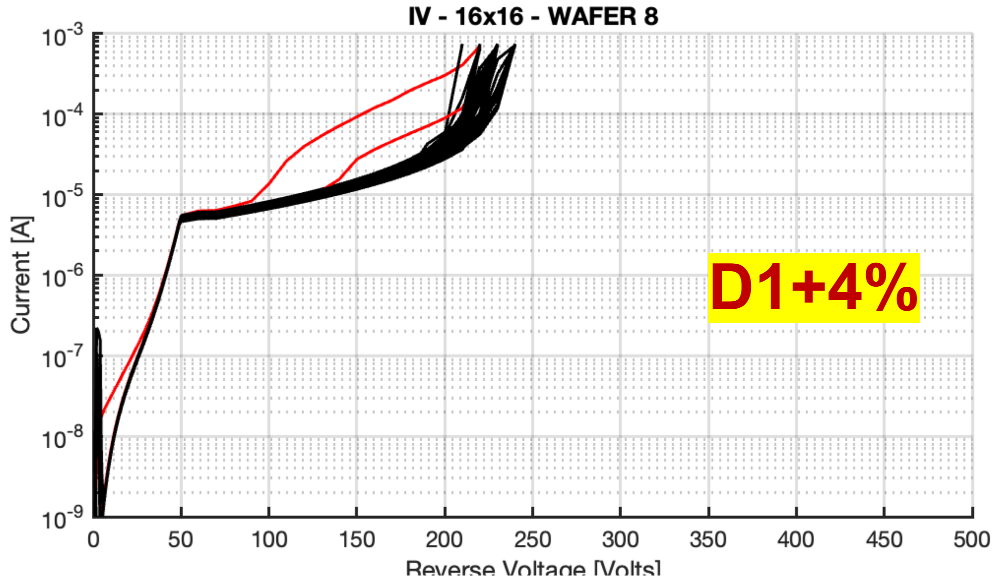




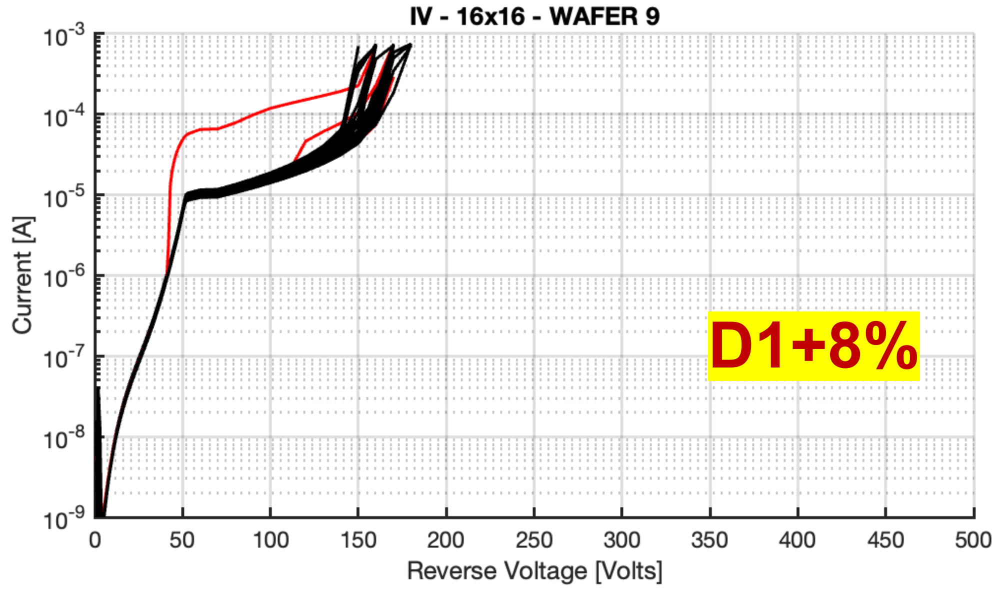








Increasing dose

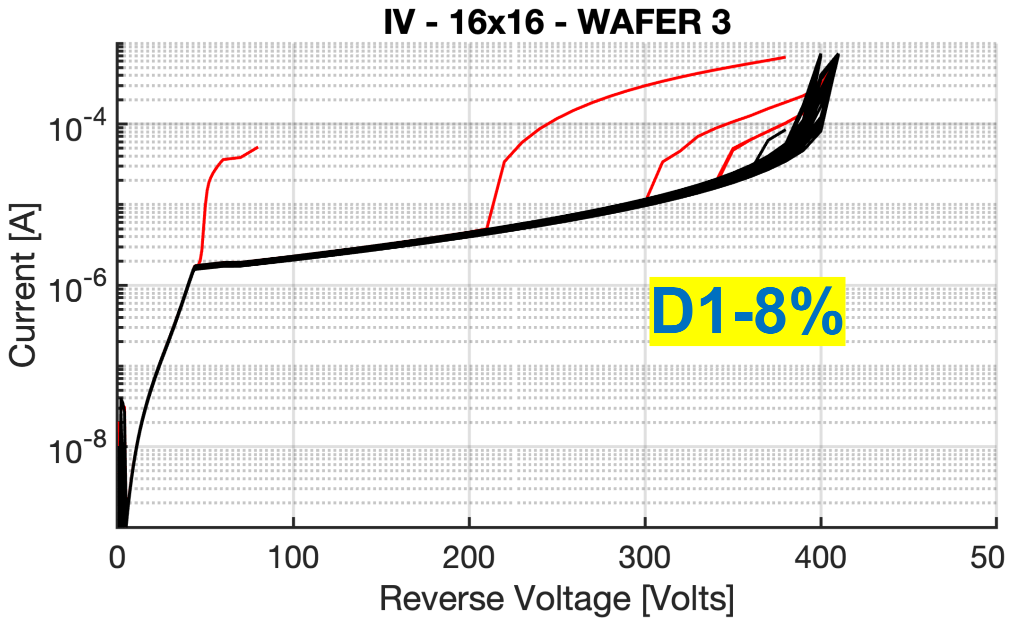


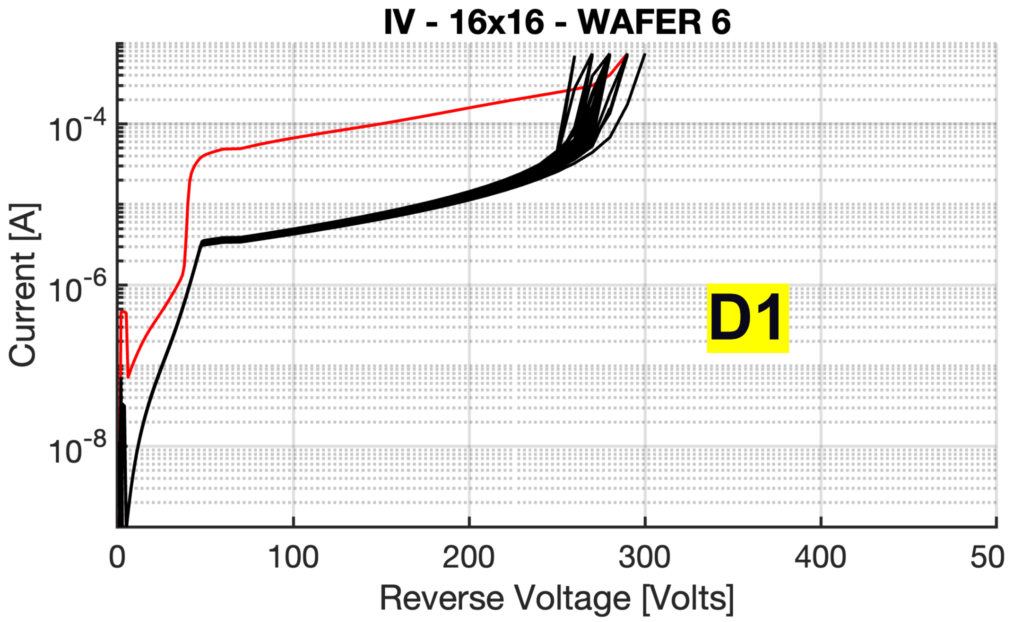
Reds = Bads due to premature BD or high current

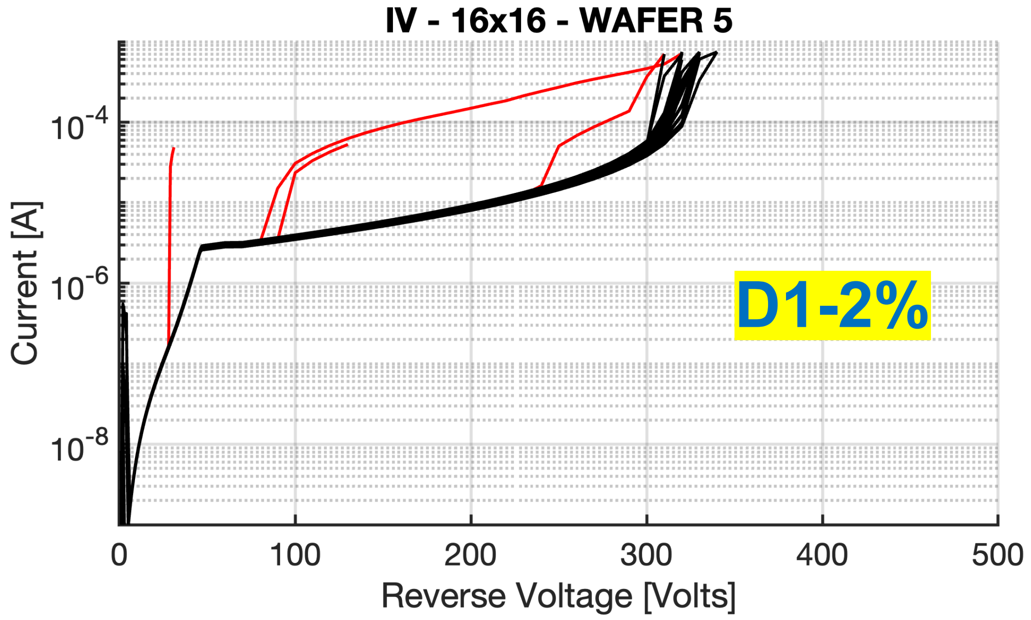
Wafer Level Characterization: DARK IV (DEEP Split)

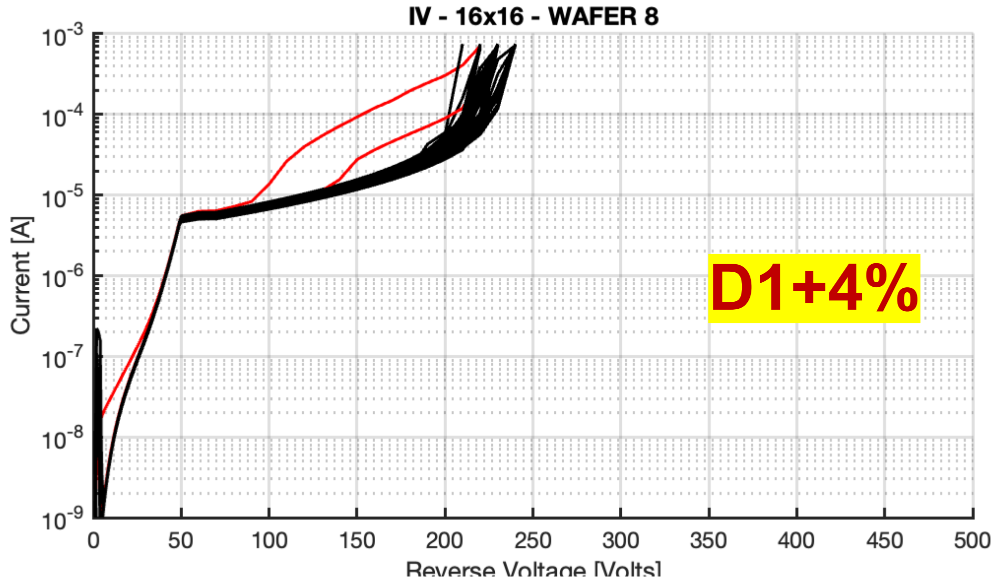
YIELD

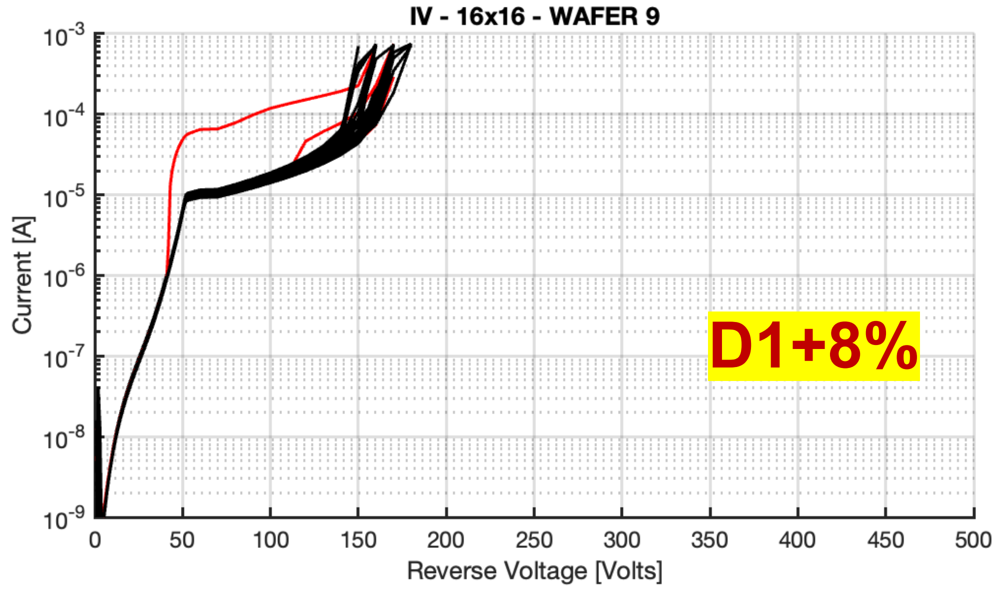
Wafer #	GOODS	BADS	YIELD
1	36	8	81.8%
2	41	3	93.2%
3	39	5	88.6%
4	43	1	97.7%
5	40	4	90.9%
6	43	1	97.7%
7	41	3	93.2%
8	42	2	95.5%
9	42	2	95.5%











Conclusion

- **FBK started a Technology Transfer of the custom FBK-LGAD Technology** to an external CMOS Foundry to investigate the reliability of the fabrication process for possible future large volume-productions

- The First Batch was completed in May ‘24. Wafer-level characterization showed promising results in terms of Yiled, V_{BD}, Dark current, Gain and Wafer-level uniformity

- Some aspects still to be optimized: high GR current (supposed to be due to epi-type inversion); high V_{BD} spread in the Shallow PGAIN Split

- Further characterization is ongoing by INFN and University of Turin (test beam, irradiation tests)

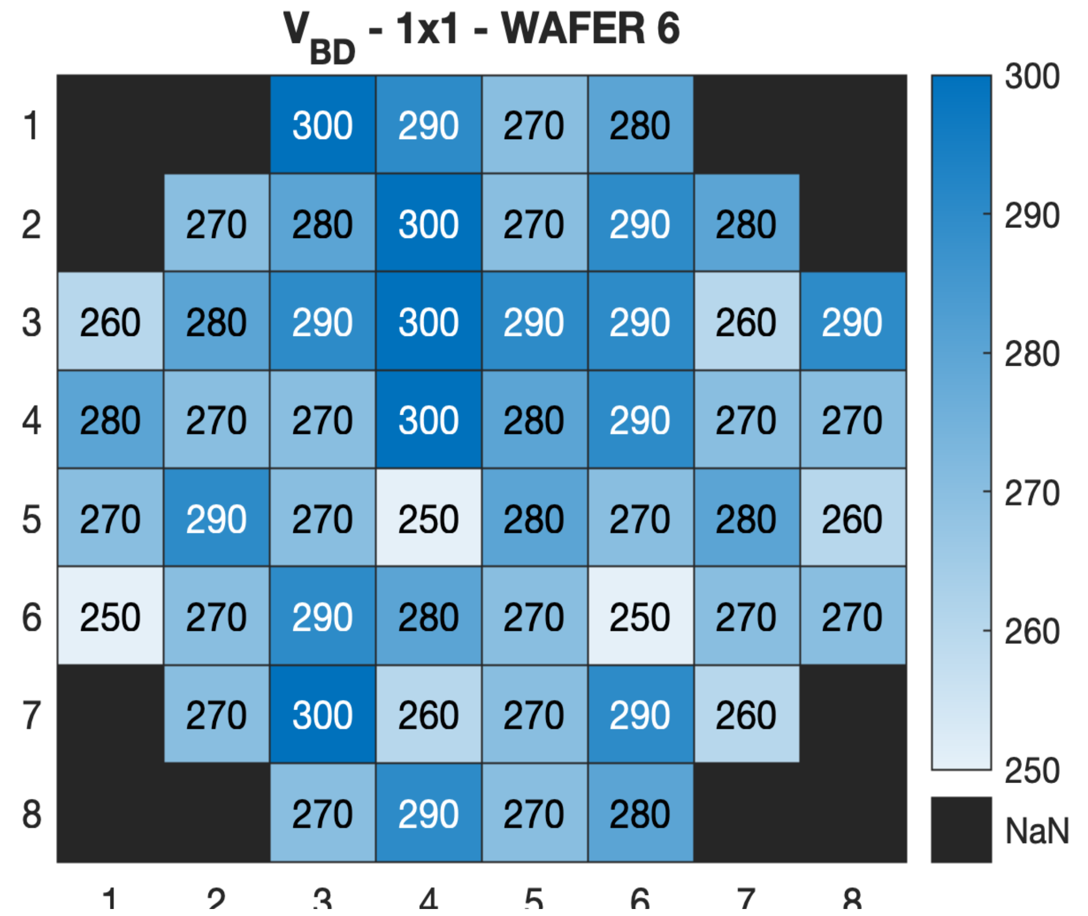
- The next batch is planned for Sept 2024

THANKS!

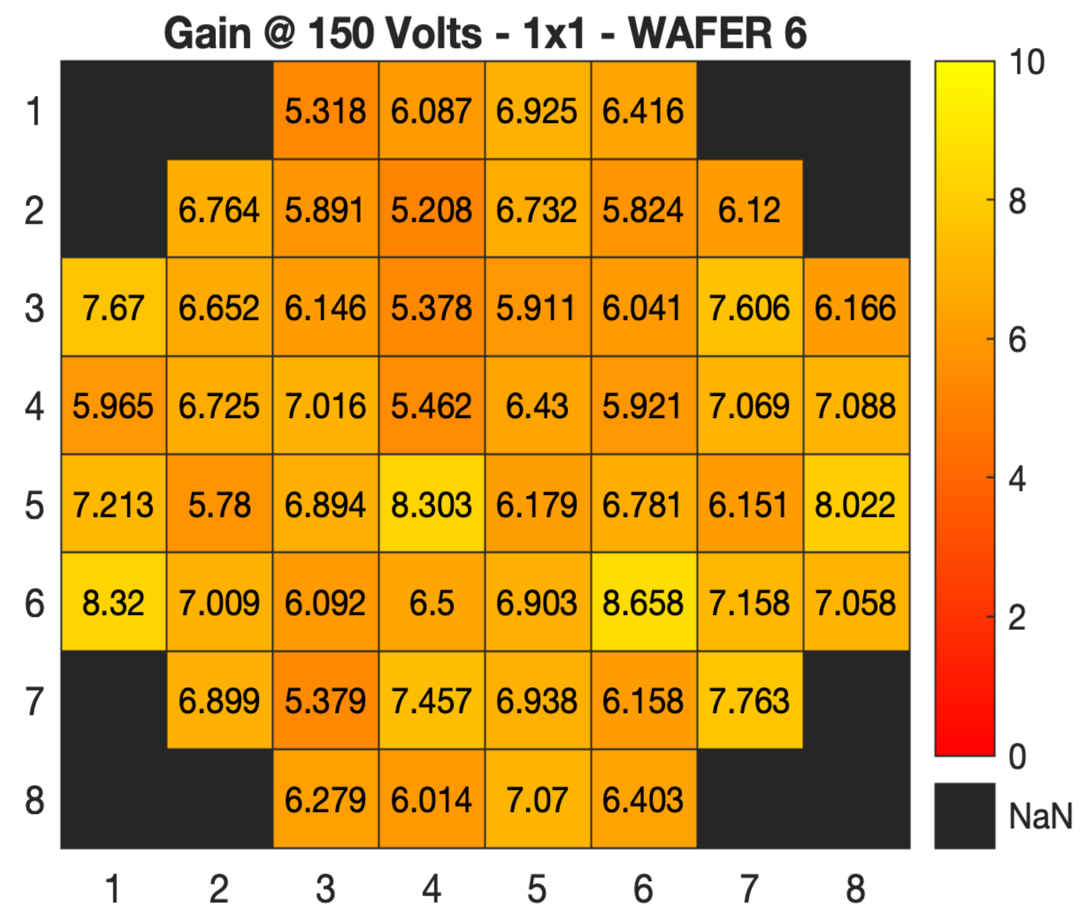
Special acknowledgement to:
INFN and University of Turin
University of Piemonte Orientale
University of Perugia
University of Trento

And to the LFoundry Team

PAD Characterization: **BD and GAIN (DEEP Split)**

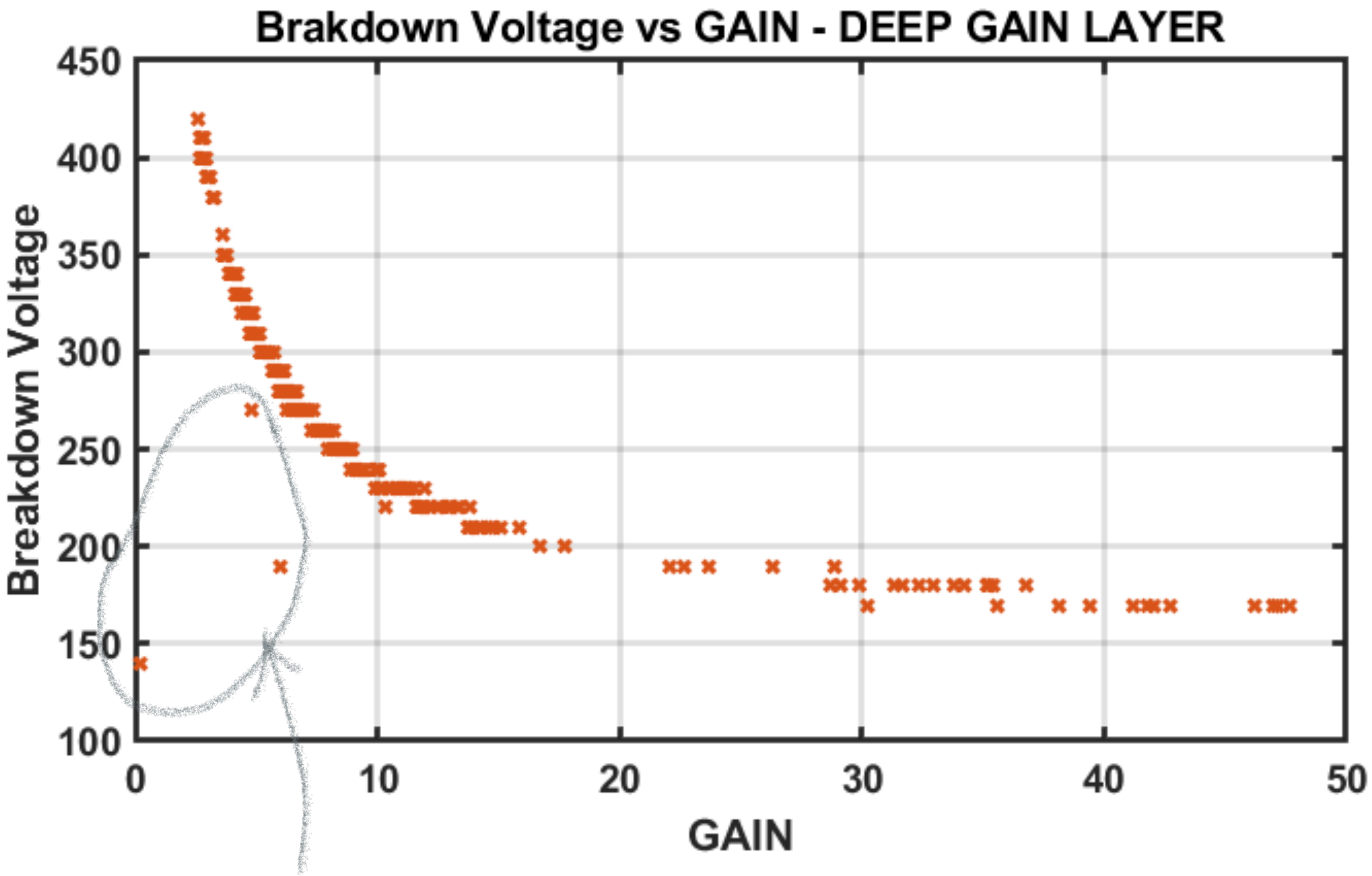

V_{BD} - 1x1 - WAFER 6

	1	2	3	4	5	6	7	8
1			300	290	270	280		
2		270	280	300	270	290	280	
3	260	280	290	300	290	290	260	290
4	280	270	270	300	280	290	270	270
5	270	290	270	250	280	270	280	260
6	250	270	290	280	270	250	270	270
7		270	300	260	270	290	260	
8			270	290	270	280		


Gain @ 150 Volts - 1x1 - WAFER 6

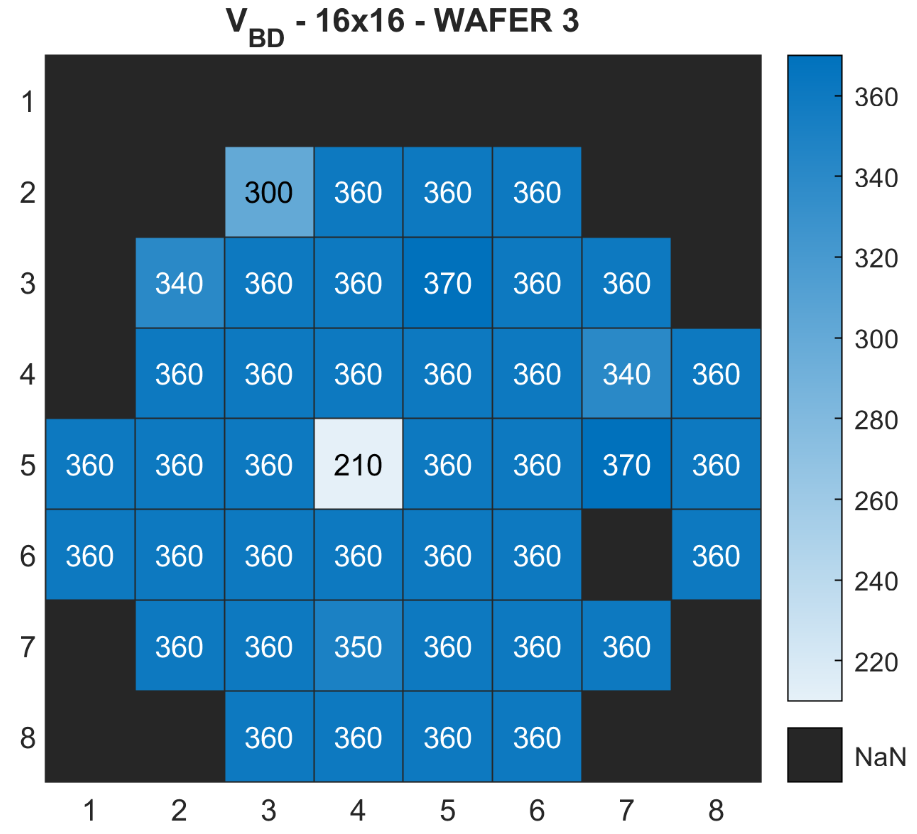
	1	2	3	4	5	6	7	8
1			5.318	6.087	6.925	6.416		
2		6.764	5.891	5.208	6.732	5.824	6.12	
3	7.67	6.652	6.146	5.378	5.911	6.041	7.606	6.166
4	5.965	6.725	7.016	5.462	6.43	5.921	7.069	7.088
5	7.213	5.78	6.894	8.303	6.179	6.781	6.151	8.022
6	8.32	7.009	6.092	6.5	6.903	8.658	7.158	7.058
7		6.899	5.379	7.457	6.938	6.158	7.763	
8			6.279	6.014	7.07	6.403		

Scatter plot VBD vs Gain at 150 V for all the 9 wafers of the DEEP split (with different PGain Doses)

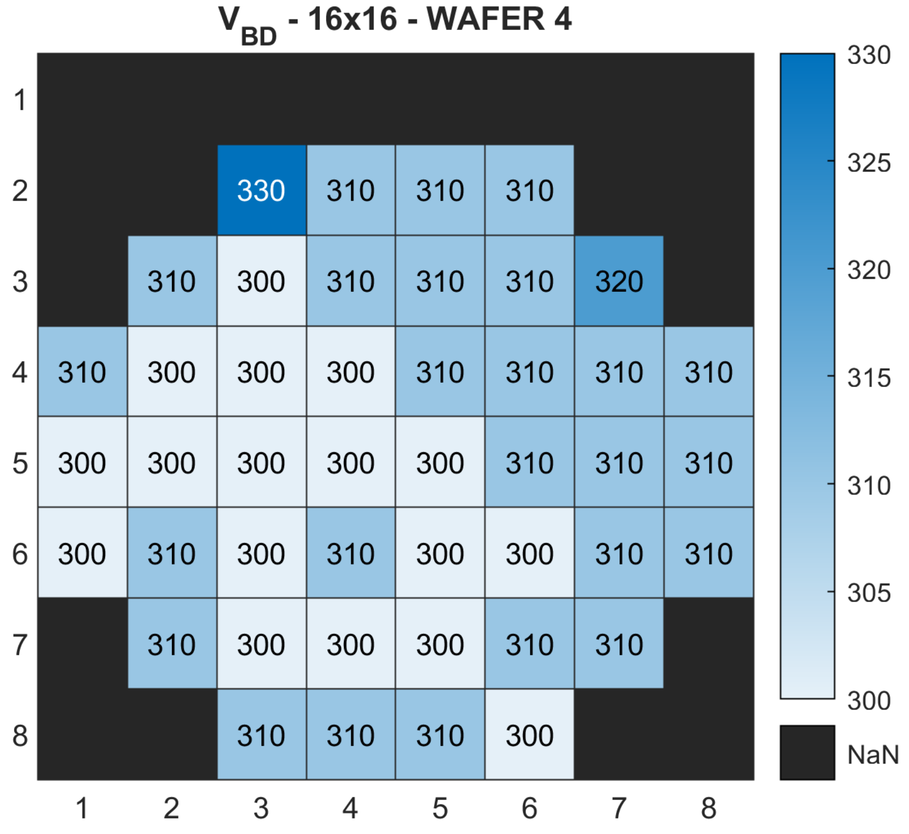


Only 3 out 486 samples show a premature breakdown (not due to gain)

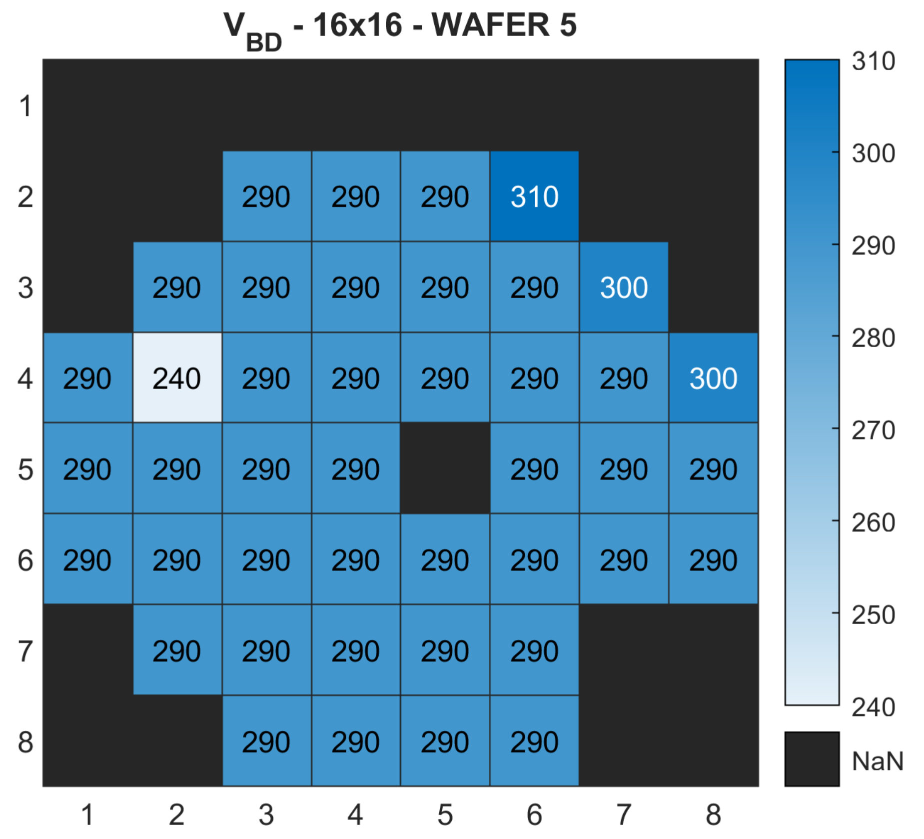
16x16 LGAD Characterization: V_{BD} MAPS (DEEP SPLIT)


V_{BD} - 16x16 - WAFER 3

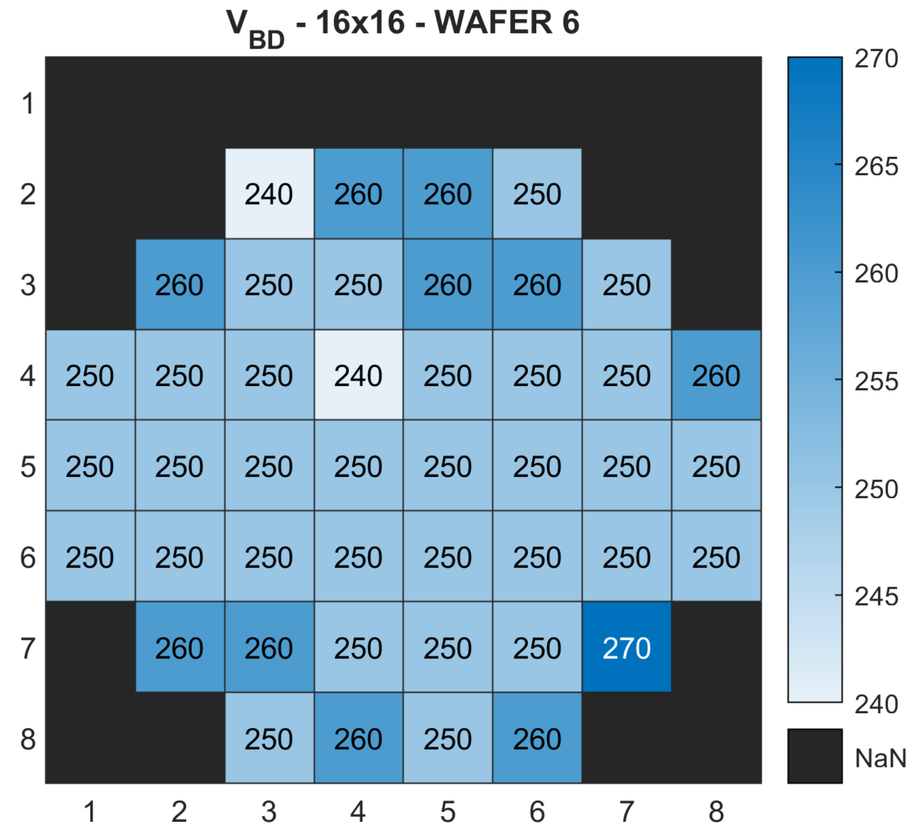
	1	2	3	4	5	6	7	8
1								
2			300	360	360	360		
3		340	360	360	370	360	360	
4		360	360	360	360	360	340	360
5	360	360	360	210	360	360	370	360
6	360	360	360	360	360	360		360
7		360	360	350	360	360	360	
8			360	360	360	360		


V_{BD} - 16x16 - WAFER 4

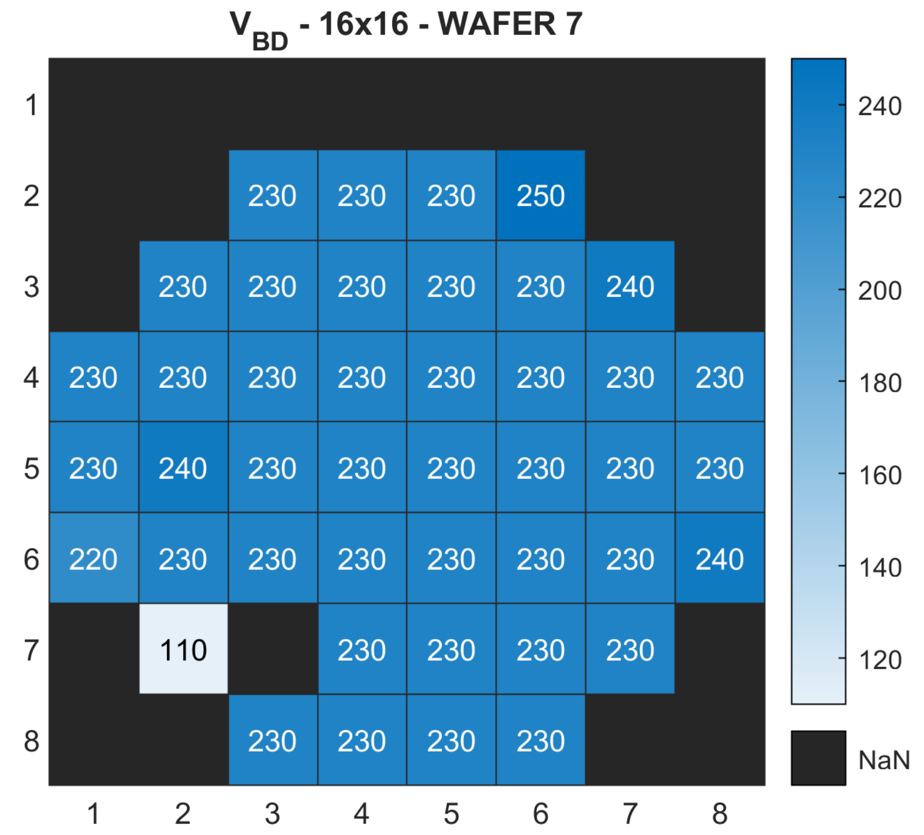
	1	2	3	4	5	6	7	8
1								
2			330	310	310	310		
3		310	300	310	310	310	320	
4	310	300	300	300	310	310	310	310
5	300	300	300	300	300	310	310	310
6	300	310	300	310	300	300	310	310
7		310	300	300	300	310	310	
8			310	310	310	300		


V_{BD} - 16x16 - WAFER 5

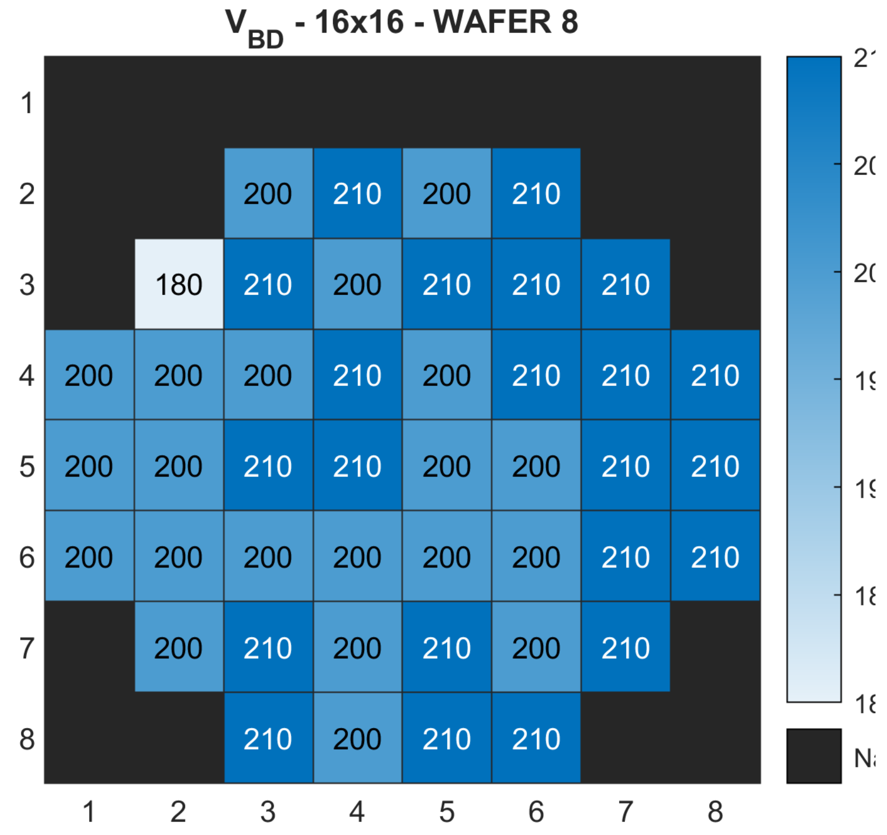
	1	2	3	4	5	6	7	8
1								
2			290	290	290	310		
3		290	290	290	290	290	300	
4	290	240	290	290	290	290	290	300
5	290	290	290	290		290	290	290
6	290	290	290	290	290	290	290	290
7		290	290	290	290	290		
8			290	290	290	290		


V_{BD} - 16x16 - WAFER 6

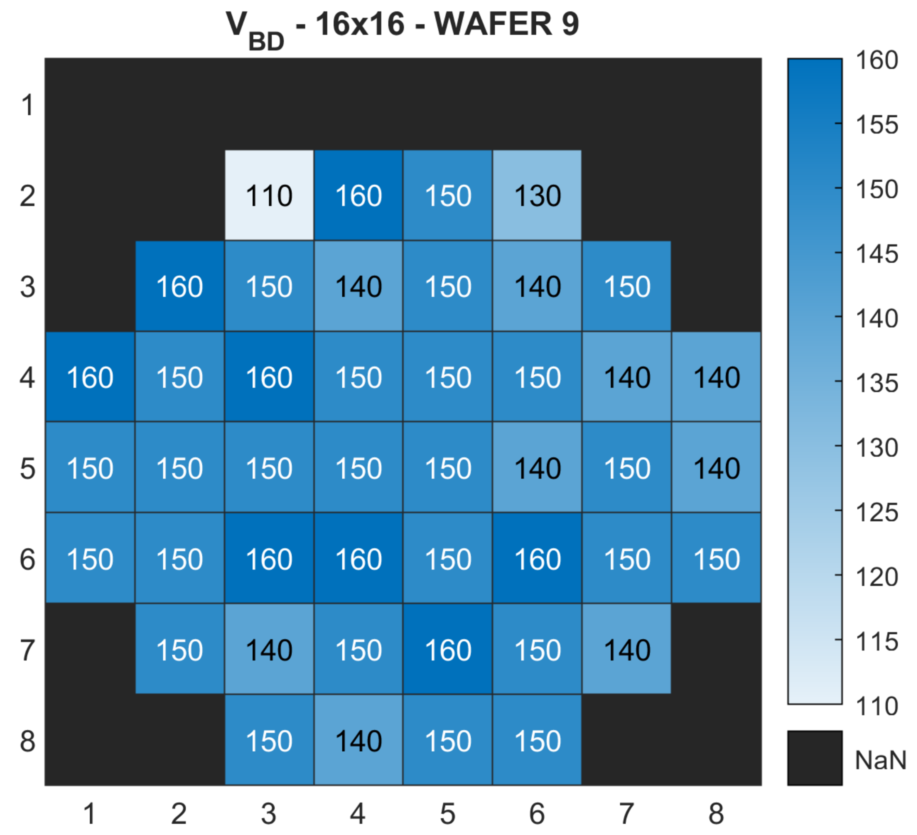
	1	2	3	4	5	6	7	8
1								
2			240	260	260	250		
3		260	250	250	260	260	250	
4	250	250	250	240	250	250	250	260
5	250	250	250	250	250	250	250	250
6	250	250	250	250	250	250	250	250
7		260	260	250	250	250	270	
8			250	260	250	260		


V_{BD} - 16x16 - WAFER 7

	1	2	3	4	5	6	7	8
1								
2			230	230	230	250		
3		230	230	230	230	230	240	
4	230	230	230	230	230	230	230	230
5	230	240	230	230	230	230	230	230
6	220	230	230	230	230	230	230	240
7		110		230	230	230	230	
8			230	230	230	230		


V_{BD} - 16x16 - WAFER 8

	1	2	3	4	5	6	7	8
1								
2			200	210	200	210		
3		180	210	200	210	210	210	
4	200	200	200	210	200	210	210	210
5	200	200	210	210	200	200	210	210
6	200	200	200	200	200	200	210	210
7		200	210	200	210	200	210	
8			210	200	210	210		


V_{BD} - 16x16 - WAFER 9

	1	2	3	4	5	6	7	8
1								
2			110	160	150	130		
3		160	150	140	150	140	150	
4	160	150	160	150	150	150	140	140
5	150	150	150	150	150	140	150	140
6	150	150	160	160	150	160	150	150
7		150	140	150	160	150	140	
8			150	140	150	150		