MAX PLANCK SEMICONDUCTOR LABORATORY

MARTHA - Monolithic Array of Reach Through Avalanche photo Diodes

developed at

Max Planck Semiconductor Laboratory

(in German Halbleiterlabor der Max Planck Gesellschaft – MPG HLL)

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MPS Semiconductor Laboratory (in German: MPG Halbleiterlabor - HLL)

Till end 2023 @ Siemens Campus Neuperlach Munich

- 1000m^2 of clean room area
- 330m^2 of ISO3 area
- Full 6 inch silicon process line

From 2024 @ IPP Campus Garching

- 1500m^2 of clean room area
- 600m^2 of ISO3 & ISO4 area
- 8 inch silicon process line

From 2024 HLL is part of Munich Quantum Valley

Central facility of the Max Planck Society
with 40 employees: scientists, engineers and technicians + guest scientists, engineers and students

MPG HLL is the lab specialized on development of fully depleted silicon radiation sensors with integrated electronics optimized for different scientific projects

Inside HLL – Sensors and Systems : Design, fabrication & Test

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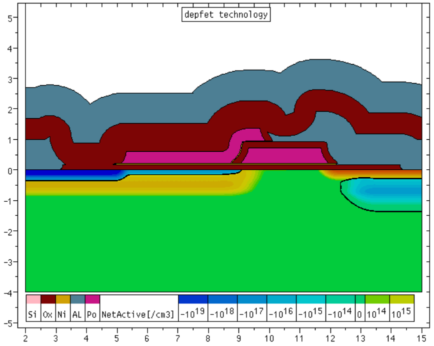
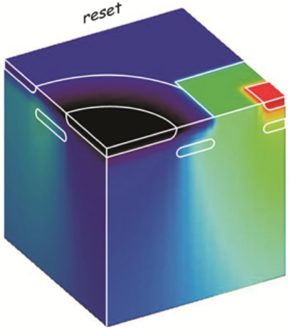
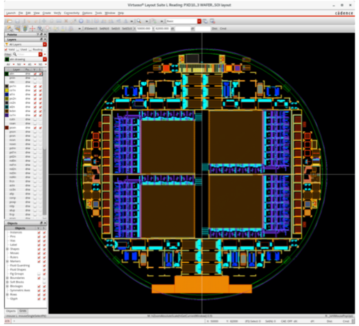
Process simulation



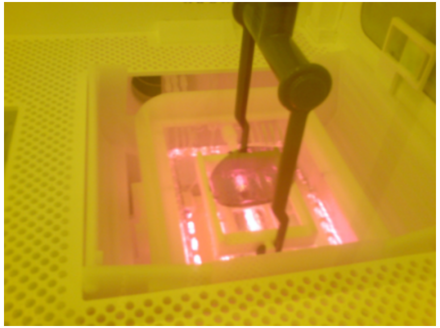
Device simulation, 2D and 3D



State-of-the-art layout tools



In house fabrication



Wire bonding, hybrid assembly

@ HLL:

- sensor design and fabrication
- interconnection
- system/camera design and test

System test facilities

Highlights from the past

- **NA11 - NA32 experiments at CERN (1982 -1988)   [MPP]**
  First usage of silicon strip detectors in the high energy physics

- **XMM Newton (launch 1999) [MPE]**
  Large area device with 100% fill factor, and very sensitive entrance window

- **ATLAS (2004) [MPP]**
  development at HLL, fabrication at industry, 3.000 wafers produced

- **LAMP (2011 – 2014) [CFEL]**
  Photon sicence: Large area device with ultra sensitive entrance windows

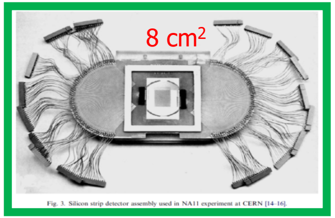
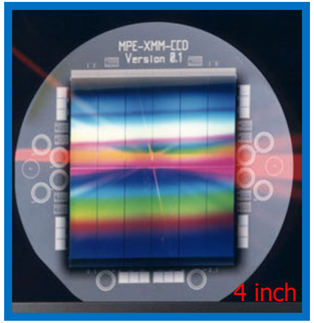
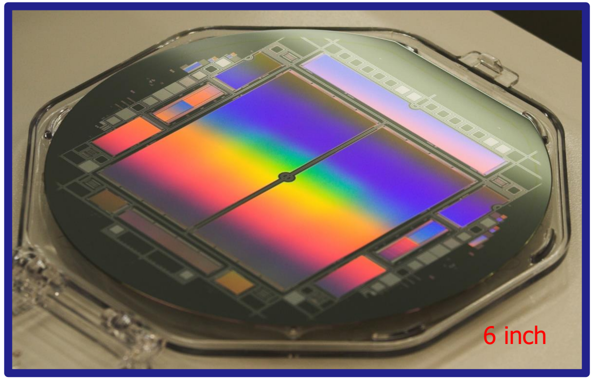


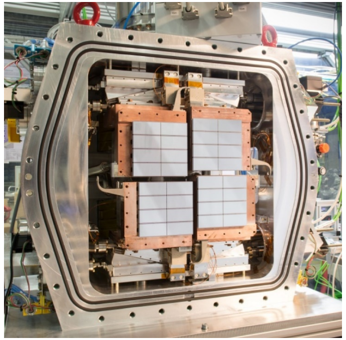
Fig. 3. Silicon strip detector assembly used in NA11 experiment at CERN [14-16].





Recent development highlights

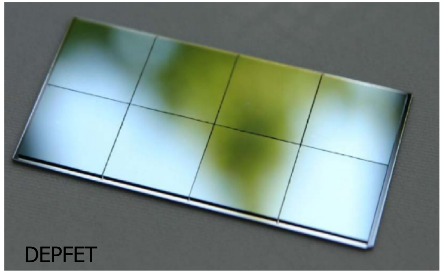
Mini SDD - DSSC @ EuXFEL
(imaging of X-ray diffraction patterns)



M. Porro et al., *The MiniSDD-based 1-Megapixel Camera of the DSSC Project for the European XFEL*, IEEE TNS 68(6), pp. 1334 - 1350, June 2021

camera	**1024 x 1024 pixels** 21 x 21 cm² 32 sensor chips 4 quadrants central hole for direct beam
sensor	mini-SDD cells 128 x 256 pixels 3.0 x 6.2 cm² (chip)
hex. pixel pitch	204 μm × 236 μm
energy range	**0.25 keV – 6 keV**
noise	60 el. r.m.s.
peak frame rate	**4.5 MHz**
frame storage	800 frames

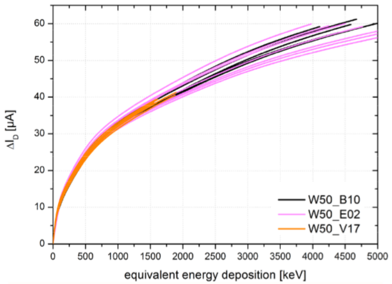
DSSC @ EuXFEL
DEPFET **S**ensor with **S**ignal **C**ompression
(imaging of X-ray diffraction patterns)



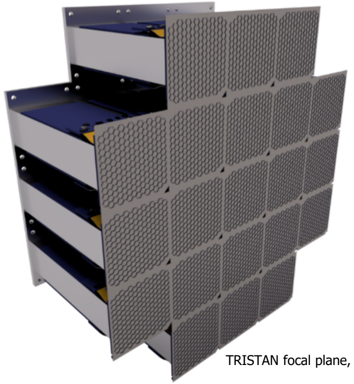
Sensor	**2.56 x 10.24 cm²** 512 × 128 pixels

Hybrid detector
with 8 readout ASICs (64x64)

Pixel size:	204 x 236 μm²
Frame time:	**220ns (4.5MHz)**



TRISTAN (tritium sterile anti-neutrino) @ KIT
sterile neutrino search by electron spectroscopy



TRISTAN focal plane, 21 modules.

system	21 sensors **20 cm diameter**
sensor	SDD with integrated FET **166 cells (~ 14 x 12 array)** **3.8 x 4.0 cm² (chip)**
SDD cell	hexagonal, 3 mm side length 7 mm² area
energy resolution	< 300 eV FWHM @ 20 keV
count rate	≤ 10^8/sec on focal plane ≤ 10^5/sec on sensor cell
dead layer	**as thin as possible**

Recent DEPFET development highlights

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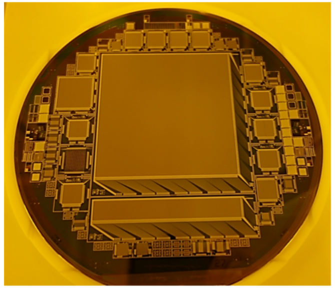
ATHENA Wide Field Imager

the **A**dvanced **T**elescope for **H**igh-**En**ergy **A**strophysics as ESA's next-generation X-ray astronomy observatory

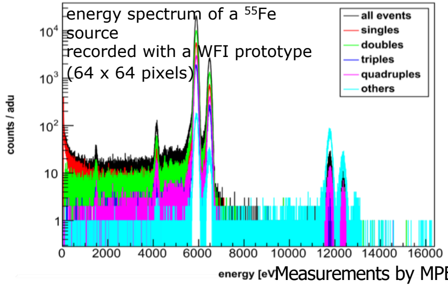


Sensor: 512 x 512 pixels
78.00 x 76.15 mm²

rolling shutter mode

Pixel size: 130x 130 μm^2

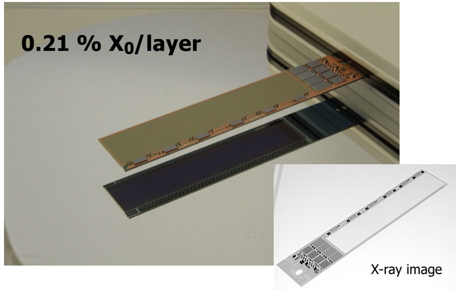
Frame time: **1.28 msec, i.e. 2.5 μsec / row**
with 128 eV (singles) & 136 eV (all)



Measurements by MPE

BELLE II pixel detector

High energy particle vertexing

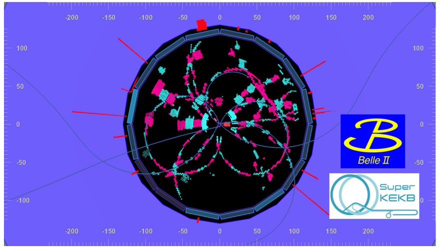


Active area 12.5 x 44.8(61.44)mm^2
250 x 800 pixels
Thickness: **75 μm**

rolling shutter mode

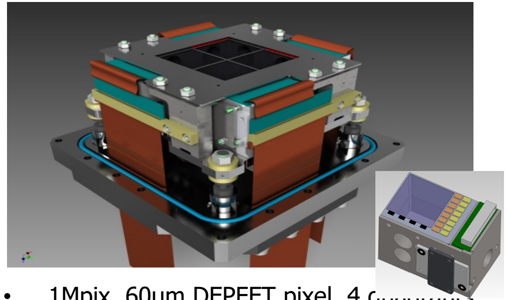
Pixel size: 50 x 55(85) μm^2

Frame time: 20ms (50kHz) (10MHz -row)

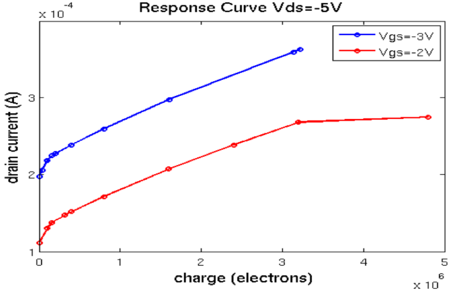


EDET80k Detector

Ultrafast TEM camera



- 1Mpix, 60μm DEPFET pixel, 4 quadrants, 6x6 cm² sensitive
- 1-3 M electrons to store into internal gate
- 30-50μm thin sensitive area
- Bidirectional 4-fold read out, frame rate: 80kHz
- memory to store ~100 frames



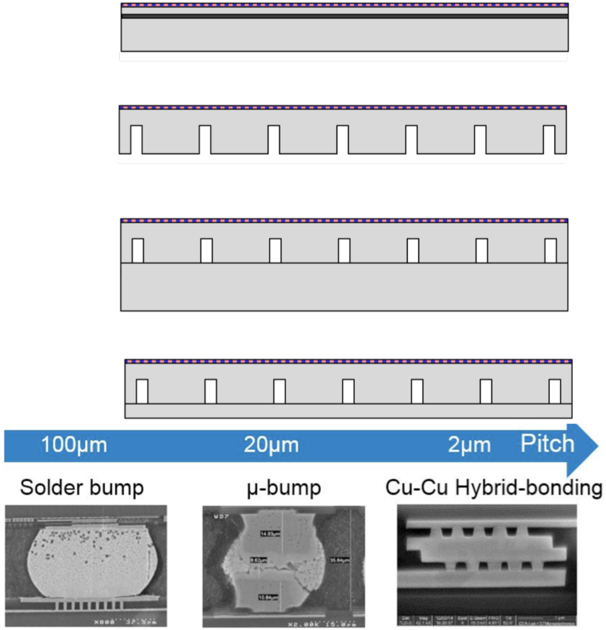
New building new technology Extension - MQV … but not only MQV …

Goal

- Install post-processing capabilities of (externally) produced wafers
  - CMOS or PICs wafers or …
- Heterogenous integration (2.5 D, 3 D)
- Development of superconducting qubits

Key process modules to be installed and qualified at HLL

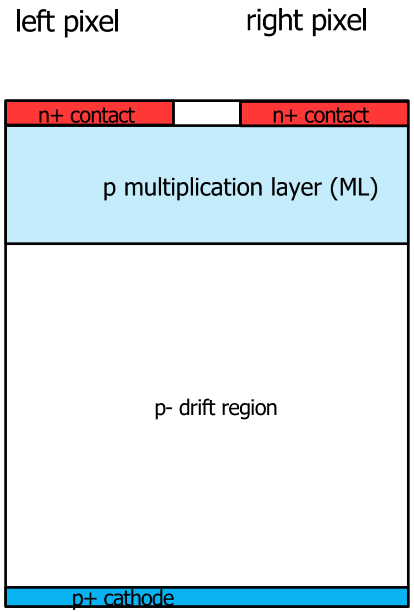
- Deep reactive ion etching (ICP-DRIE, "Bosch" Process)
  - TSVs, micro-channels
- CMP tool for planarization and prep. for wafer bonding
  - Surface quality crucial for hybrid bonding
- Wafer Bonding
  - direct Si-Si Bonds and hybrid bonding with embedded metal-metal interconnect
  - Back-end-of-line compatible low-temperature annealing
- Ebeam writing to enable nano patterning
- Indium bumping
- …



Imed Jani. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes, 2019

Martha - **M**onolytic **A**rray of **R**each **T**hrough **AP**Ds

Initial motivation – develop low gain avalanche device with high fill factor for photon science applications

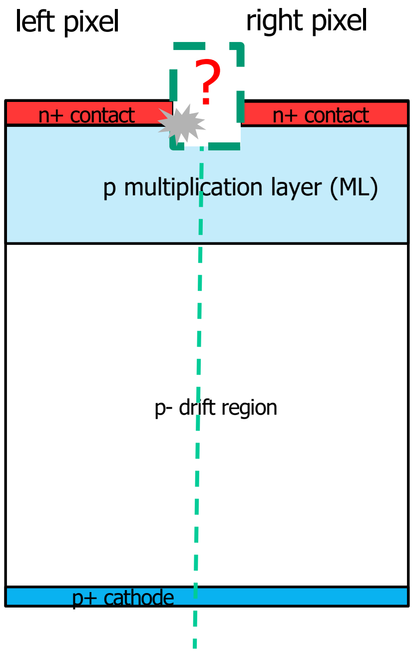


(Soft X-ray) Photon Counting

For applications at FELs

- (HLL) thin entrance window + avalanche multiplication
- homogeneous gain
- high k-factor (low excess noise)

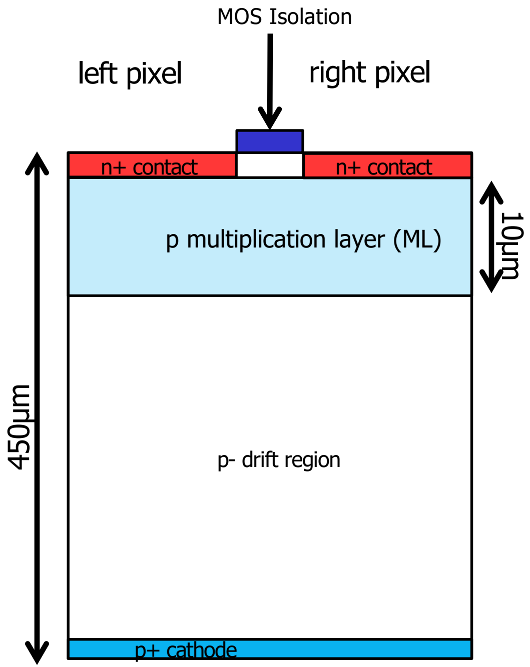
Martha - Interpixel isolation



Interpixel isolation requirements

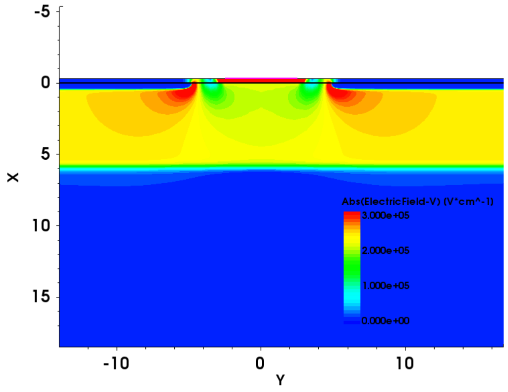
- Isolation
- Suppress edge break down
- Reduction of E-fields at interface
  (oxide charge up, H-bond cracking)

Strip array 50μm pitch (2D simulation)



HF region extends over pixel gaps

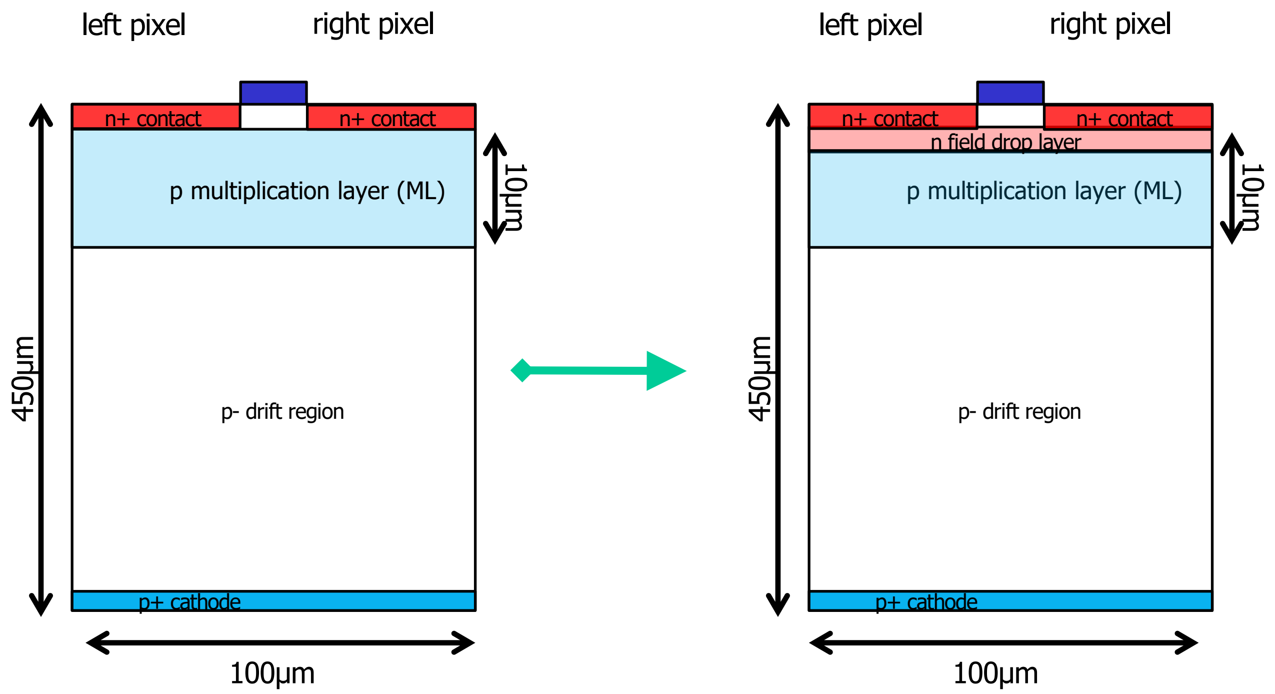
- Reach-through APD
- 50 μm pitch
- MOS isolation
- Based on HLL „standard" technology



Avalanche (breakdown) at edges

Approach not usable

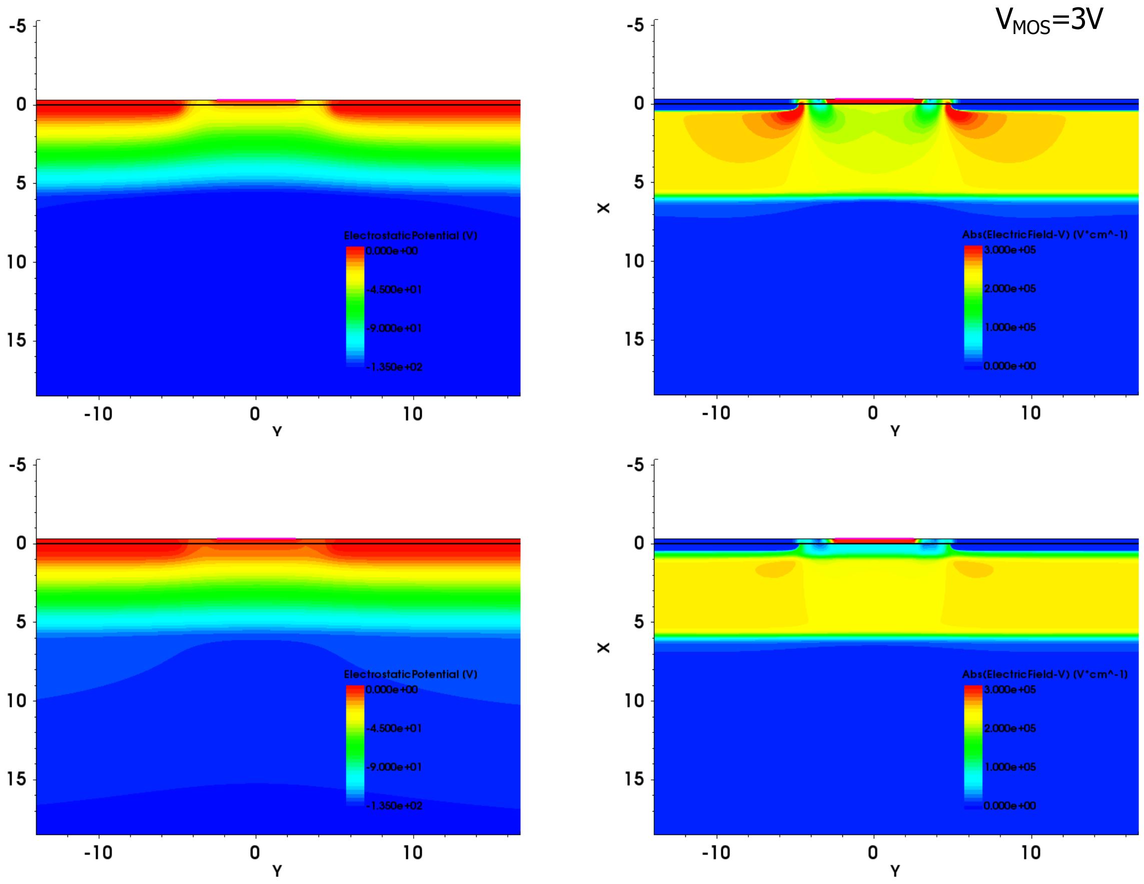
2D Simulation Edge Breakdown Suppression



2D Simulation Edge Breakdown Suppression

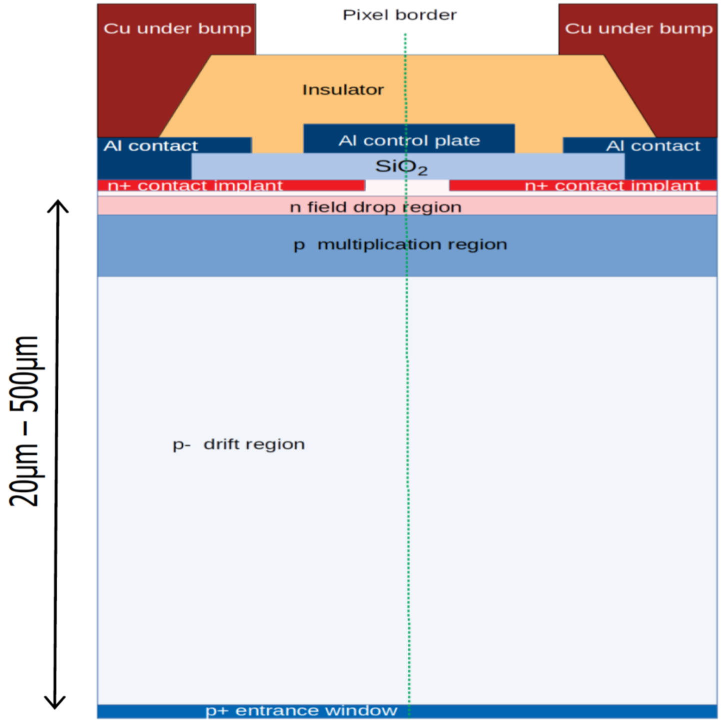
HF region extends over pixel gaps

HF region and field drop layer extend over pixel gaps



MARTHA - **M**onolytic **A**rray of **R**each **T**hrough **A**PDs

Low gain avalanche device with high fill factor for photon science applications



Expected features:

Gain up to 20

Collection efficiencies: > 99%

Pixel pitch: given by bump bond technology and read out electronics space consumption (ATLAS 50µm)

Position resolution: $\ll \frac{pitch}{\sqrt{12}}$ ($\ll 10\mu$m)

Time resolution:

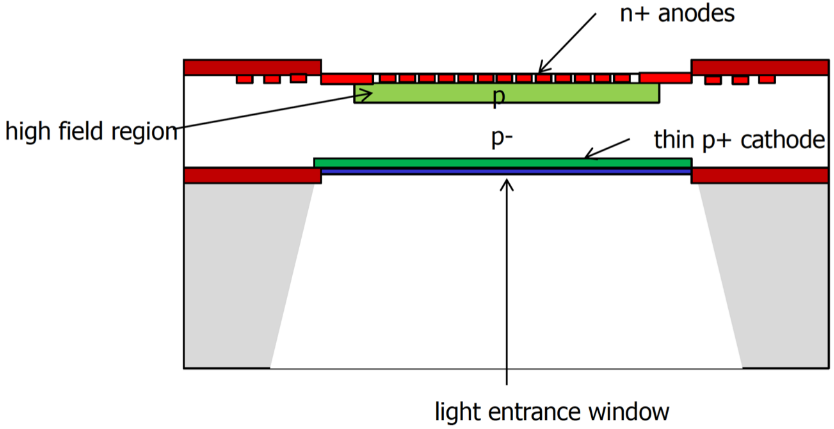
Application dependent

- Leading edge trigger: <50ps
- Full signal formation 50ns (for thickness 500µm)

Simulation results paper in review process

MARTHA - **M**onolytic **A**rray of **R**each **T**hrough **A**PDs

Faster device for particle tracking ? → Thinned Reach Through APD based on HLL SOI Technology



$t_{APD} \gtrsim 20\mu m$

$t\_handle\_wafer \approx 400\mu m$

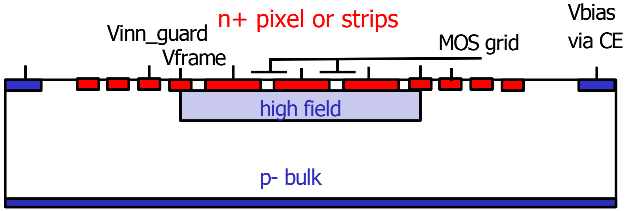
t_{APD} = 20µm: drift times (triggering electrons + amplified holes) ≈ 0.5ns

Full signal formation 0.5ns (50ns for thickness 500µm)

Prototype production

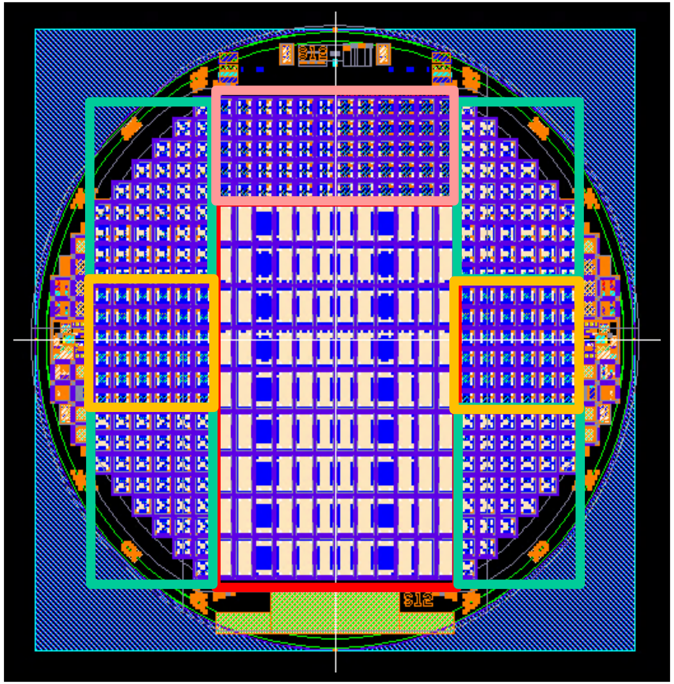
Aims

- proof of principle
- Efficiency, gain, cross talk, noise
- find reliable narrow guard ring structure (in view of buttable arrays)



backside p+ entrace window
non structured, no Al

Pixel Strips Diodes MGR Diodes



production finished in the old lab
tests started in the new lab

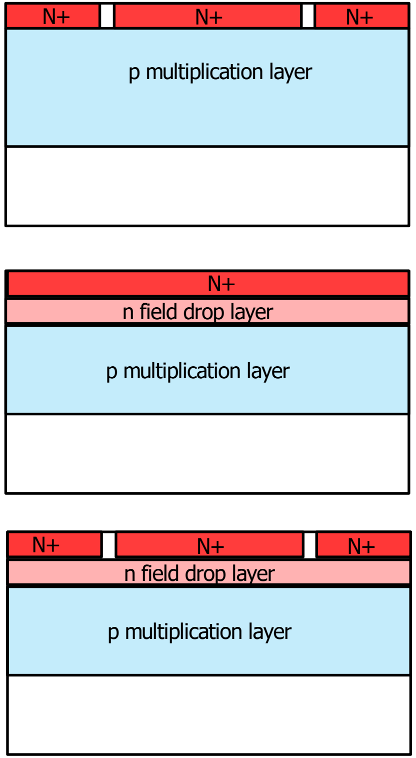
APD Diodes with and without Gaps

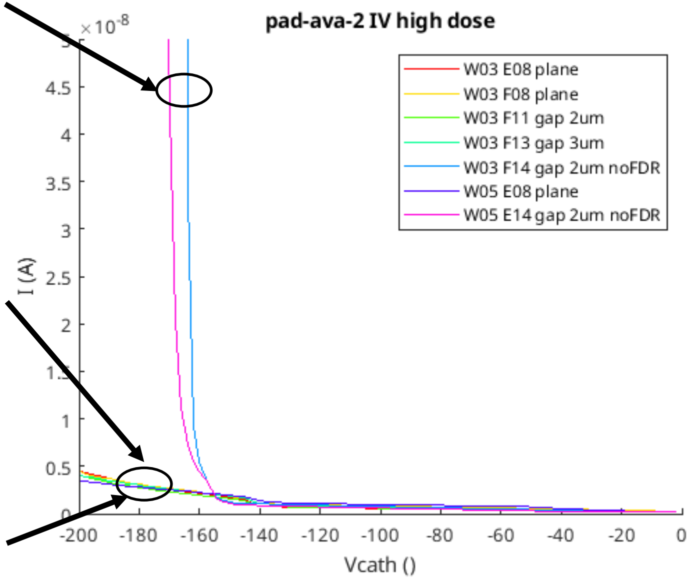
diodes 2x2mm²

diode with gaps but without FDL

plane diode

diode with gaps and FDL



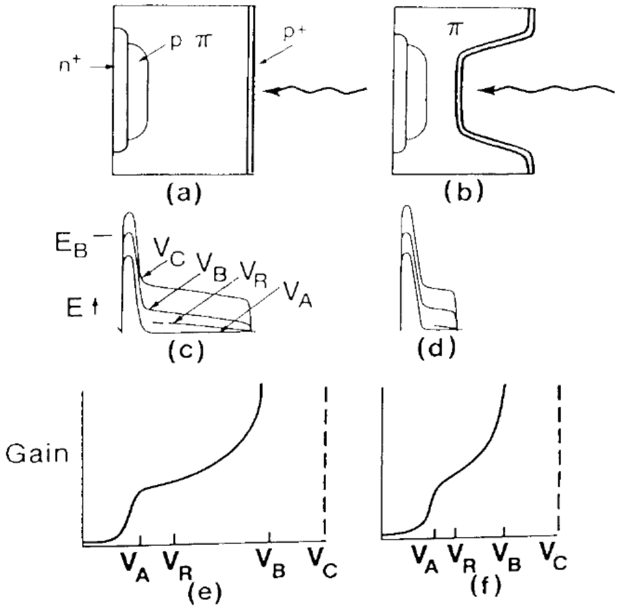


Edge breakdown suppression works as intended

Homogeneity of high energy implantation (multiplication region)

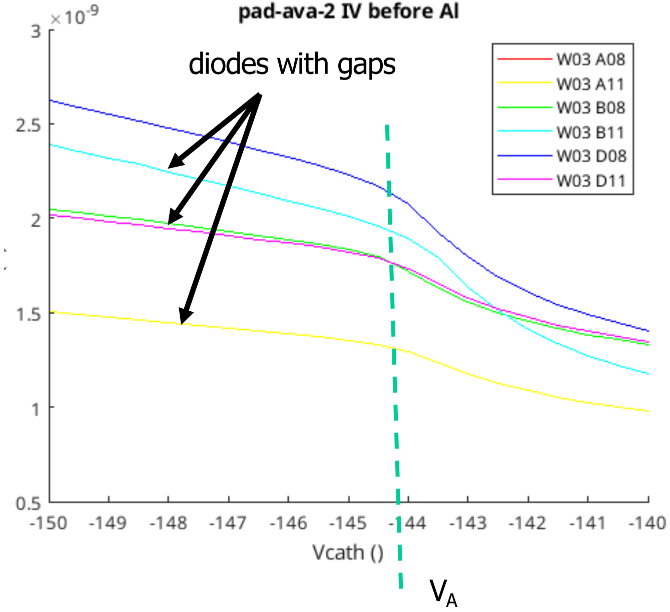
Typical Reach-Through APD IVs

R. J. McIntyre, 1985



point of inflection V_A

p multiplication region fully depleted



no difference between diodes and gap diodes (preliminary)

Summary

MARTHA – a new approach for LGADs

- operated in proportional mode
- no inter pixel dead space
- suitable for large pixel arrays
- low excess noise due to HE high field implantation
- First prototyping – small APD arrays and strips
- will be tested further soon
- Faster devices possible with thinner material

Expected features:

Gain up to 20

Collection efficiencies: > 99%

Pixel pitch: given by bump bond technology and read out electronics space consumption (ATLAS 50µm)

Position resolution: $<< \frac{pitch}{\sqrt{12}}$ ($<< 10\mu m$)

Time resolution:

Application dependent

Leading edge trigger: <50ps

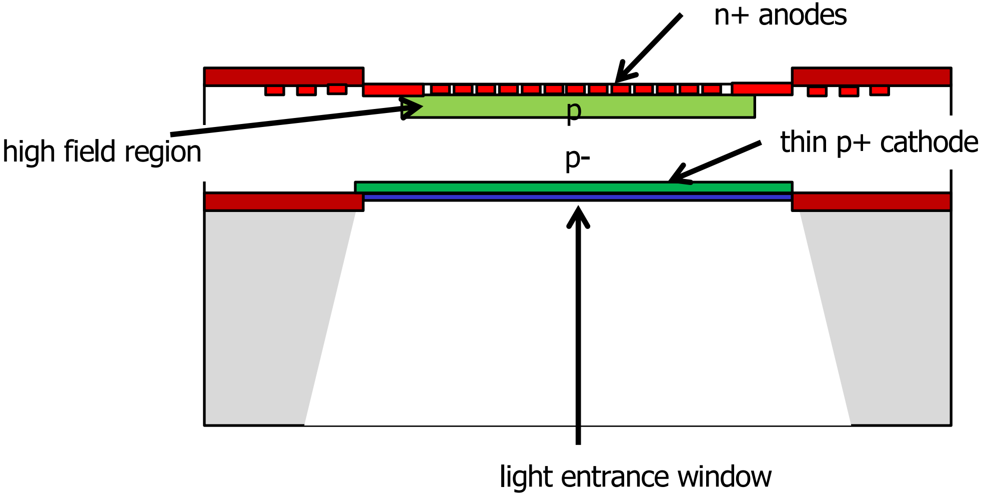
Full signal formation 50ns (for thickness 500µm)

0.5ns for 20 µm

Outlook

next steps:

- Proof of concept measurements (started)
- Discussions with potential users and ASIC designers
- Next production run in preparation for early/mid of next year as multi project wafer run – both thin and thick wafers planned
- Searching for collaboration partners for optimization and testing of thin MARTHA devices with improved timing capabilities



$t\_handle\_wafer \approx 400\mu m$

$t_{APD} \gtrsim 20\mu m$

Thank you for your attention …