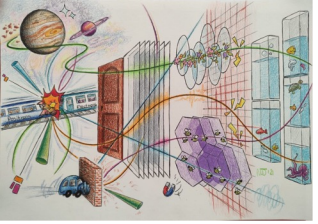
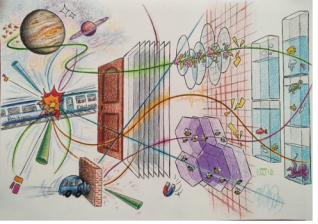


WG7 session - discussion on interconnects

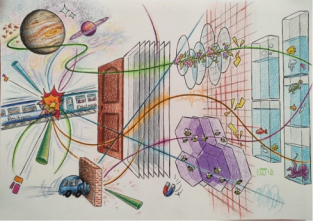
G. Calderini (LPNHE Paris), D. Dannheim (CERN), F. Huegging (Bonn)



Expressions of Interest

DRD3

Group	Contact	Ongoing work / topics of interest	Maskless	classical processes	2.5D integr. / modules	3D integration	FTE
ANL	Jessica Metcalfe	technologies for large-scale tracking devices	☐	☐	☐	☐	
Bonn University*	Fabian Hügging, Jochen Dingfelder	fine-pitch (<50 um) bonding; W2W bonding; in-house hybridisation	☑	☑	☐	☑	1 Staff + 1 Stud./Postdoc/Techn.
CERN*	Dominik Dannheim	In-house plating and hybridisation; compact module studies (including silicon photonics integration)	☑	☐	☑	☐	2.5 Res. + 2 Stud.
FBK	Giovanni Paternoster	3d-integration and interconnection of BSI-SiPMs for NUV/VUV; mask and mask-less UBM; W2W temporary bonding; chip-level solder-ball bonding >50 um; wafer-level micro bumps/pillars <50 um; in-house maskless interconnects	☑	☑	☑	☑	1 Staff
Fraunhofer IZM*	Thomas Fritzsch	hybridisation with <=25 um pitch; W2W bonding; wafer-level packaging; single-chip bump bonding for R&D	☐	☑	☐	☑	1 Staff
Geneva University*	Mateus Vicente	In-house flip-chip bonding: gold studs, ACP/ACF, Cu pillars; chip-to-flex	☑	☐	☑	☐	
IMB-CNM-CSIC	Miguel Ullán	RDL, TSV, interposers	☐	☑	☑	☐	0.5 Res.
INFN Bari	Giovanni Francesco Ciani	interconnection between bent sensors; stacking of several CMOS sensors for full 3d tracking	☐	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Cagliari	Adriano Lai	in-house single-die hybridisation with innovative bonding techniques such as ACF/ACP	☑	☐	☐	☐	
INFN Firenze	Giacomo Sguazzoni, Giovanni Passaleva	Novel interconnection techniques for future applications	☑	☐	☑	☐	0.5 Res. + 0.5 Stud.
INFN Milano	Gianluca Alimonti	Indium bump bonding; in-house die-to-die and die-to-PCB bonding; hybridisation of RSD; multi-chip systems on PCB/bus tape	☑	☑	☑	☐	
INFN Trieste	Giacomo Contin	interconnects for bent and ultrathin chips (ALICE ITS3); aerosol jet printing for RDL and contactless interconnects; TSV and wafer-to-wafer for 3D stacking	☐	☐	☐	☑	3 Res. + 1 Stud.
IPHC Strasbourg	Maciej Kachel	3D integration; small pitch (<10 um) interconnection	☐	☑	☐	☑	0.1 Staff
IP2I Lyon	Didier Contardo	wafer-to-wafer interconnect demonstrator	☐	☐	☐	☑	0.6 Physicist + 2.8 Tech
KIT Karlsruhe	Michele Caselle	in-house flip chip, gold studs, TSV processing, RDL	☑	☐	☑	☐	0.5 Staff + 1 Stud.
LPNHE Paris	Giovanni Calderini	interconnects: ACF, ACP, gold studs; characterisation techniques and devices; reliability testing; new interconnection techniques / scalability	☑	☐	☐	☐	1.5 Res. + 1 Stud. + 1 Techn.
MPG Halbleiterlabor*	Ladislav Andricek, Jelena Ninkovic	direct wafer bonding; 3D/2.5D systems with micro-channel cooling; W2W/C2W bonding	☐	☑	☑	☑	1 Staff + 2 Stud./Postdoc/Techn.
NIKHEF	Martin Fransen	high-frequency ASIC to module integration (RDL, TSV), wire bonding	☐	☐	☑	☐	0.2 Staff
ORNL	Mathieu Benoit	in-house interconnect for hybridisation and module building: single-chip bumping, UBM, bonding; gold studs, ACP/ACF, Cu pillars; chip-to-flex, chip-to-interposer; interposer fabrication	☑	☐	☑	☐	1 Staff + 1 Stud./Postdoc/Techn.
*groups presenting at DRD3 workshop June 2024							**~30 FTE in total**



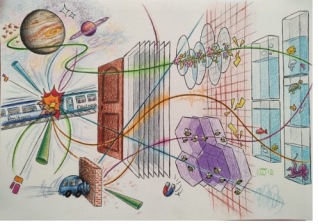
Maskless processes, single-die hybridisation

DRD3

- Interested institutes: Bonn, CERN, FBK, Geneva U, Cagliari, Firenze, Milano, KIT, LPNHE, ORNL

- Examples of previous or ongoing projects and collaborative work:
  - In-house Ni/Au plating for single dies (CERN EP R&D; linked to several external projects)
  - TimeSpot hybridisation with conductive adhesives (Cagliari, Geneva U, CERN EP R&D)
  - Timepix3 hybridisation with conductive adhesives (Geneva U, CERN EP R&D, Medipix)
  - Solder-ball jetting, gold studs (Bonn, Geneva U, CERN EP R&D, with industries)

- Scope of a possible WP / research goals to be addressed:
  - *RG 7.1: Yield consolidation for fast interconnection technologies*
  - *RG 7.2: Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to < 30 µm)*



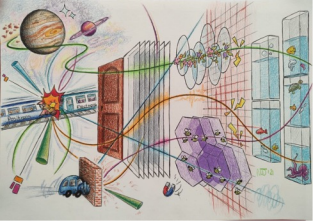
Improved classical bump-bonding processes

DRD3

- Interested institutes: Bonn, FBK, IZM, CNM, MPG-HLL, Milano, IPHC
- Examples of previous projects:
  - Support-wafer bump bonding for 25 µm pitch (IZM, CERN EP R&D)

- Scope of a possible WP / research goals to be addressed:
  - Bump-bonding techniques for small pitch
  - *RG 7.3: Development of post-processing for classical bumping interconnection*

- Several EoIs indicate interest, but currently no submitted/presented activities

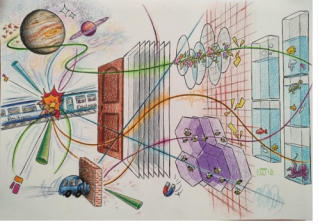


Module / 2.5D integration

- Interested institutes: CERN, FBK, Geneva U, CNM, Bari, Firenze, Milano, KIT, MPG-HLL, NIKHEF, ORNL

- Examples of ongoing projects and collaborative work:
  - 100µPET (Geneva U, EPFL, HUG Geneva)
  - MALTA compact-module studies (CERN EP R&D, Geneva U)
  - ALICE ITS3 wafer-scale bent modules (Bari, Trieste, with other ALICE institutes)
  - Timepix4 TSV bonding with ACF/ACP (Geneva U, CERN Medipix)
  - All-silicon ladder for Belle2 VTX (Bonn, IZM, Valencia)
  - 4-side buttable sensor with micro-channel cooling, interposer (MPG-HLL)

- Scope of a possible WP / research goals to be addressed:
  - *RG 7.3: Development of post-processing for classical bumping interconnection*
  - Validation of demonstrator modules (test beam, radiation hardness)
  - Integration of silicon photonics chips

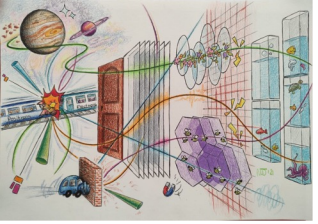


3D integration

- Interested institutes: Bonn, FBK, IZM, Trieste, IPHC, Lyon, MPG-HLL

- Examples of ongoing projects and collaborative work:
  - AIDAinnova wafer-to-wafer bonding with Timepix3 (Bonn, IZM)

- Scope of a possible WP / research goals to be addressed:
  - *RG 7.4: Development of wafer-to-wafer approach in presently advanced interconnection*
  - *RG 7.5: Development of VIAS in multi-tier sensor/front-end assemblies*
  - Activity directly addresses *DRD-T3.4 - develop full 3D-interconnection technologies for solid state devices in particle physics*



Points for discussion

- Received 18 EoIs for interconnect activities, ~30 FTE
  - 35 groups had expressed interest in initial questionnaire
  - No concrete WP project proposals submitted yet
    - no clear prospects for added benefits, such as dedicated new funding for WP projects

- Several institutes already pursue interconnect activities
  - 4 institutes presented ongoing activities today
  - Mostly linked to various ongoing / approved projects (also large overlap with AIDAinnova WP6)
  - Interconnects have typically *supporting* role for WG1/2 activities and/or other approved projects, rather than being focused *strategic R&D*

- Links to other WGs and DRDs:
  - WG7 provides interconnect technologies for hybrid (WG2) and monolithic (WG1) sensors
    - Typically comes at a later stage of R&D, when seizable demonstrator chips are available
  - WG7 focuses on applications, in-house processing, evaluation; DRD7 provides access to *industrial* wafer-level 3D integration

- Proposal on how to proceed:
  - Define a few *light-weight* WP projects in the coming weeks, based on ongoing / newly proposed developments
  - Add more ambitious *strategic R&D* project(s) at a later stage, when funding and reviewing schemes become more clear?