

1st DRD3 week on Solid State Detectors R&D
18th June 2024

First characterisation of Trench Isolated LGADs fabricated at Micron Semiconductor Ltd

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Outline

- Motivation
- Segmentation Techniques
- Fabrication
 - TCAD simulations
 - Run
 - Electrical Measurements
- TCT Measurements
 - Gain
 - Pixel Isolation
 - Inter-pixel distance (IPD)
- Discussion
- Summary & Future Work

Motivation

- To develop a fast-timing silicon hybrid pixel detector (sub 100ps) , within the working group **PixelGAD**, a UK based effort to develop LGAD technology.
- We must understand the LGAD technology, build simulation models and develop a fabrication process in collaboration with Micron Semiconductor.
- Detector should be for HEP experiments with modest radiation levels which require fast timing and good spatial resolution **(i.e. LHCb Velo II Upgrade)**.
- Detector applications include imaging **"soft"** or **"tender"** (< 5 keV) energy x-rays, with focus on the water window (~500 eV).
- The detectors will be applicable to and demonstrated on **synchrotron beamlines** and for **electron microscopy**.
- We do not target a given experiment but aim to push the small pixel LGAD technology and demonstrate this with start-of-the-art small pixel fast timing pixel chips.
- We want to create an imaging detector in collaboration with the **Timepix4** readout ASIC.

Pixel Segmentation

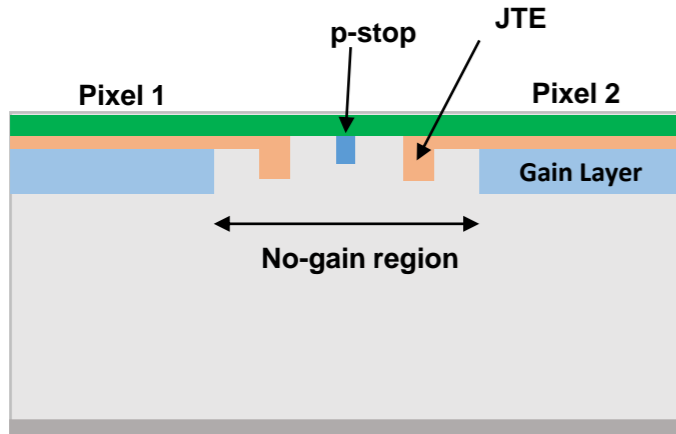


Fig 1(a): Standard LGAD

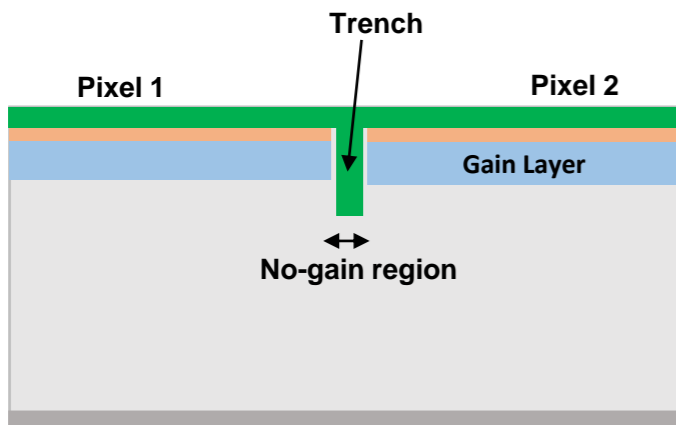


Fig 1(b): Trench-isolated LGAD

- **Standard LGADs:**

- Segmentation → Junction Termination Extension (JTE), p-stop, virtual Guard-Rings
- Large “no-gain region”
- IPD ~ 50 μm ([G. Paternoster et. al., 2021](#))
- Low fill-factor

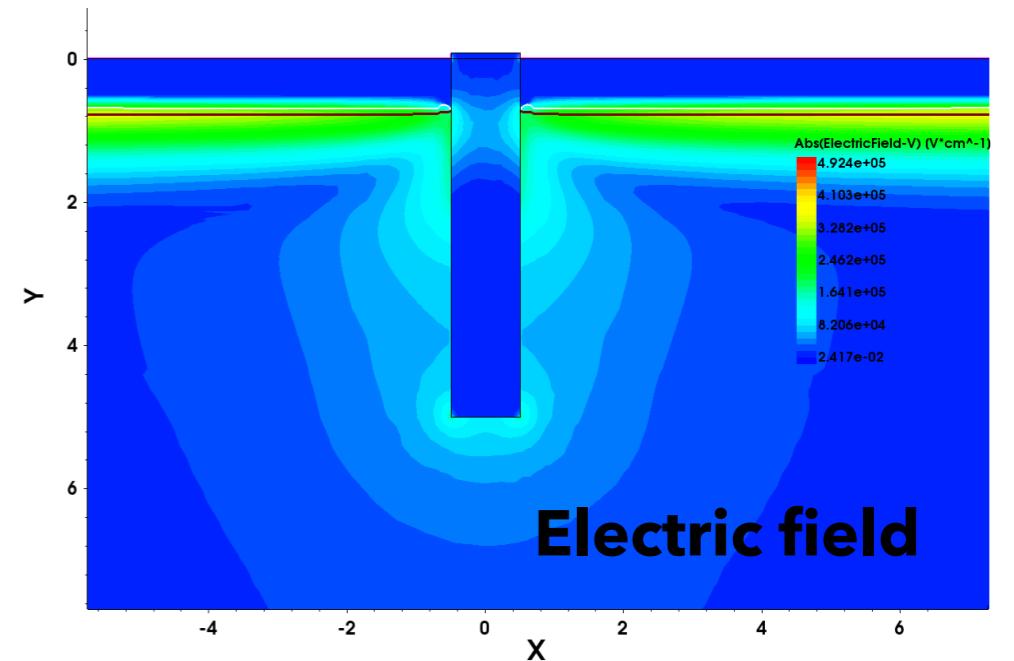
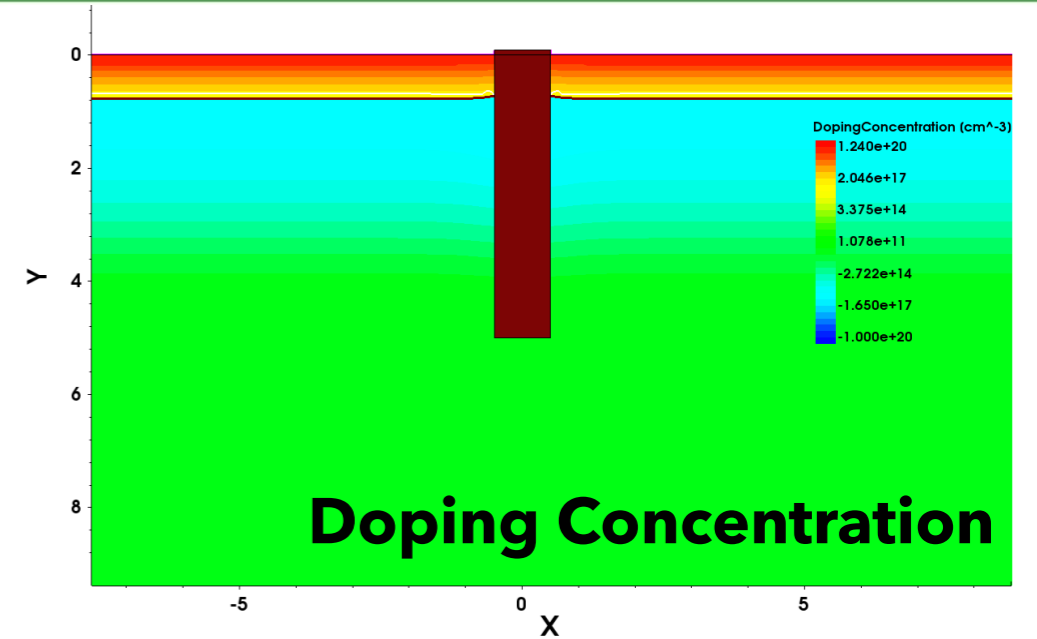
- **Trench-Isolated LGADs:**

- Segmentation → **Trenches** (SiO_2 filled)
- 1 μm wide, and a few microns deep
- “no-gain region” is significantly reduced
- Fill-factor is increased
- Enhanced spatial resolution

[G. Paternoster, et. al., 2017](#)

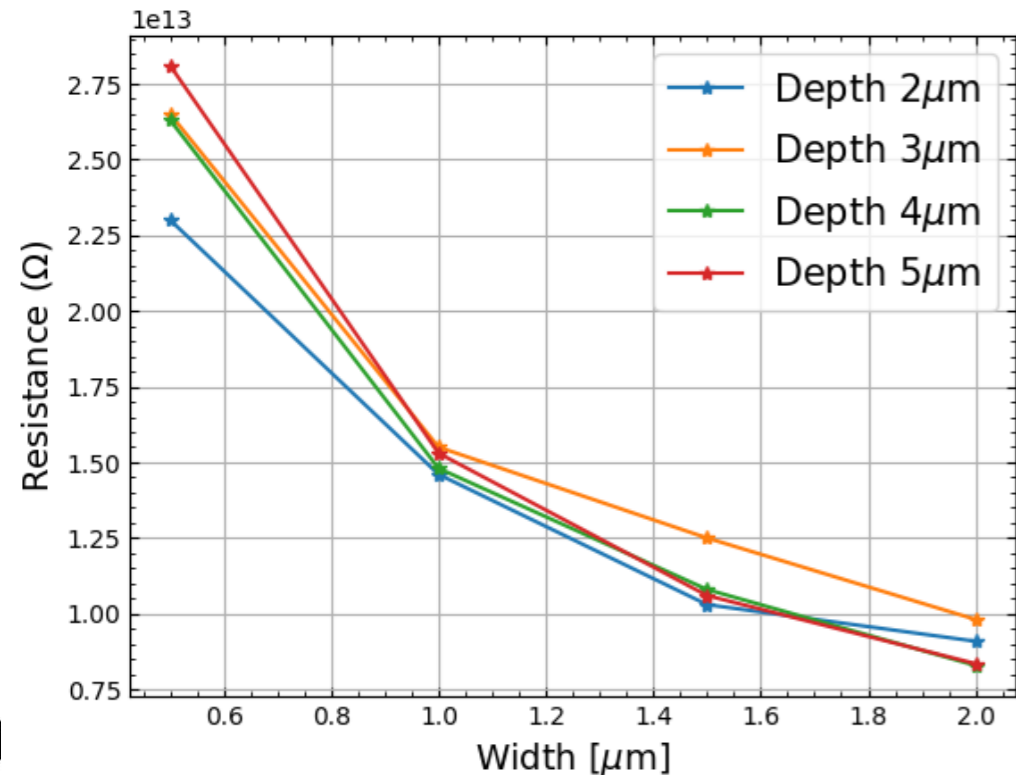
Simulations (I)

- **Sentaurus TCAD** model used to create two adjacent pixels.
- Trench used to isolate the pixels.
- Trenched etched in silicon - **No gap** between trench and implantations

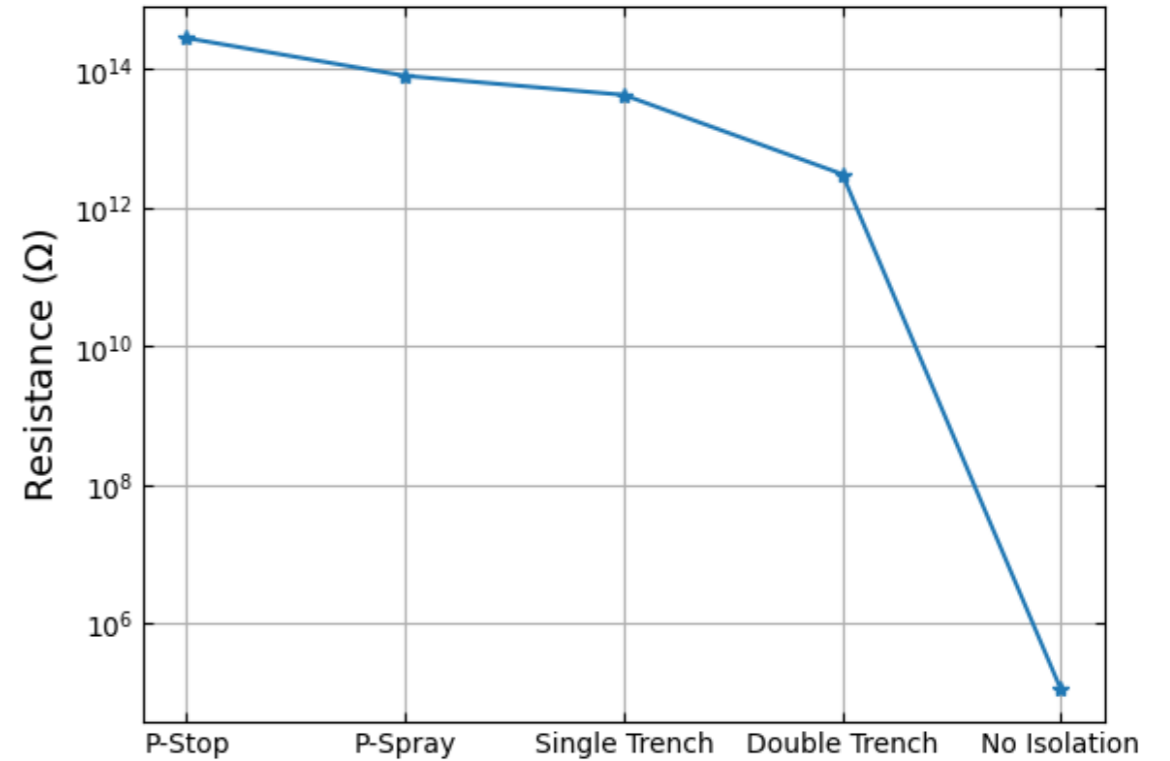


Simulations (II)

- Isolation determined by the resistance between the adjacent pixels. **Must be high resistance up to oxide charge saturation.**
- Isolation compared to standard isolation methods. i.e. p-spray and p stop.



Trench parameters optimised for highest isolation

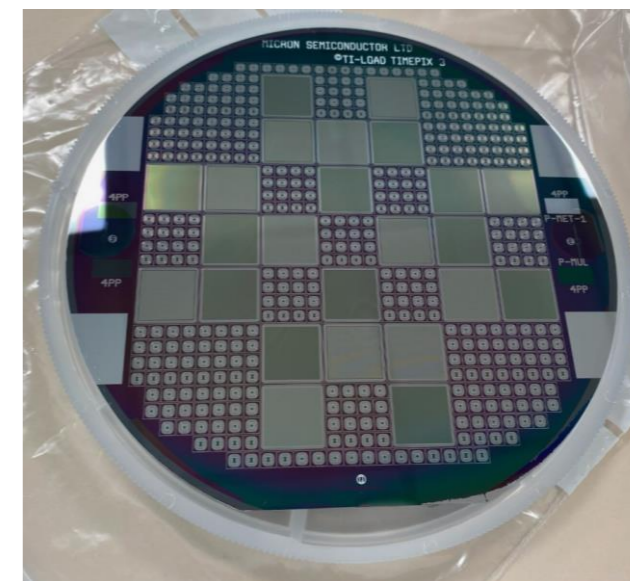
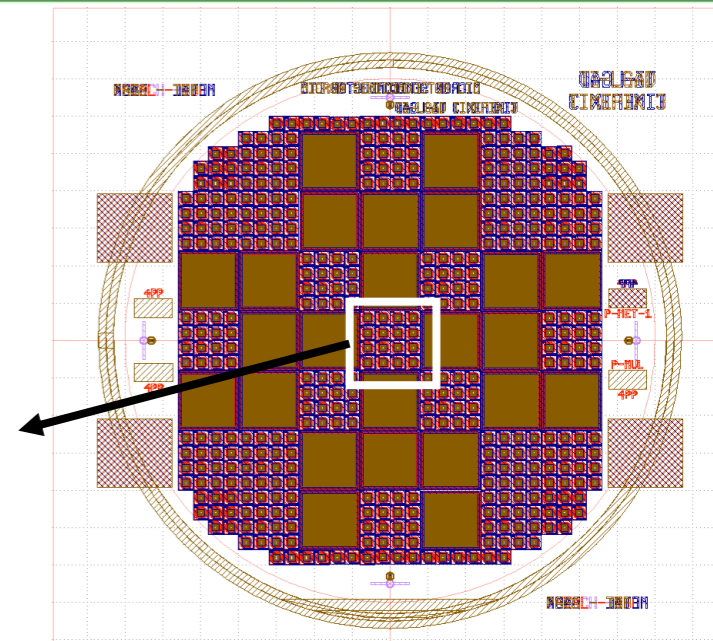
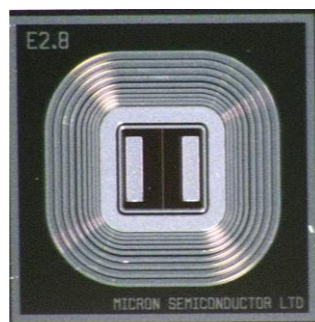
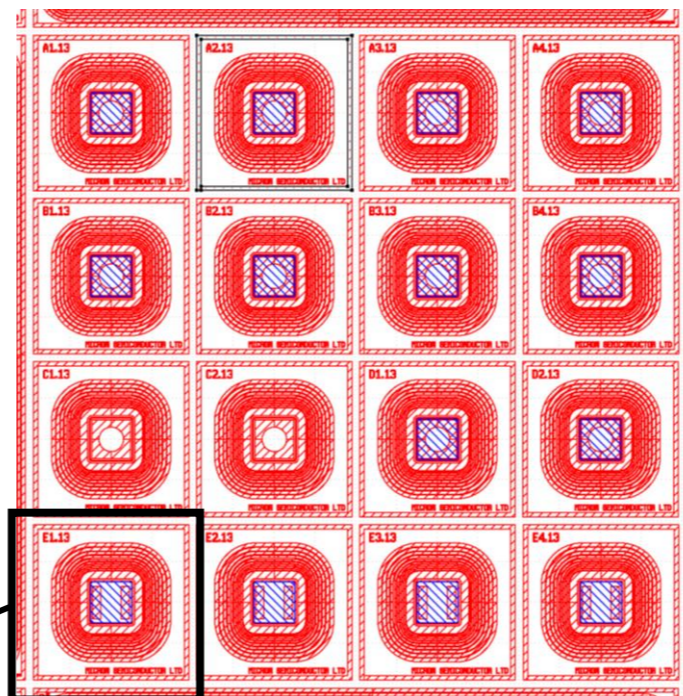


Comparison of isolation methods between adjacent pixels: p-spray, p-stop, no-isolation, single-trench, double-trench

Production of TI-LGADs

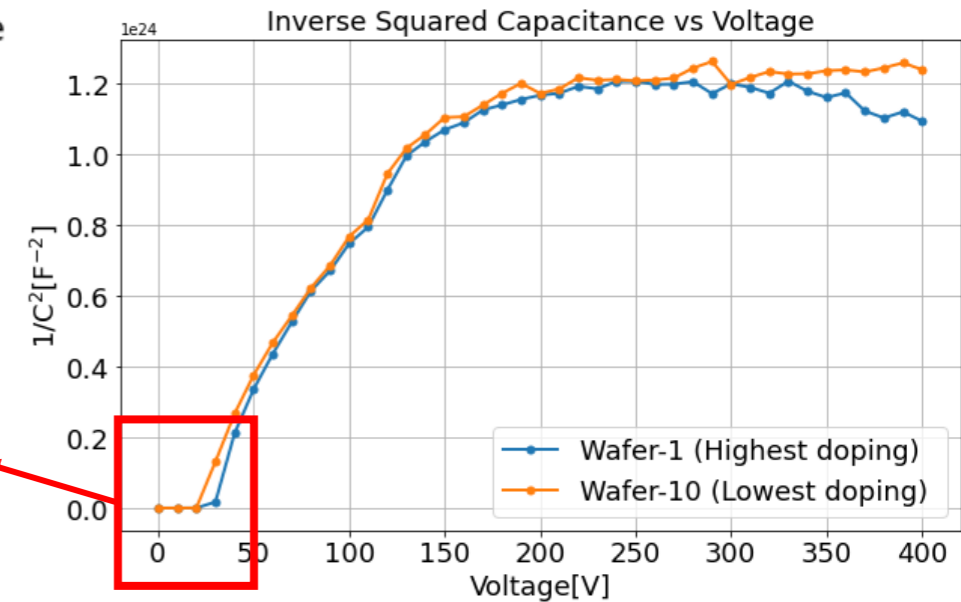
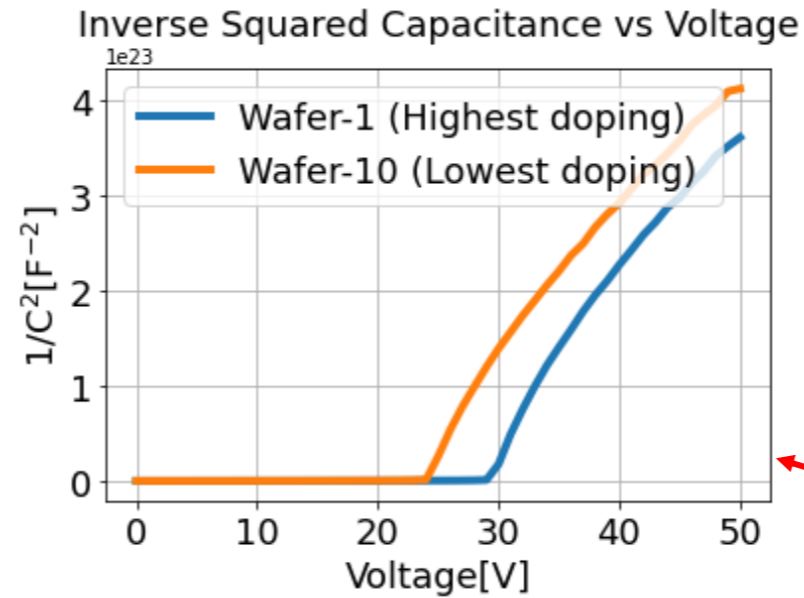
Run-3455 produced by Micron Semiconductor Ltd:

- Wafer production based on increasing gain layer doping
- Active thickness = 250 μm
- Pad area = 1x1 mm²
- Devices:
 - A: 1x1 LGADs with JTE
 - B: 1x1 LGADs with JTE + Trench
 - C: 1x1 PIN (no gain)
 - D: 1x1 LGADs with Trench
 - E: 1x2 Pixels, isolated with Trench
- Medipix Arrays:
 - 55 μm pitch
 - 110 μm pitch



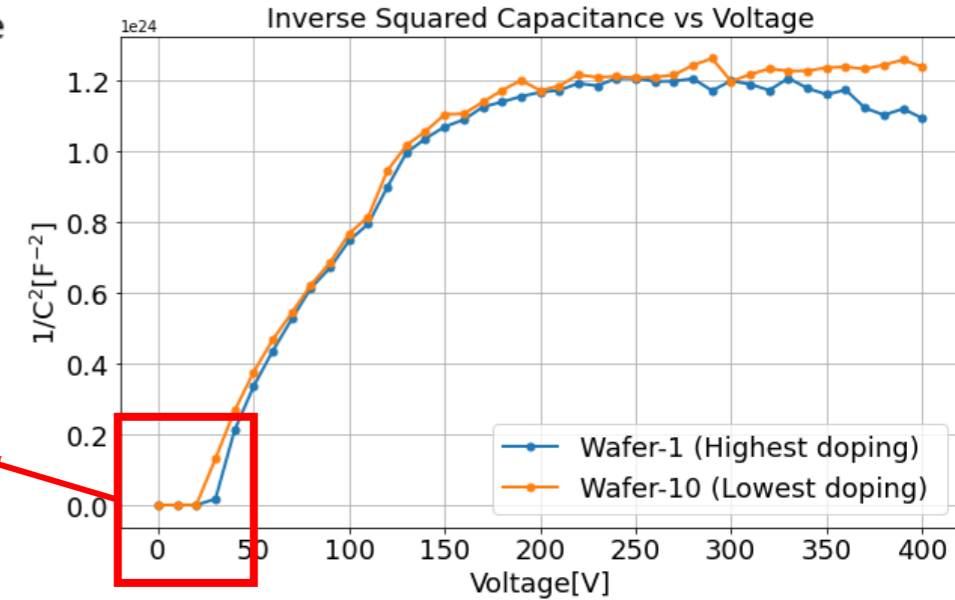
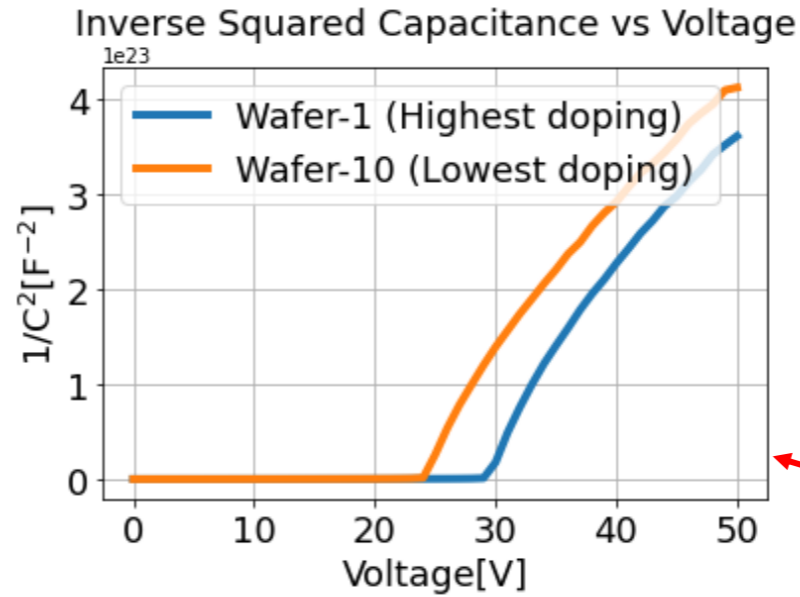
Electrical Measurements (I)

- Capacitance-Voltage (CV):
 - Gain layer depletion voltage, $V_{GL} = 25-30\text{ V}$
 - Full depletion $\sim 120\text{V}$



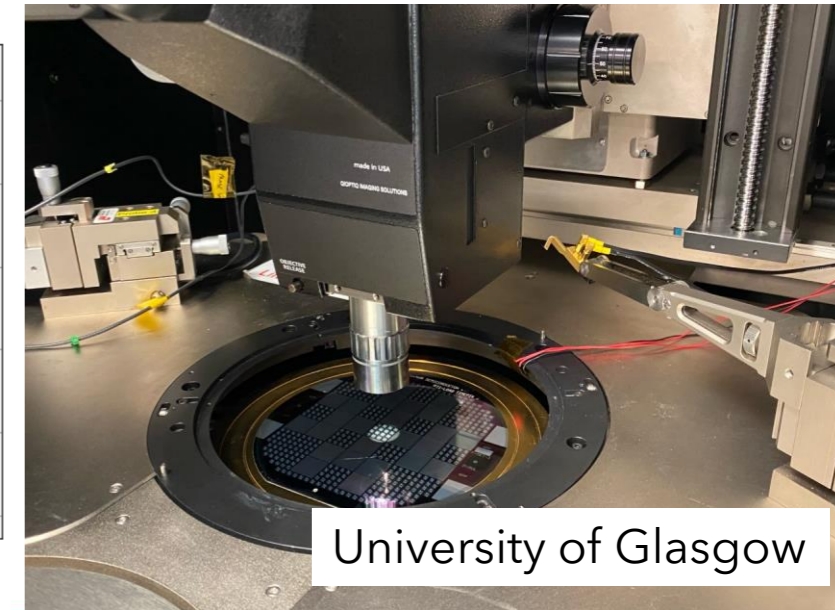
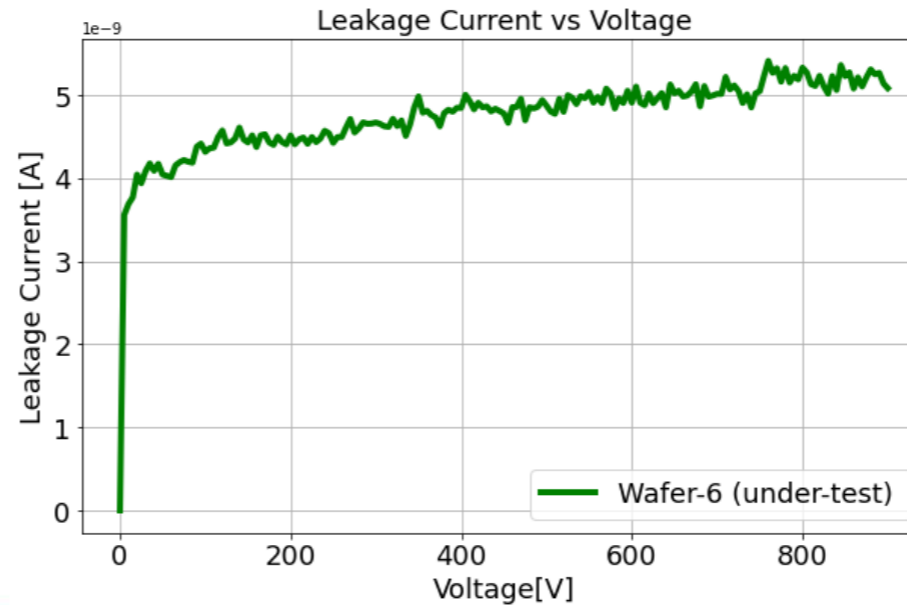
Electrical Measurements (II)

- Capacitance-Voltage (CV):
 - Gain layer depletion voltage, $V_{GL} = 25-30\text{ V}$
 - Full depletion $\sim 120\text{ V}$



- Current-Voltage (IV):
 - No sign of breakdown up to 1000V
 - Leakage current is in nA's

➤ Devices are working!

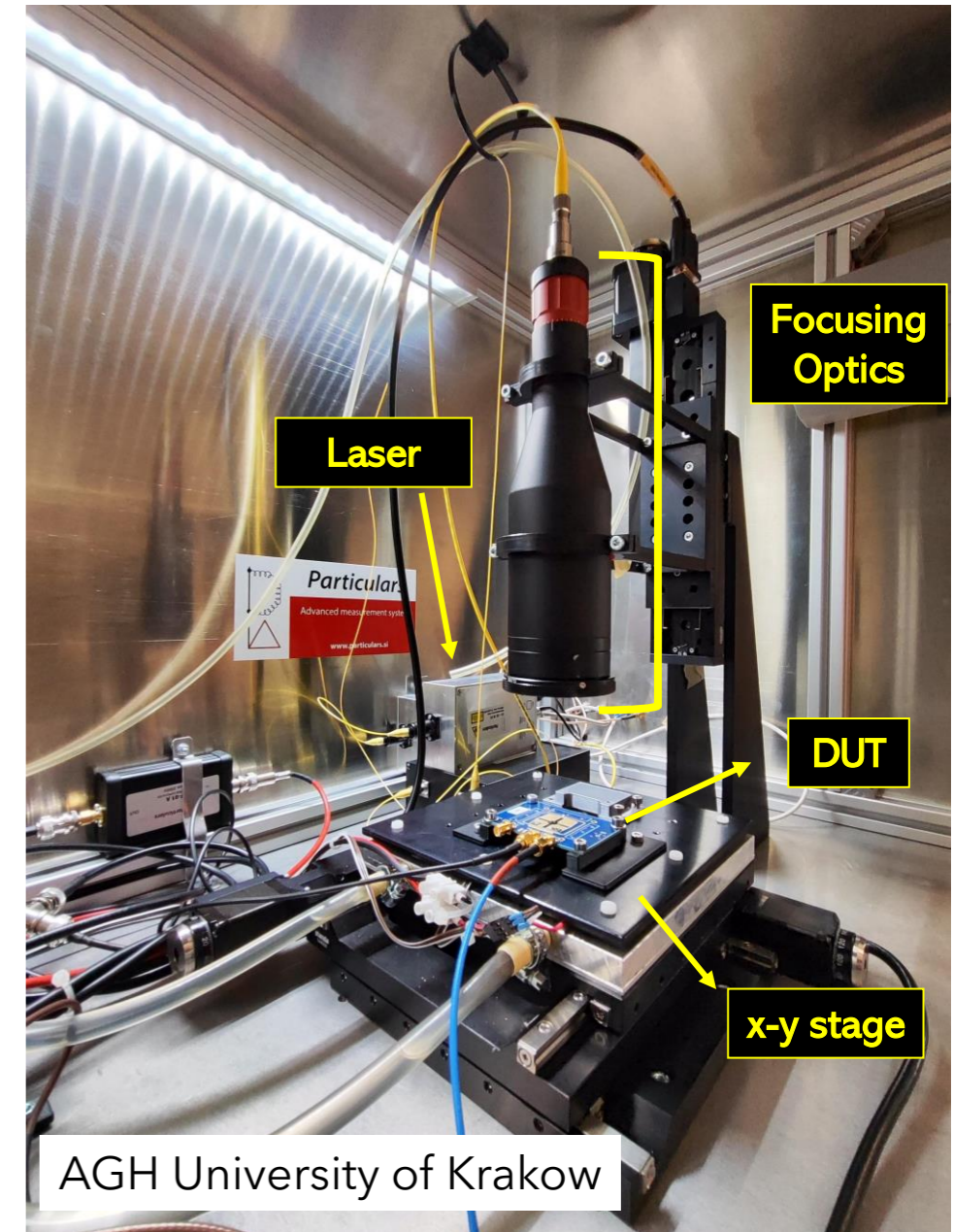


University of Glasgow

Transient Current Technique (TCT)

Particulars TCT Setup:

- IR pulsed laser (1064 nm) → 8-10 μm spot
- Broadband amplifier → 35 db
- Laser calibrated to minimum ionizing particles (MIPs)
- xy-stage with sub- μm precision



AGH University of Krakow

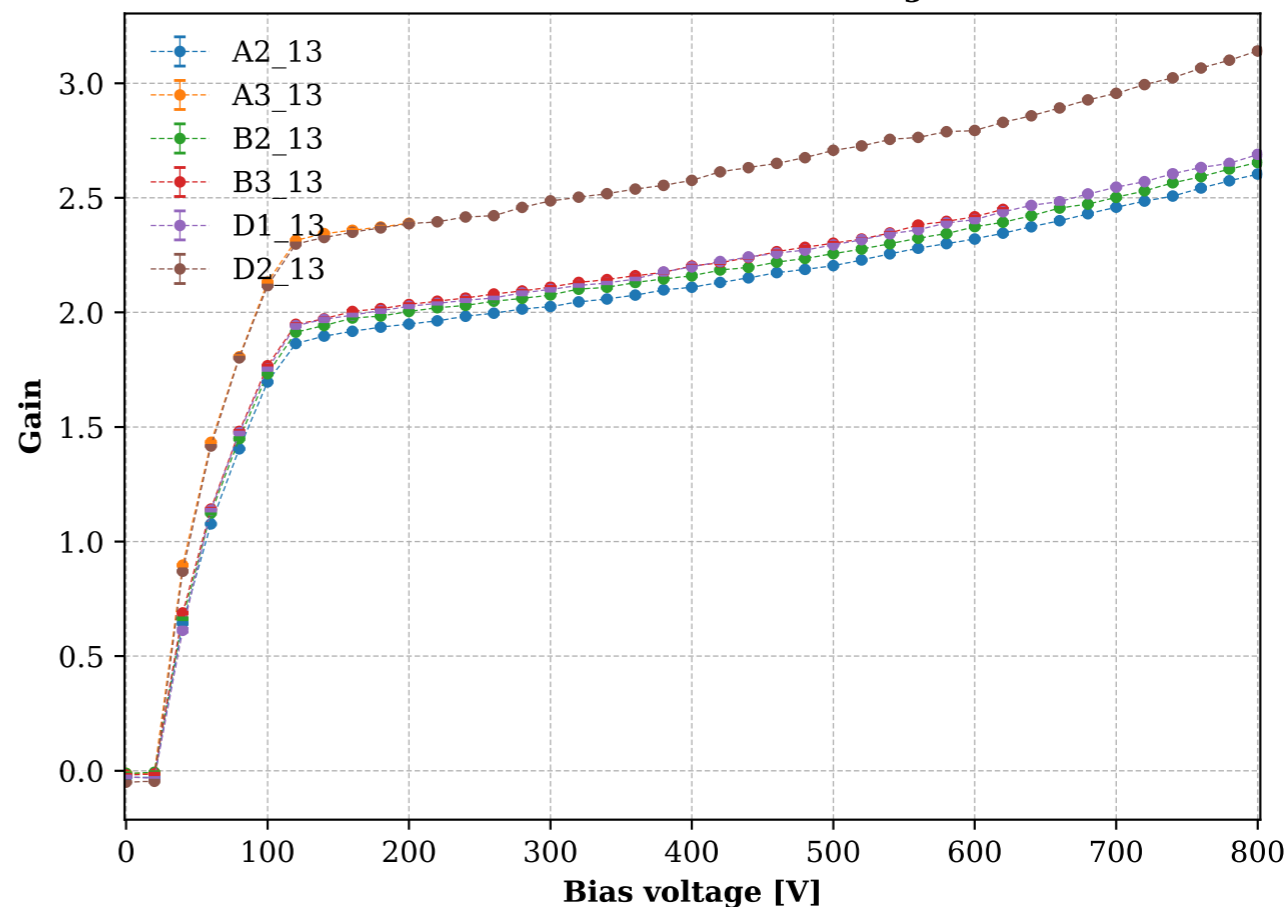
TCT: Gain Measurements

- Gain is calculated by:

$$Gain = \frac{Q_{LGAD}}{Q_{PIN}}$$

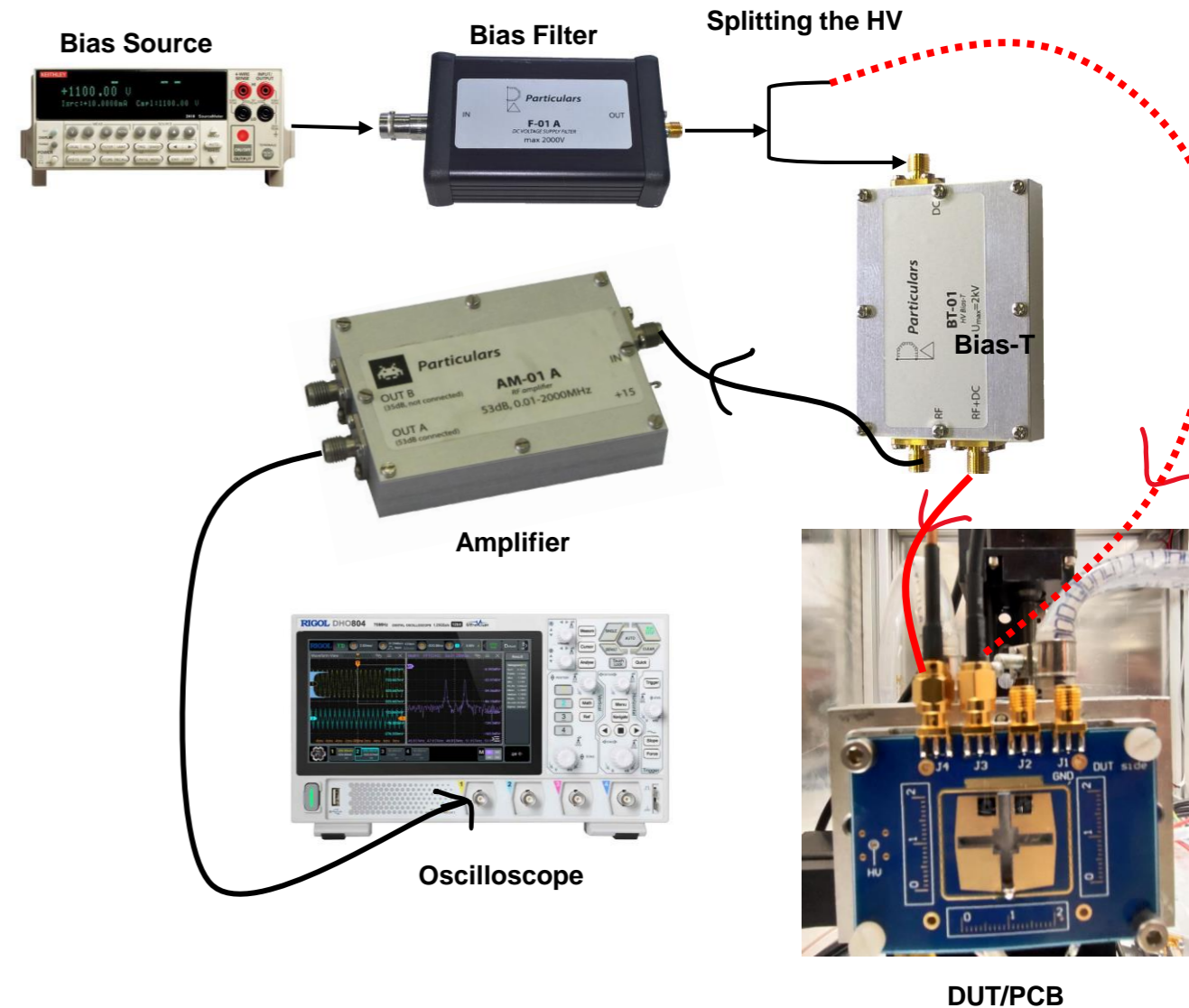
- Gain of the tested wafer (2nd lowest GL doping) is between 2-3.

200um Trench LGAD: Gain as a Function of Voltage for different devices



TCT: Pixel Isolation

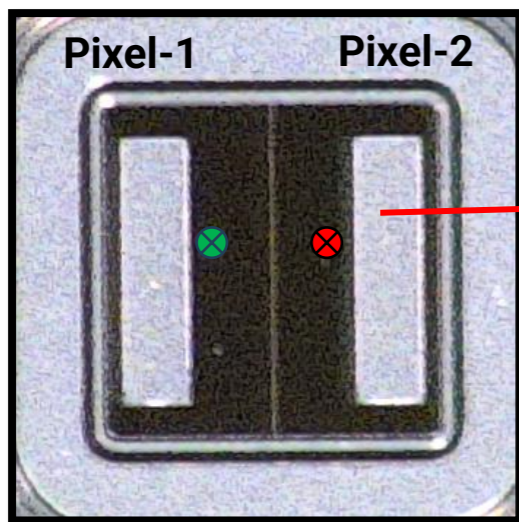
- One pixel connected to the readout
- Other pixel is only connected to bias voltage



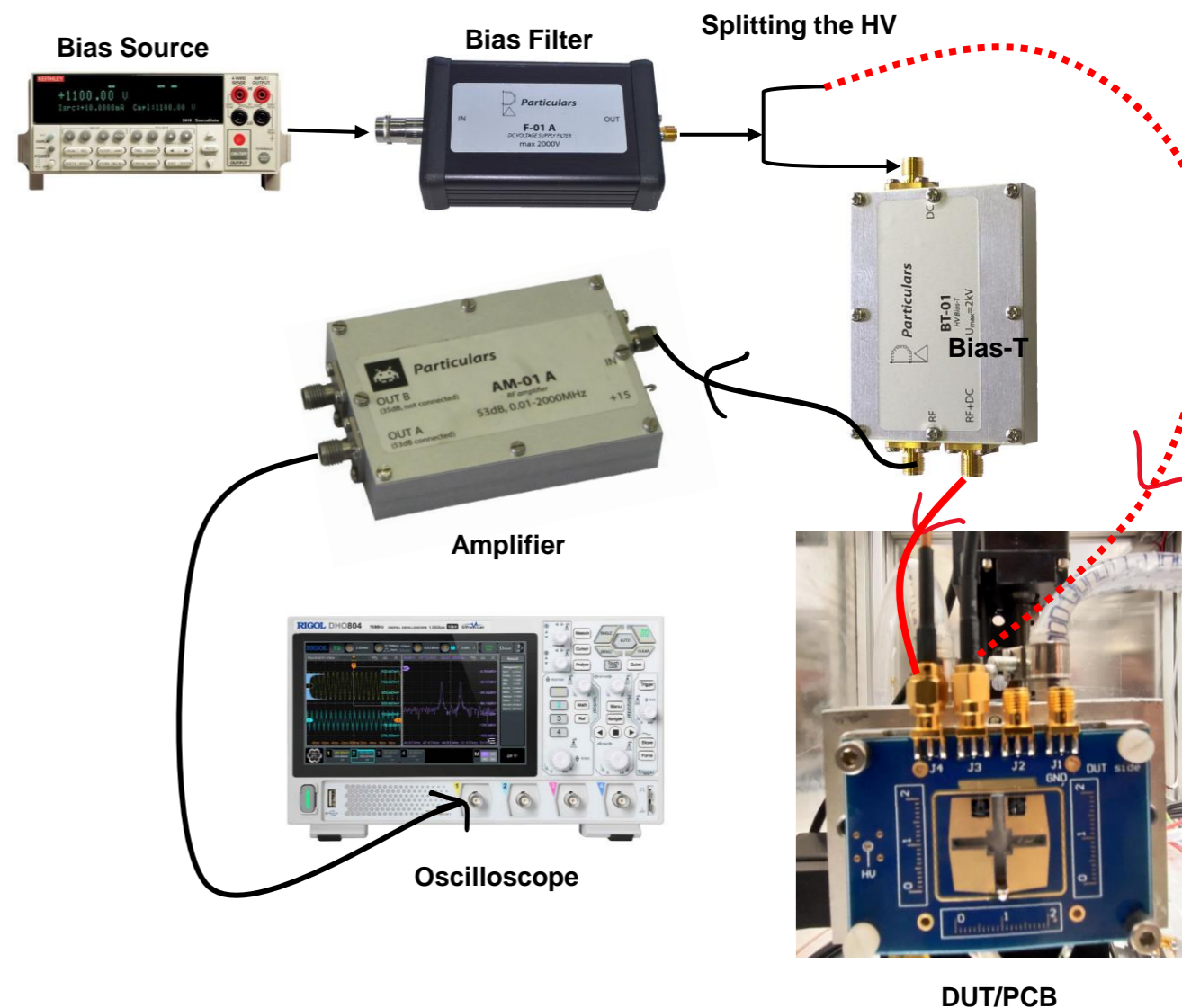
Schematics of measurement setup for pixel isolation

TCT: Pixel Isolation (II)

- One pixel connected to the readout
- Other pixel is only connected to bias voltage



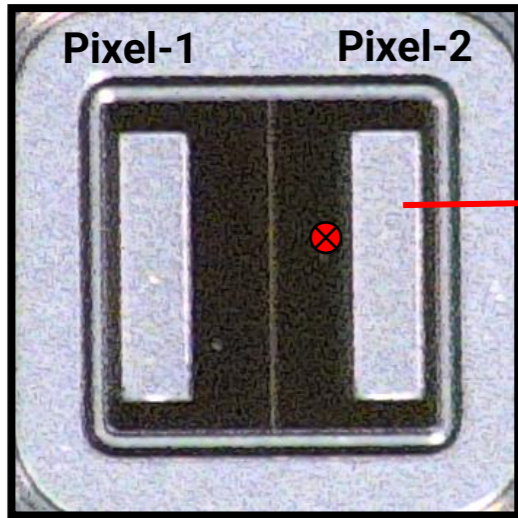
Connected to readout



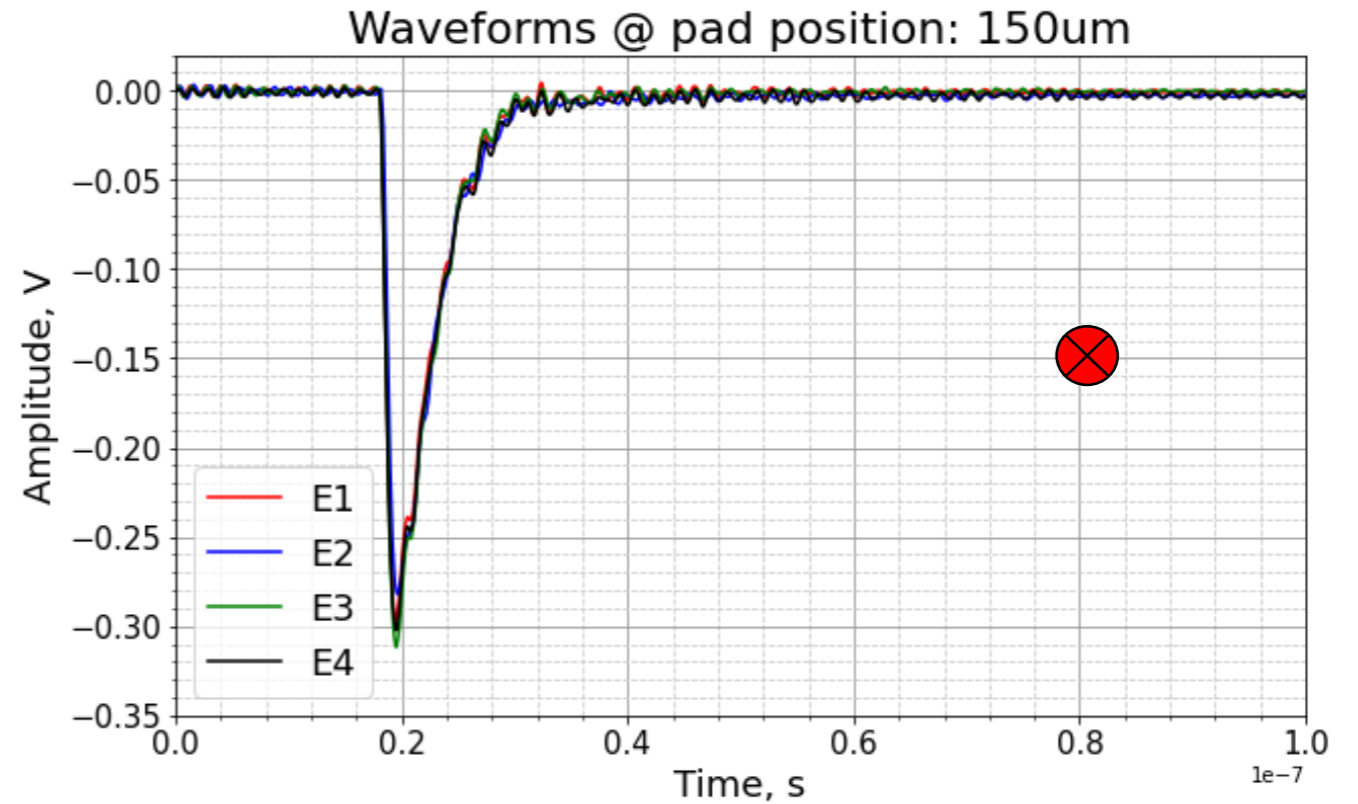
Schematics of measurement setup for pixel isolation

TCT: Pixel Isolation (III)

- Laser is shot on **pixel-2**, which is connected to readout.
- Signal is observed for all the devices.

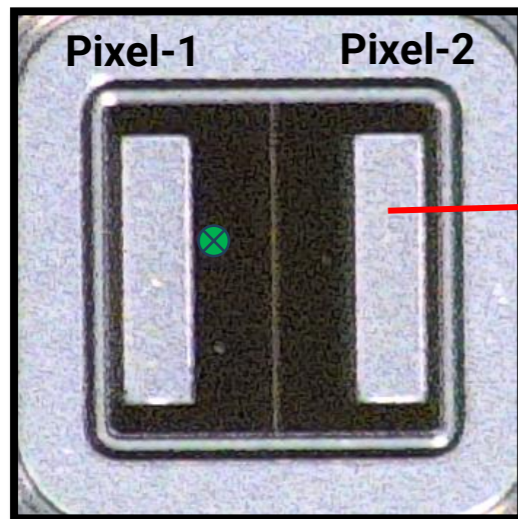


Connected to readout

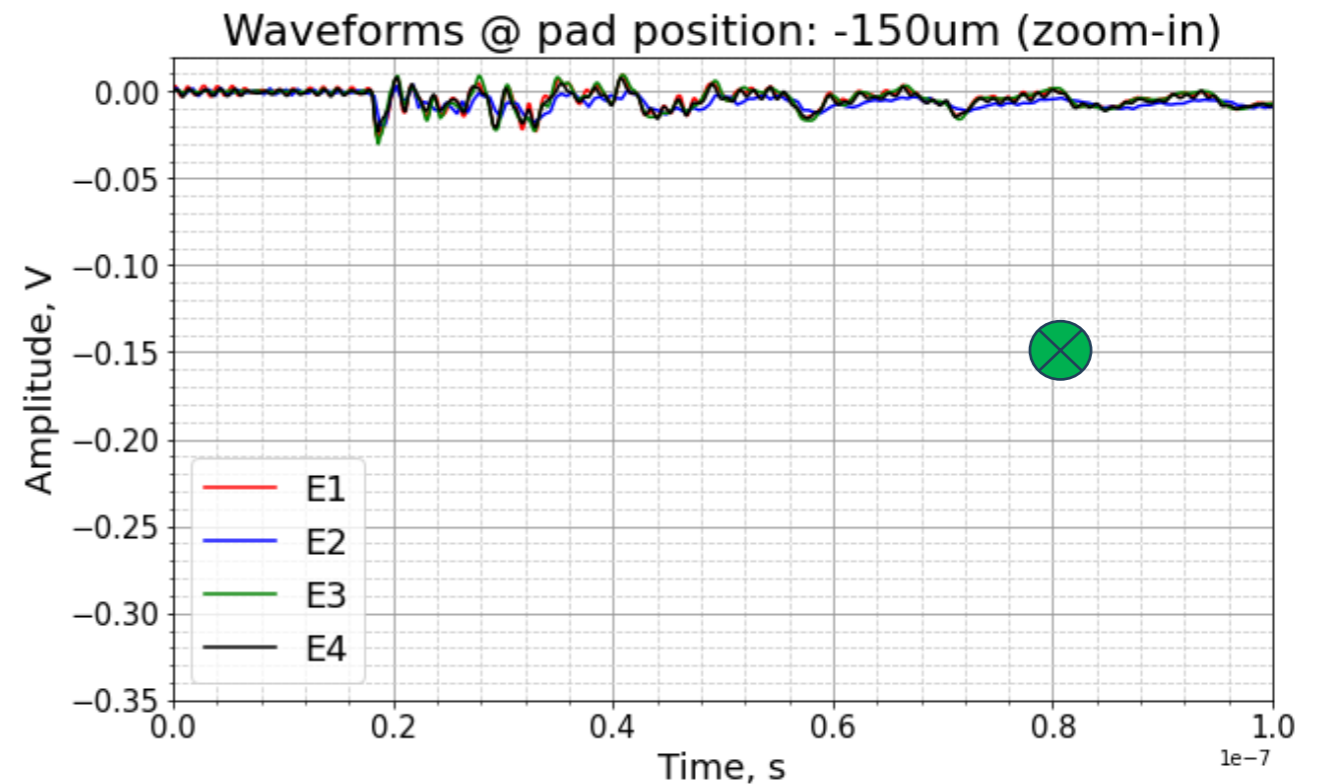


TCT: Pixel Isolation (IV)

- Laser is shot on **pixel-1**, which is not connected to readout.
- No Signal is observed for any device.
- Pixels are **isolated!** Trenches are **working!**

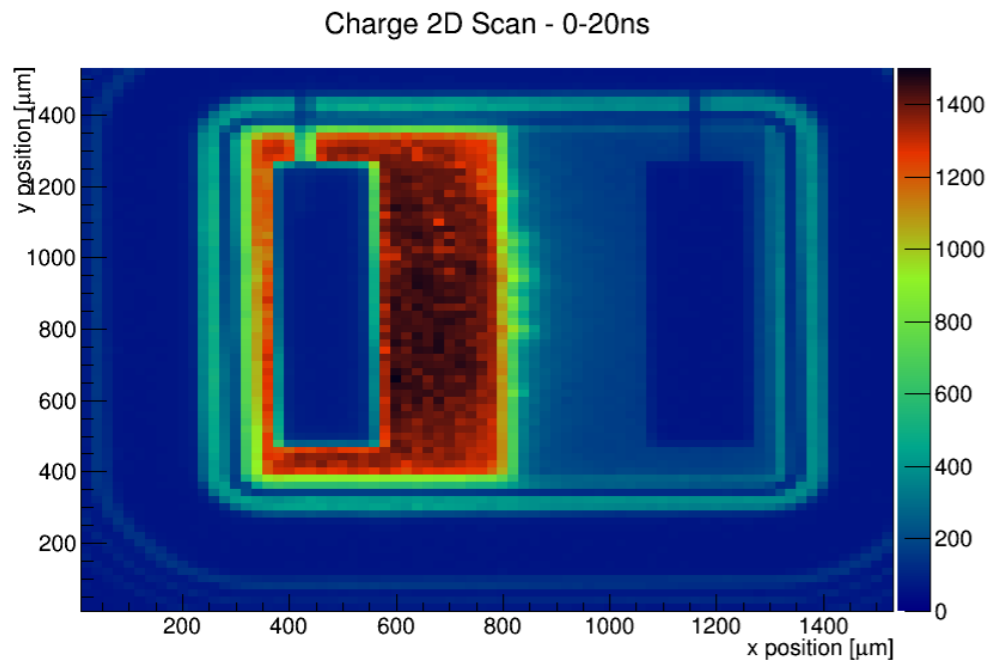
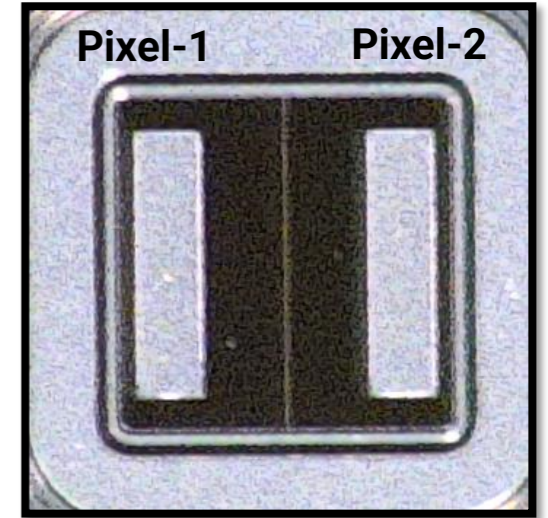


Connected to readout

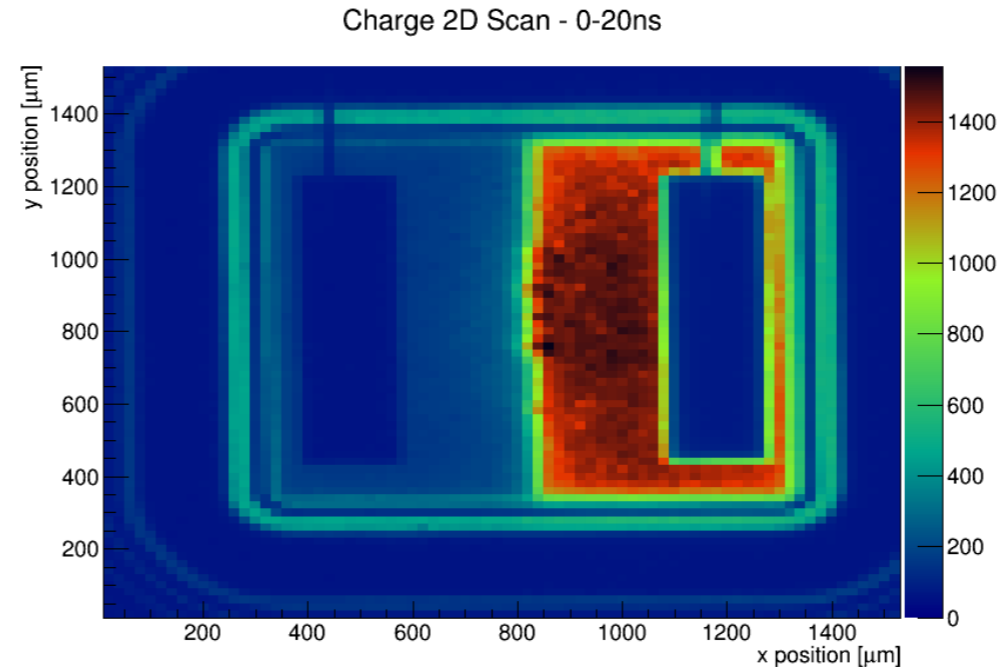


TCT: Pixel Isolation (2D Maps)

- One pixel connected to the readout
- Other pixel is only connected to bias voltage
- 2-dimensional (x-y) scans also depicts isolation between the pixels



Pixel-1 Connected to readout



Pixel-2 Connected to readout

TCT: Inter-Pixel Distance

- Measuring the “no-gain region” also referred to as inter-pixel distance (IPD).
- 1-dimensional scans along the x-position, and plot charge vs position for both pixels.
- Distance between the two pixels where normalized charge reaches 50% of its value.

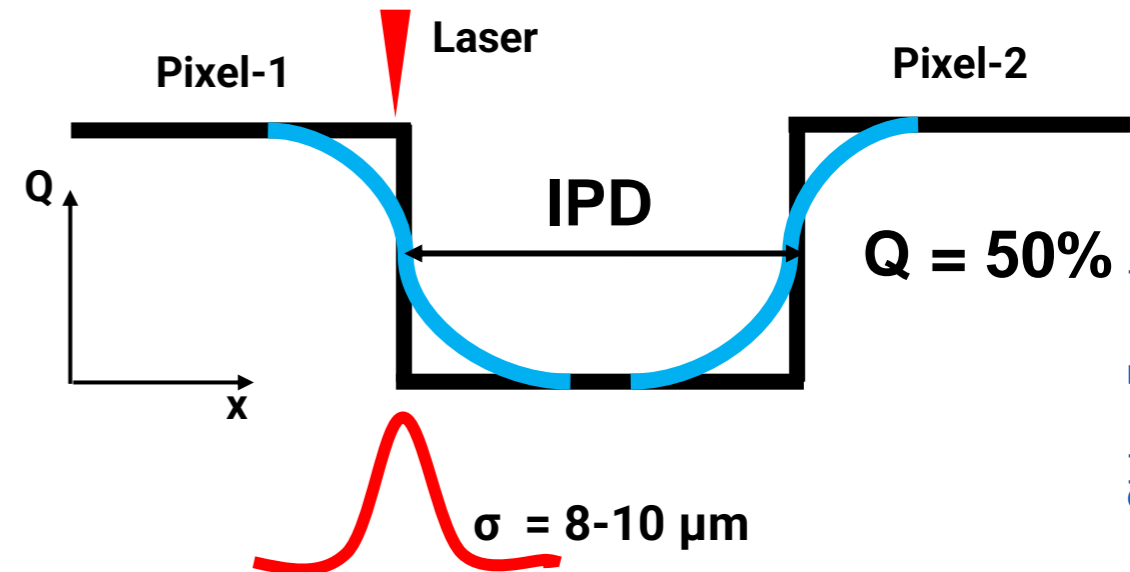


Fig: Schematics of IPD calculation

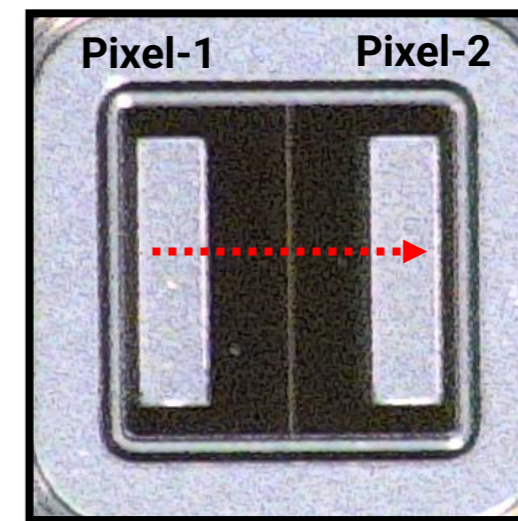


Fig: 1-dimensional scan in the x-direction

TCT: Inter-Pixel Distance (II)

- Measuring the “no-gain region” also referred to as inter-pixel distance (IPD).
- 1-dimensional scans along the x-position, and plot charge vs position for both pixels.

- Distance between the two pixels where normalized charge reaches **50%** of its value.

- Fit the s-curve on the charge obtained from each pixel, given

by:

$$f(x) = c_1 * \left[1 \pm \operatorname{erf}\left(\frac{x - c_2}{c_3}\right) \right] + c_4$$

- IPD is given by:

$$IPD = x_{RP(Q=0.5)} - x_{LP(Q=0.5)}$$

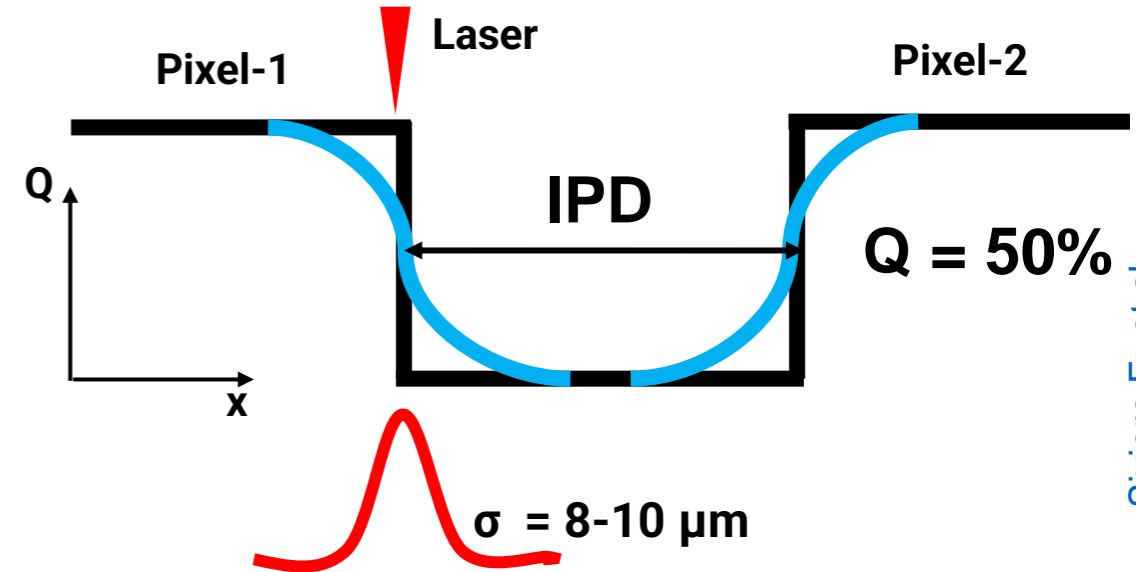
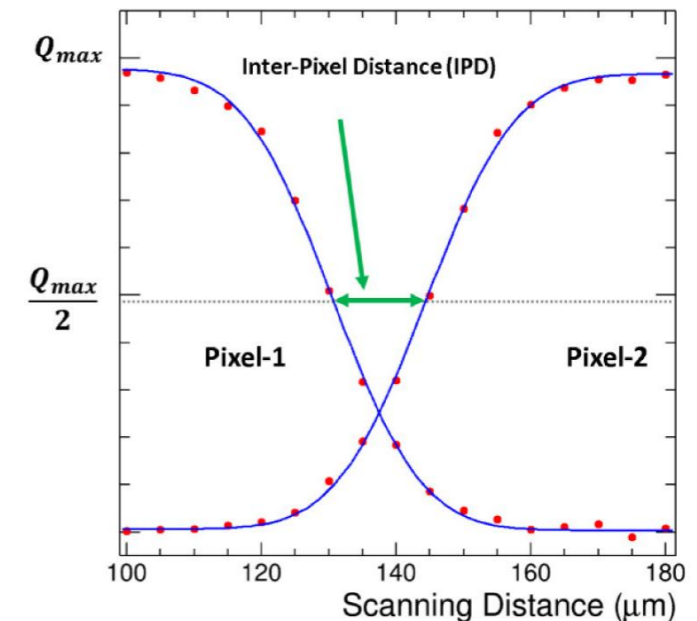
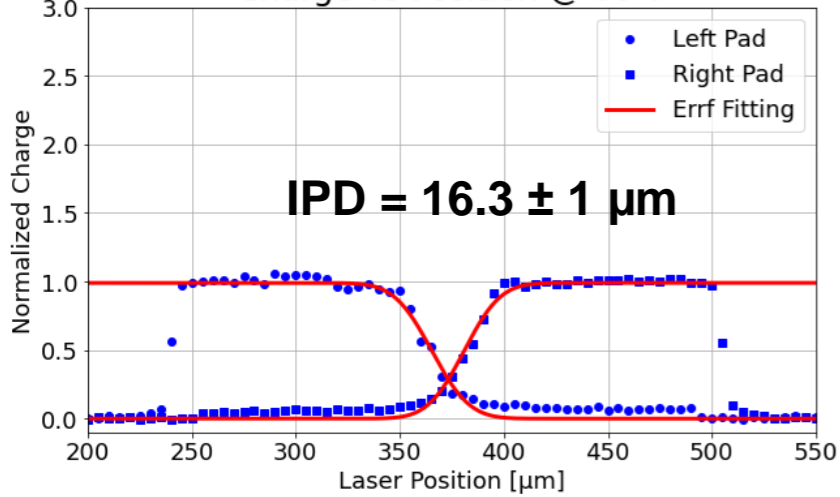


Fig: Schematics of IPD calculation

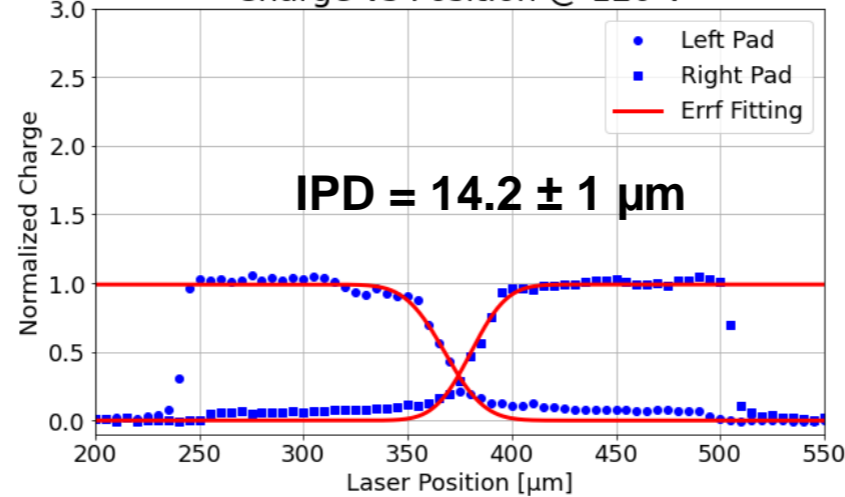


TCT: Inter-Pixel Distance (III)

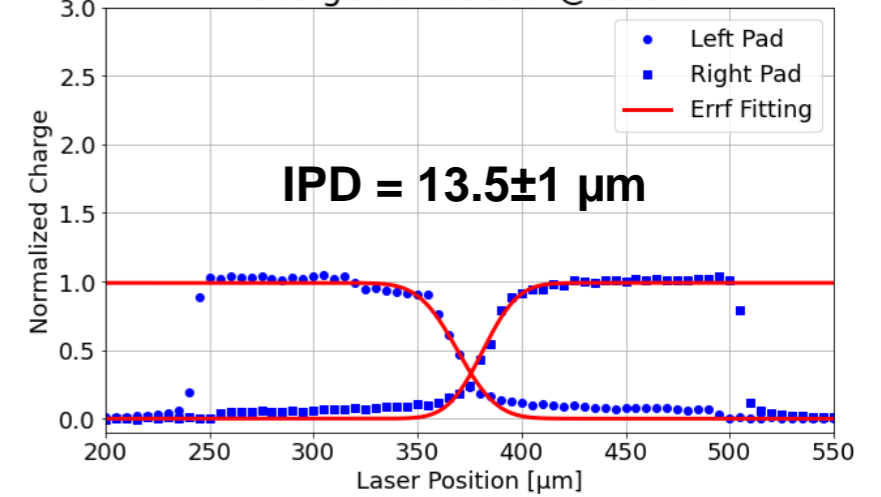
Charge vs Position @ 60 V



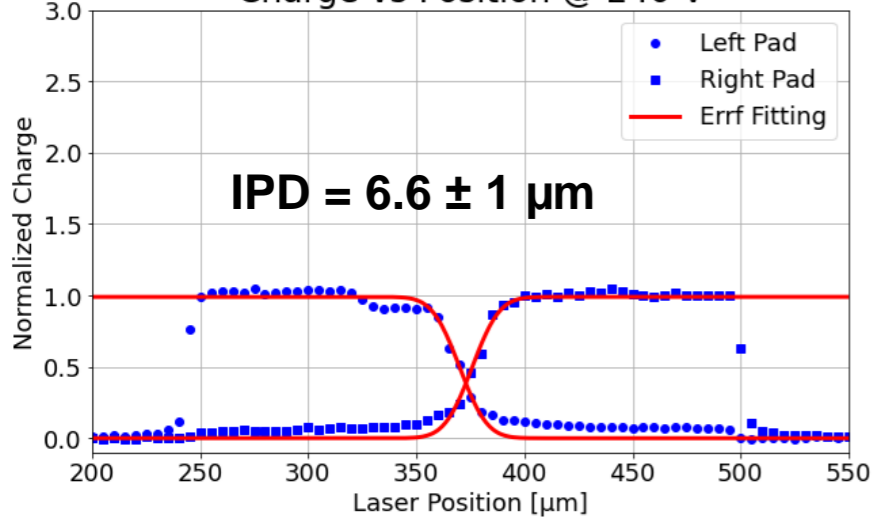
Charge vs Position @ 120 V



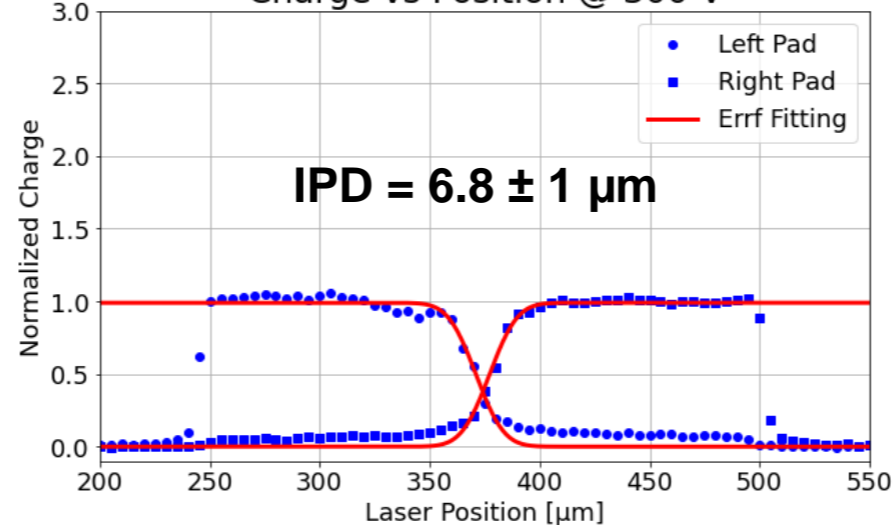
Charge vs Position @ 180 V



Charge vs Position @ 240 V



Charge vs Position @ 300 V



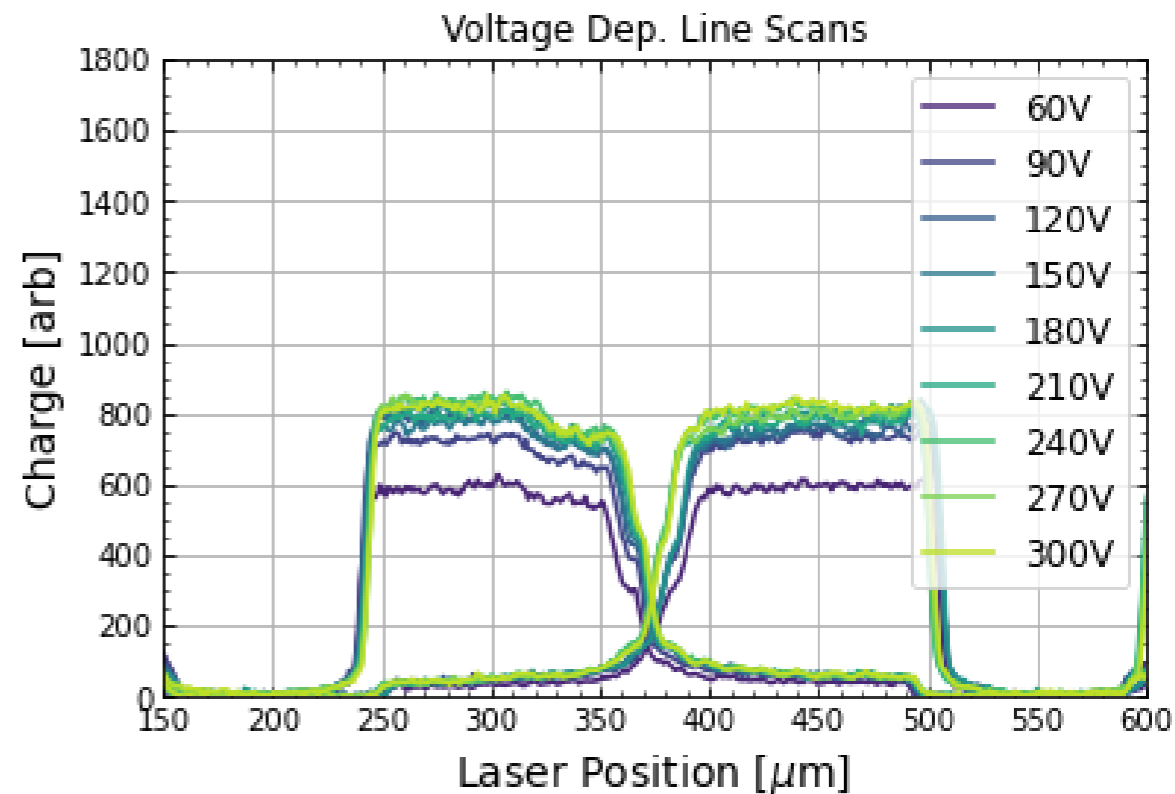
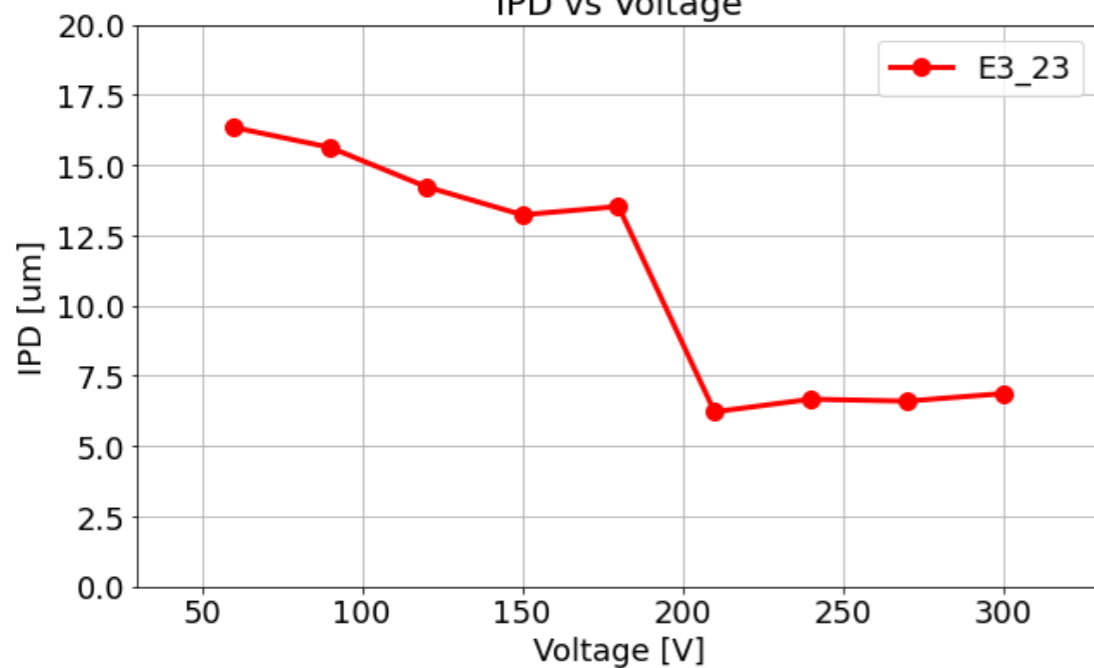
These values correspond to the
“Effective inter-pixel distance”

TCT: Inter-Pixel Distance (IV)

Interpixel distance decreases as voltage increases, as expected

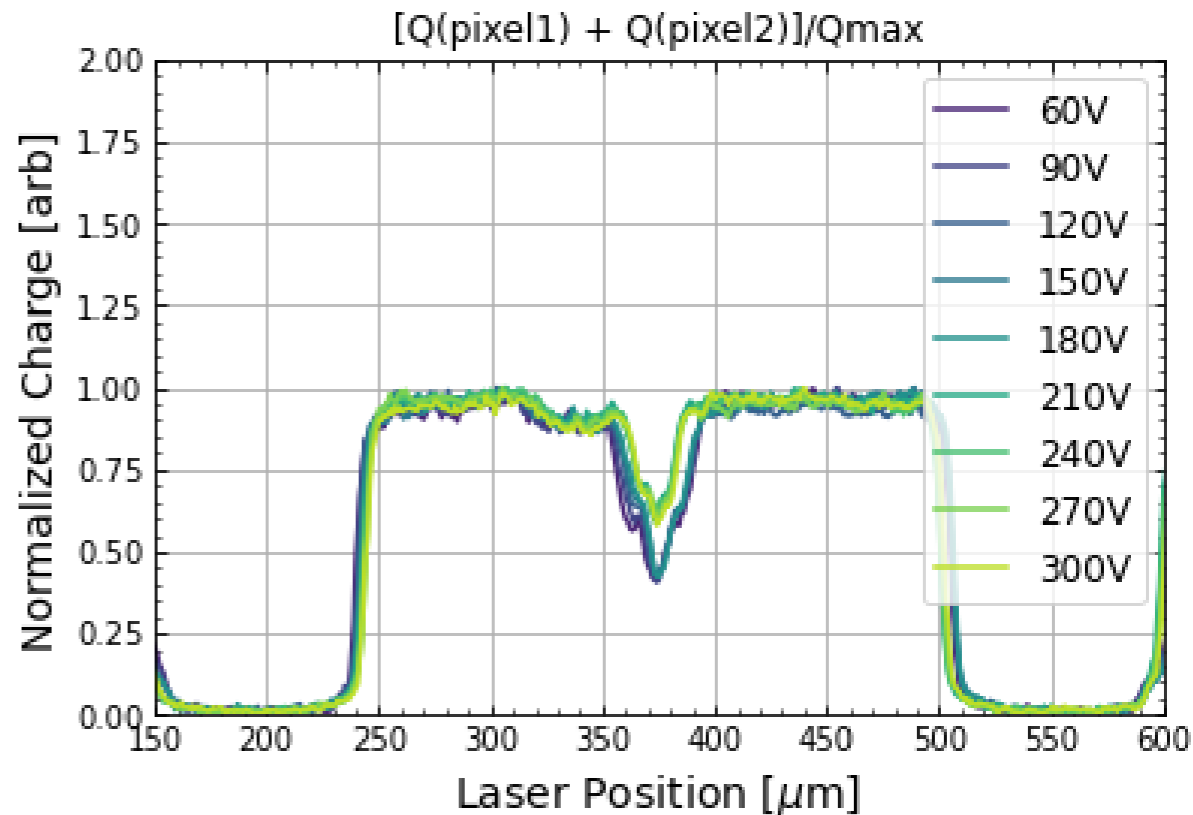
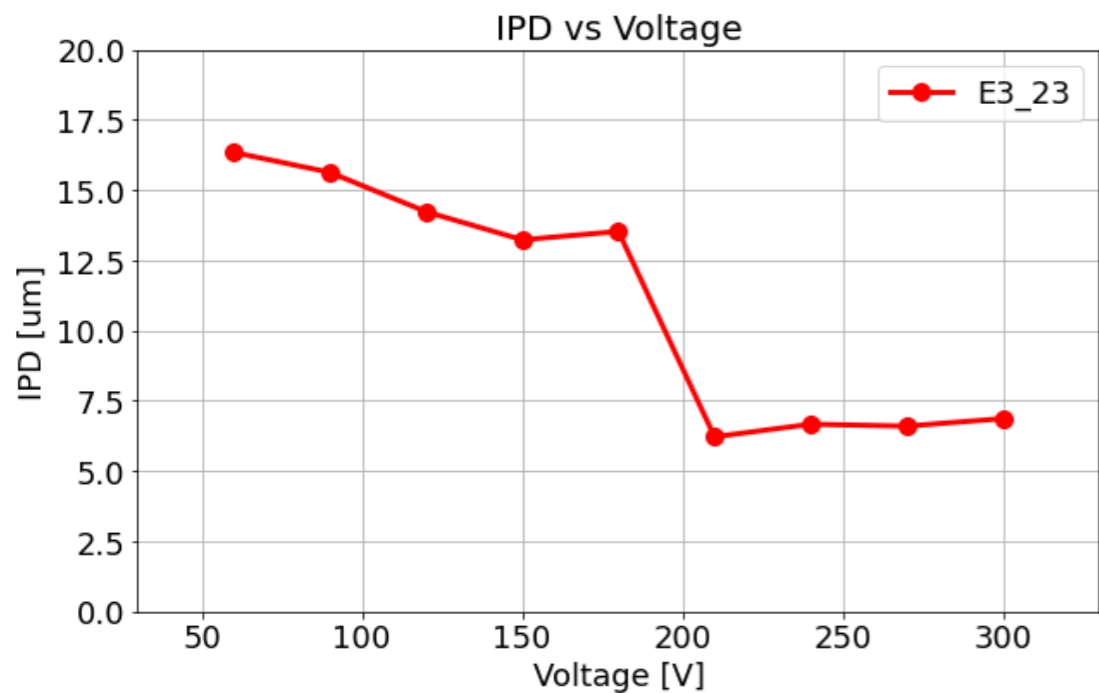


IPD vs Voltage



TCT: Inter-Pixel Distance (V)

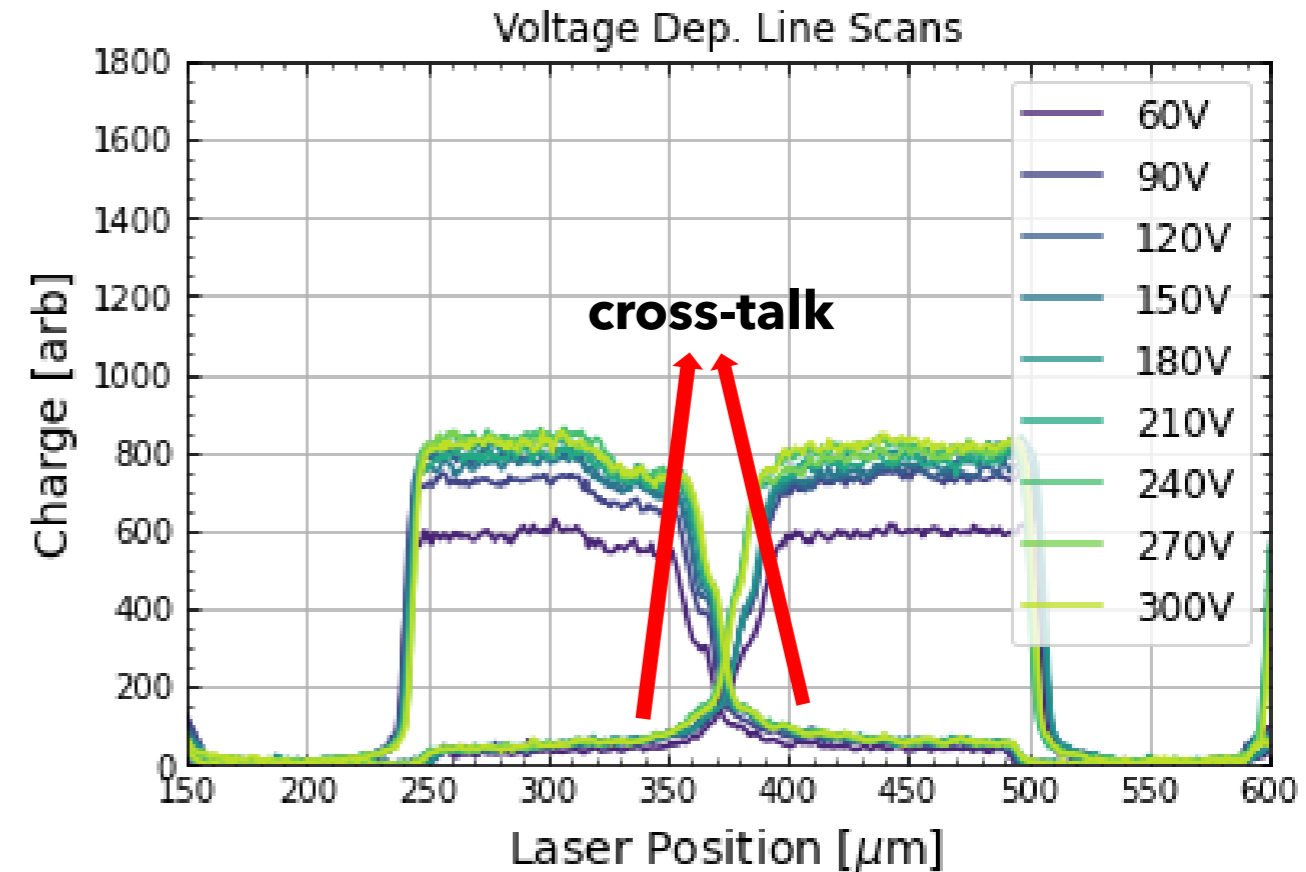
Interpixel distance decreases as voltage increases, as expected



Fill factor is nearly 97%

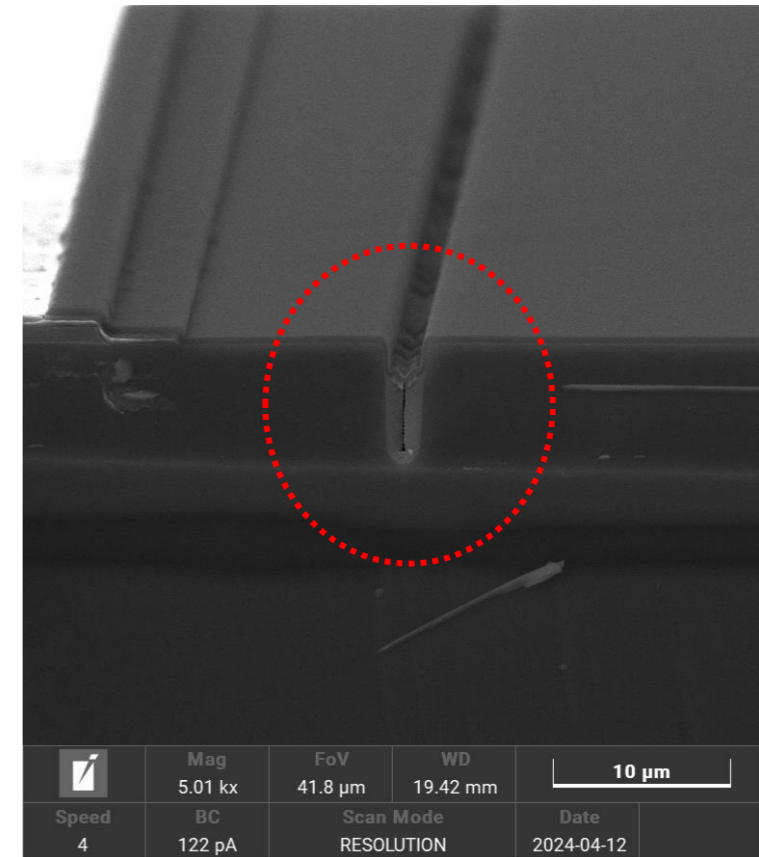
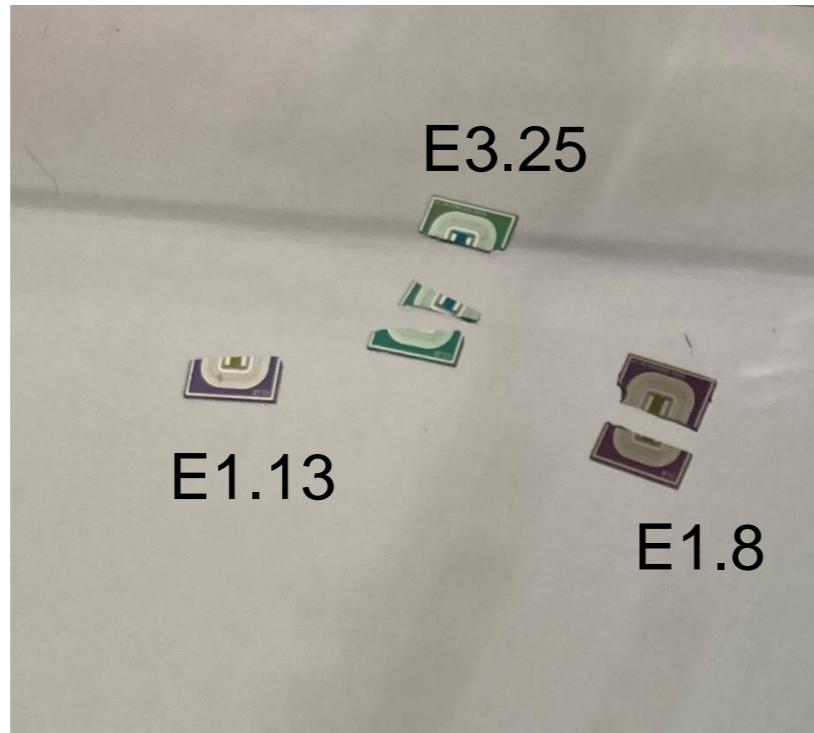
Discussion: Isolation

- There is still some charge collected from the pixel, when the laser is on adjacent pixel.
- Most probably due to the **cross-talk** between the pixels.
- Idea is to look inside the trenches



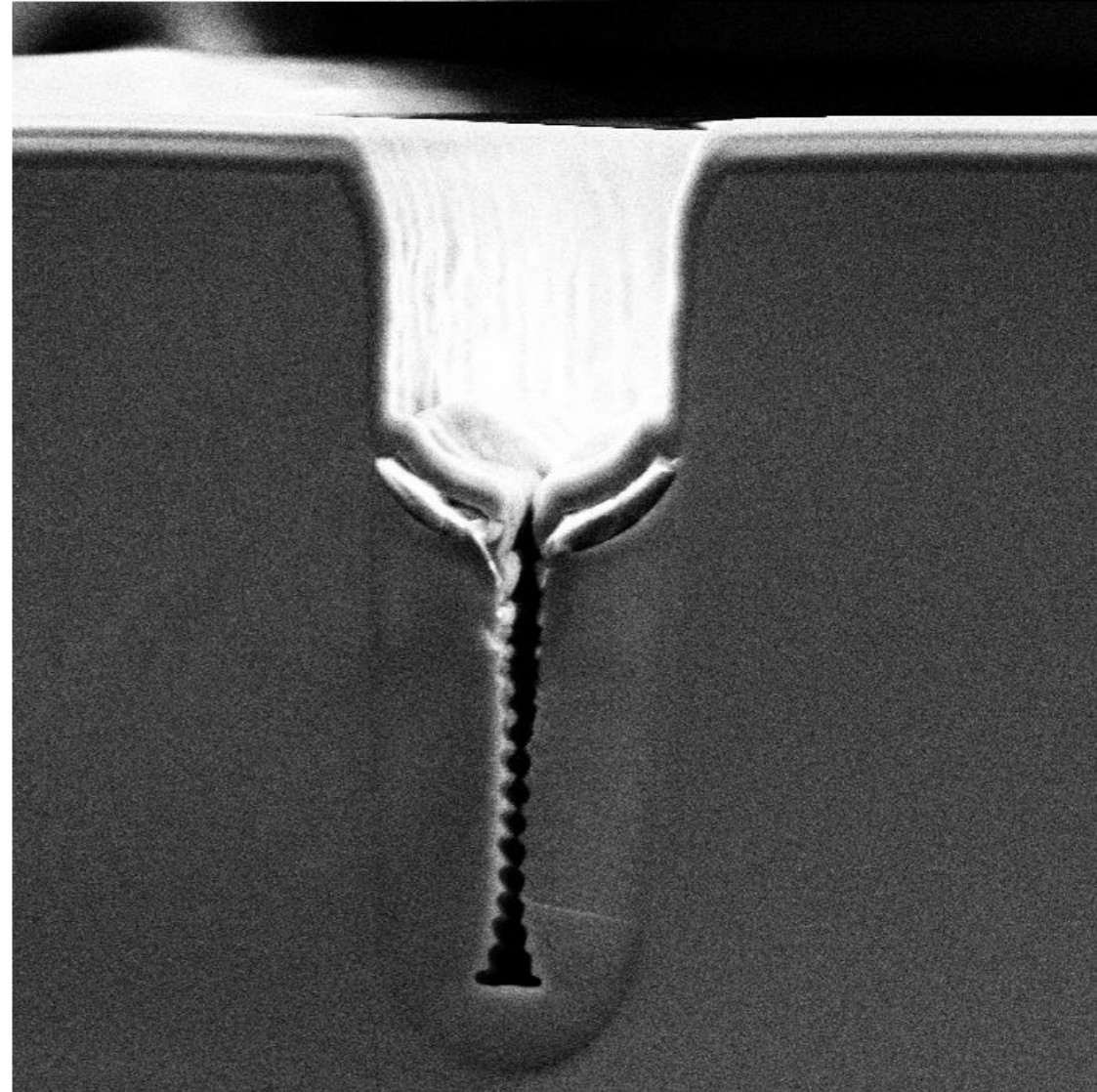
Discussion: SEM Images

- A couple of devices from a different part of the wafer were **cleaved** to investigate the trenches.



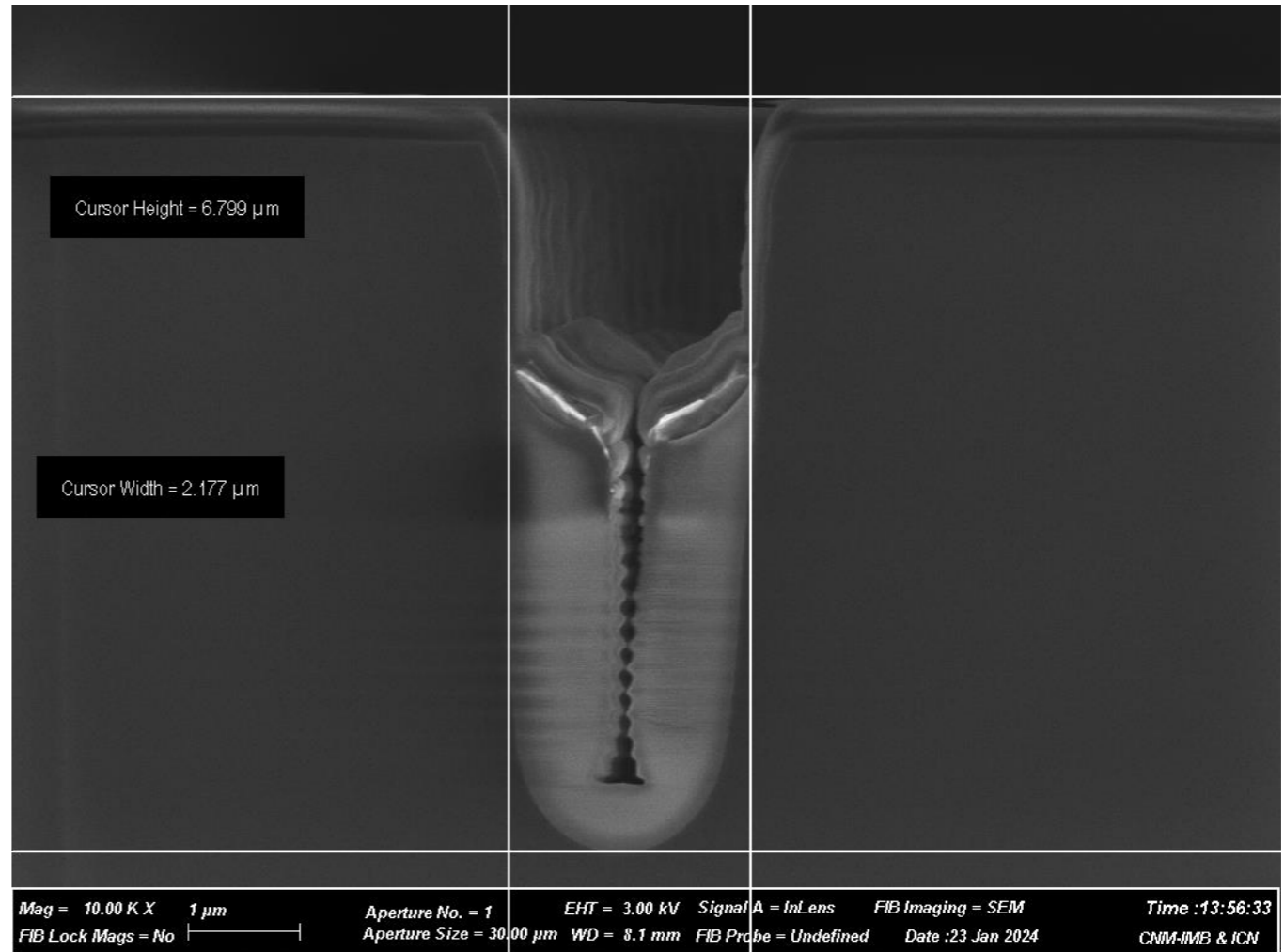
Discussion: SEM Images

Toast: to the Trench Isolated LGADs



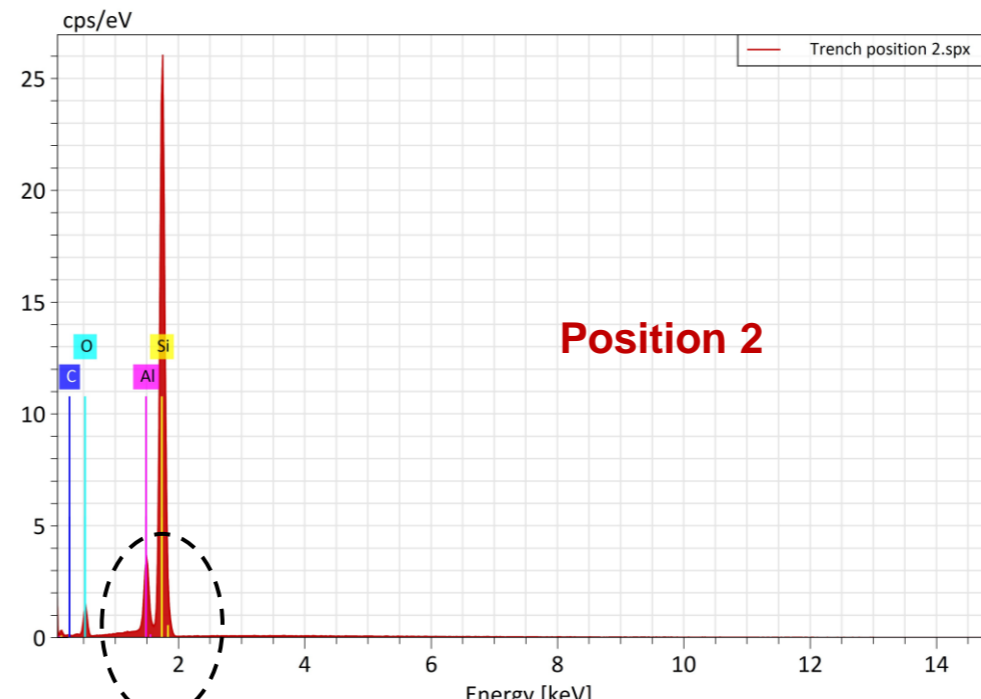
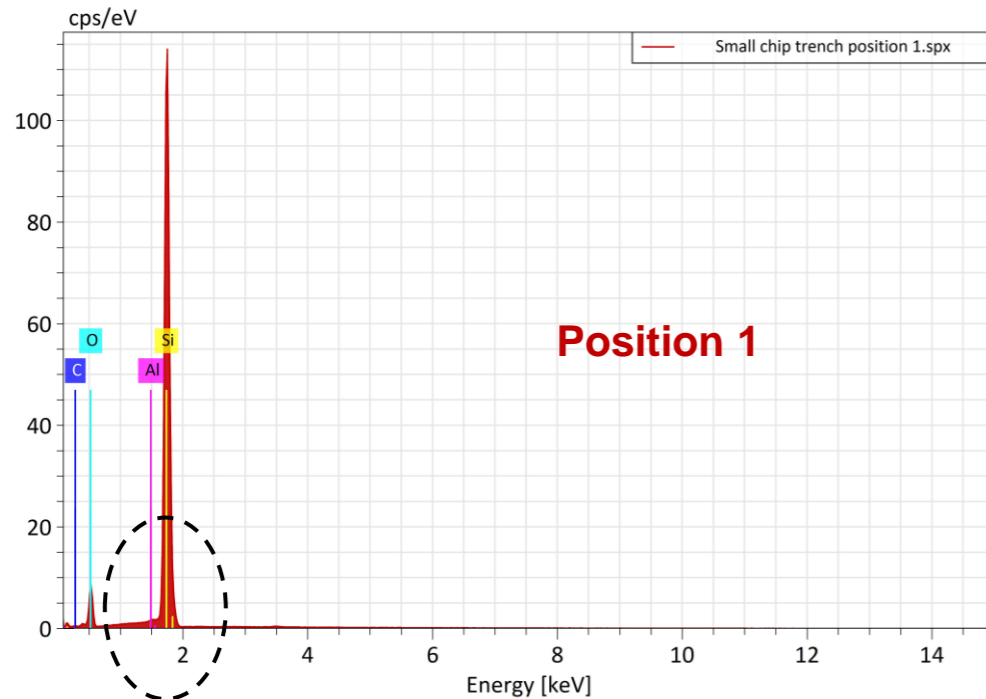
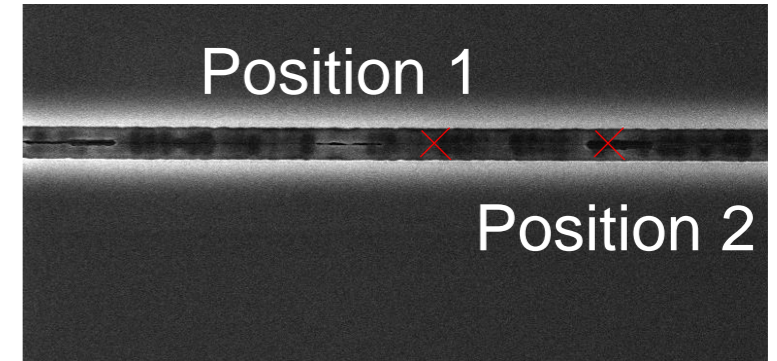
Discussion: SEM Images

- Trenches are $\sim 2\mu\text{m}$ wide and $\sim 7\mu\text{m}$ deep.
- Trench filling with SiO_2 is **not as expected**
- SiO_2 is **over-etched** during the wafer processing leaving a part of trenches empty.
- Additionally, some **metal debris** is observed in the trenches which seems to be a reason for the cross-talk.



Discussion: Energy Dispersive X-Ray (EDX) Spectra

- Confirmation of some **metal debris** in the trenches which seems to be a reason for the cross-talk.
- Aluminium peak was observed at position 2 but not in position 1.



**Measurements at
SMC, Edinburgh**

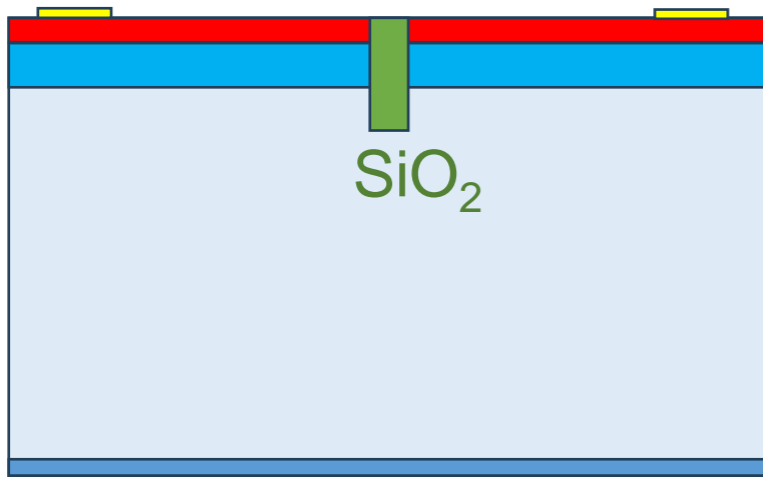
Discussion: Next Production

Gap = Distance between **trench** and **n-plus**

n-plus
Gain layer

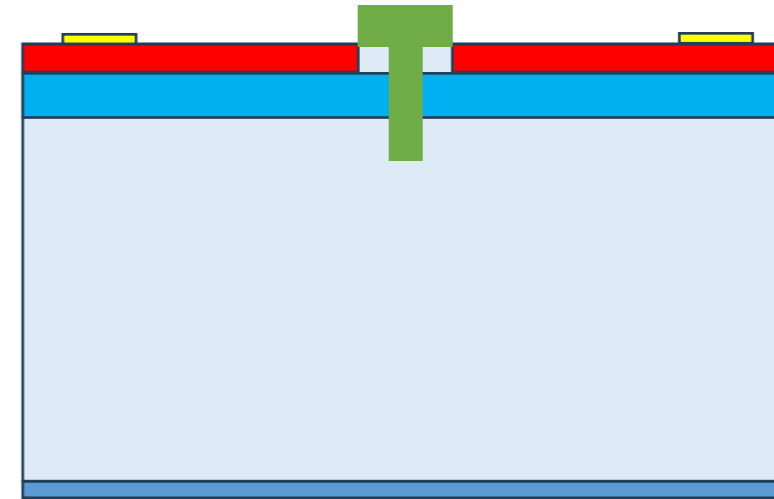
bulk

p-plus



Current Device Model

(uniform n+ implant)



New Device Model

(gap between trench and n-plus is introduced)

- To avoid over-etching of SiO_2
- Smooth trench filling

Summary and Future Work

- Preliminary results from new run of Trench-Isolated LGADs with low-gain have been presented
 - We are delighted to say that the **pixels are isolated**, but a **little cross-talk** is observed.
- Inter-pixel distance calculations shows values significantly smaller than the standard LGAD segmentation
 - **IPD < 7 μ m** at voltages above 180V
 - Fill factor is nearly **97%**
- Some issues were observed with the filling of trenches
 - **New run is in progress to avoid cross-talk \rightarrow better isolation**
- Next step is to characterise wafers with **higher gain**.
- Medipix arrays will be sent for under bump metal (UBM) \rightarrow **flip chipping to Timepix3 & Timepix4**
- **Irradiation campaign** to study the effects on pixel isolation and IPD.
- Next production on thin **epitaxial wafers (50 μ m)** for higher fill factor and improved timing resolution.

Acknowledgments

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