US-Japan project proposal : Capacitive Coupled Low Gain Avalanche Diode (AC-LGAD) detectors.

Koji Nakamura (KEK)

on behalf of US-Japan AC-LGAD collabration

History of US-Japan HEP program

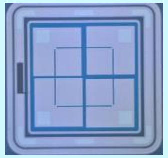
- The U.S.-Japan Cooperation Program in High Energy Physics program :
  - 2018 US-Japan Special funds : formed US-Japan collaboration for fast timing detector
  - Development of precision timing silicon detectors for future high energy collider experiments
    - 2019 Granted first US-Japan Cooperation Program (one year)
    - 2020 Granted continuous US-Japan Cooperation Program (one year)
    - 2021-2023 Granted another continuous US-Japan Cooperation Program (three years)
    - 2024- Partially granted extension of US-Japan Cooperation Program (One year approved.)
- Development of AC-LGAD detector project within this program
  - Started between KEK/Tsukuba -- Fermilab
  - Extended to BNL and UCSC starting 2020
  - **So far we made a great success of precision timing silicon detector "AC-LGAD" R&D**

US-Japan Collaboration

In 2019

Japan side development

AC-LGAD sensor development
(Hamamatsu Photonics K.K)
Spatial resolution
& radiation tolerance

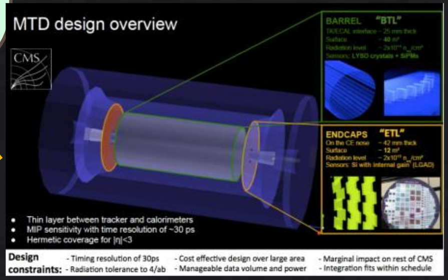


Fermilab Testbeam Facility

Testbeam

120GeV
Proton beam

CMS MTD



US-Japan Collaboration

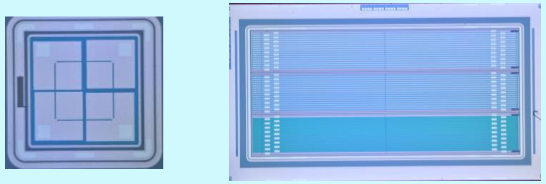
Now

Japan side development

AC-LGAD sensor development
(Hamamatsu Photonics K.K)
Spatial resolution
& radiation tolerance

KEK

筑波大学
University of Tsukuba

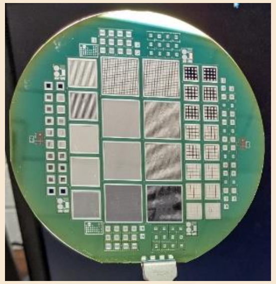


Comparison

Slightly Different approach
to achieve spatial resolution

BROOKHAVEN
NATIONAL LABORATORY

AC-LGAD sensor development
4 inch wafer fabrication
Fast feedback but
No mass production capability



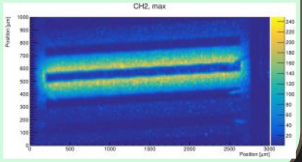
Fast ASIC development

High Speed Bi-CMOS ASIC
Designing for EIC detector

UNIVERSITY OF CALIFORNIA
SANTA CRUZ

Laser testing at LAB

Testing experience
Laser testing



Fermilab Testbeam Facility

Testbeam

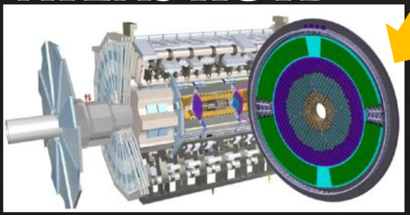
120GeV
Proton beam

Fermilab

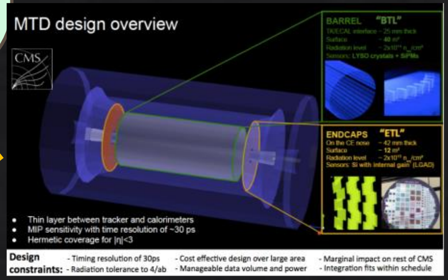
EIC ACLGAD

Illinois Univ.

ATLAS HGTD



CMS MTD



Operating and Planning Collider Experiment

World highest energy collider !

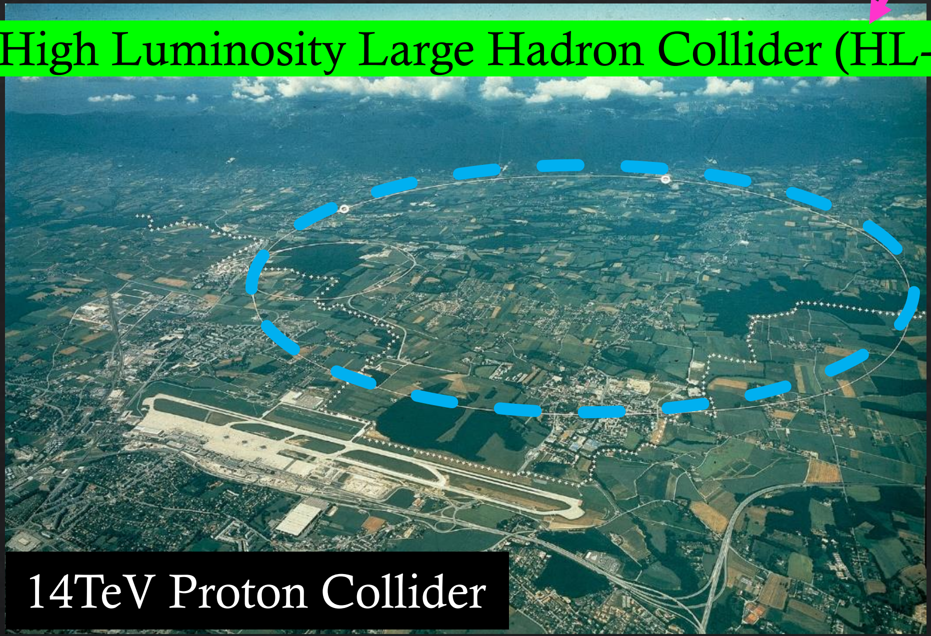
2011～ **Large Hadron Collider (LHC experiment)**

13.6TeV Proton collider

x10 Luminosity

Approved & constructing

2029～ High Luminosity Large Hadron Collider (HL-LHC)



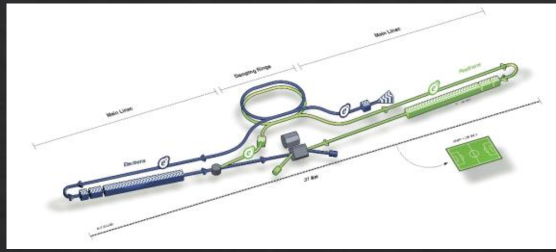
14TeV Proton Collider

Planning Experiment

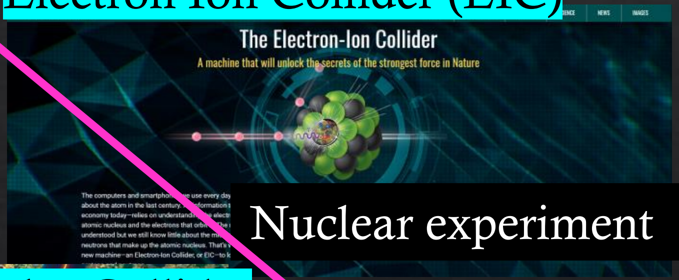
International Linear Collider (ILC)

Focusing on Higgs measurement (e+e-)

Preparing construction



Electron Ion Collider (EIC)



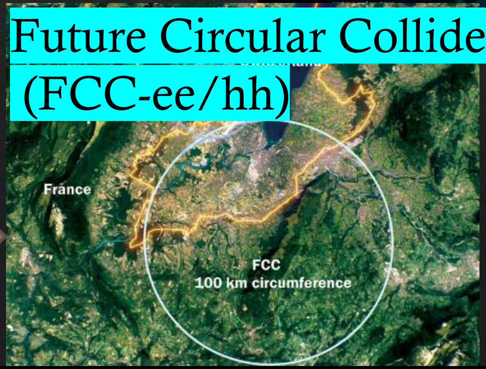
Nuclear experiment

High Energy LHC

Twice Energy

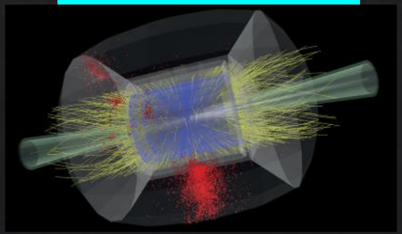
7 times Energy

Future Circular Collider (FCC-ee/hh)



100TeV Proton Collider

Muon Collider



Operating and Planning Collider Experiment

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2011～ **Large Hadron Collider (LHC experiment)**

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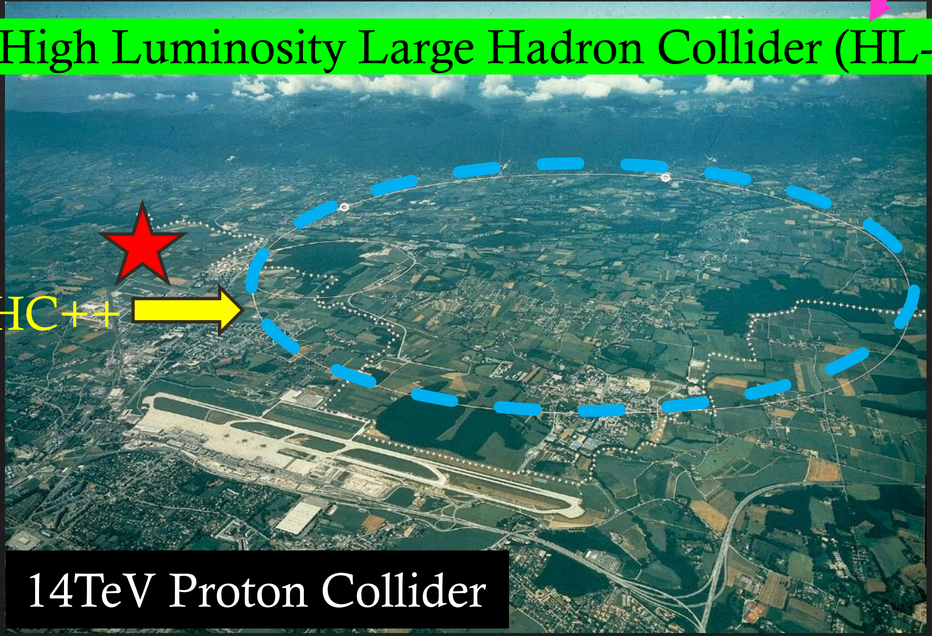
2029～

High Luminosity Large Hadron Collider (HL-LHC)



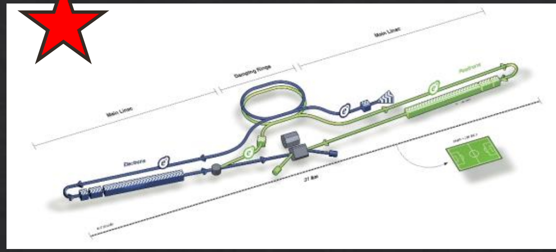
2034?
HL-LHC++

14TeV Proton Collider

Planning Experiment

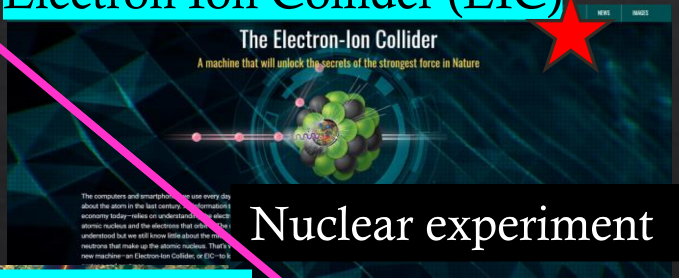
International Linear Collider (ILC)

Focusing on Higgs measurement (e+e-)



Preparing construction

Electron Ion Collider (EIC)

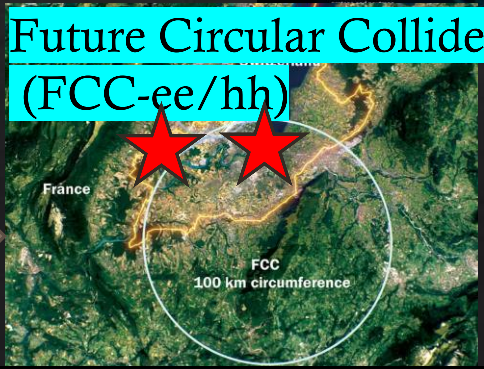


Nuclear experiment

High Energy LHC

Twice Energy

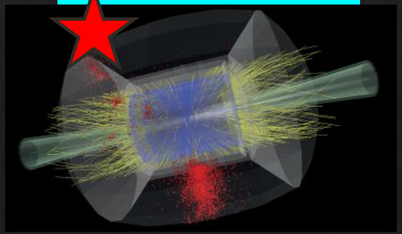
Future Circular Collider (FCC-ee/hh)



7 times Energy

100TeV Proton Collider

Muon Collider

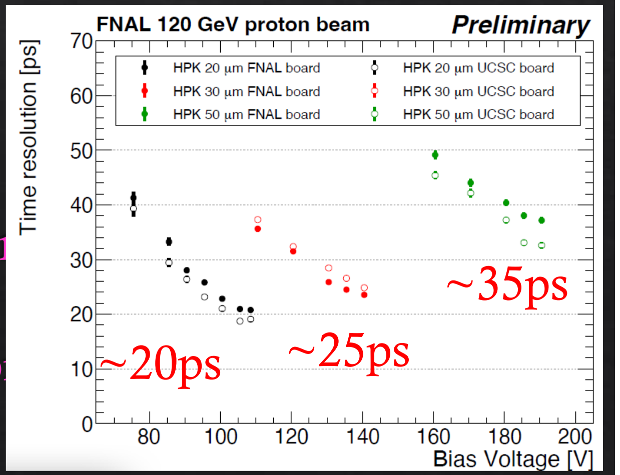


Timing Tracker is necessary for all of these colliders

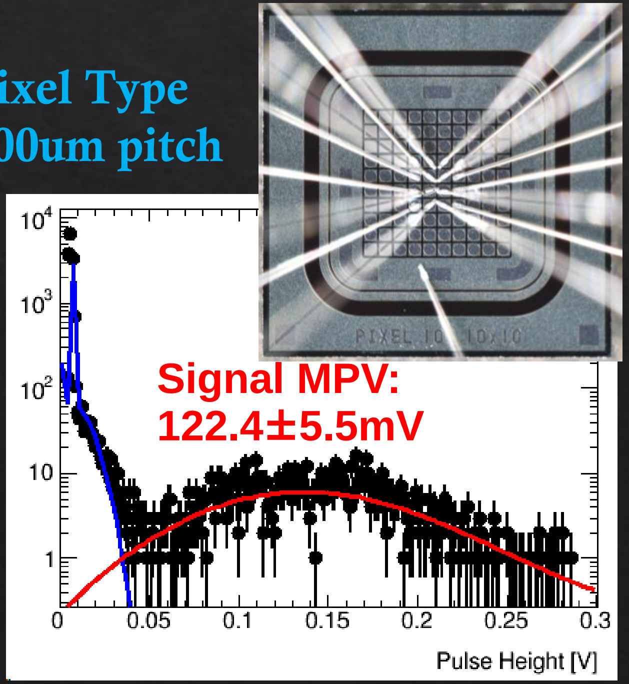
Development of AC-LGAD detectors

- Development of AC-LGAD detectors as high timing and special resolution.
- Detailed achievement so far was presented in :
  - https://indico.cern.ch/event/1402825/timetable/#93-development-of-precision-ti
- Timing resolution achieved 20ps for 20um thick AC-LGAD (by discrete amplifier board.)
- Spatial resolution : two way approach
  - 500um pitch sensor with charge sharing
  - 100um pitch pixelated sensors
- Radiation tolerance study
  - Understanding and demonstrated acceptance removal.
  - Not yet found fully solved method
- So far we have successfully developed AC-LGAD sensor by HPK and BNL
  - Planning to install to EIC TOF detector for first applicatio
  - Aiming other future collider (HL-LHC++, FCC-ee/hh)

Timing resolution
50/30/20um thick AC-LGAD



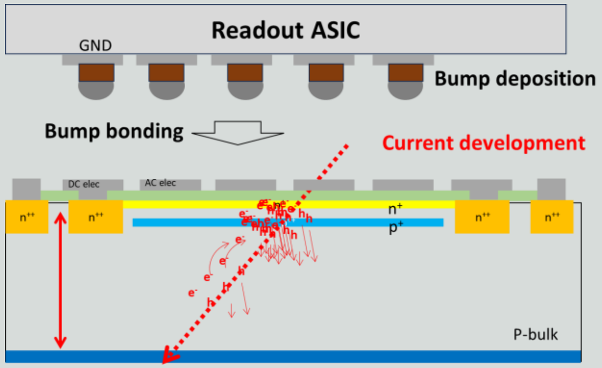
Pixel Type
100um pitch



LGAD development plan

- Goal : Detector with **10ps timing resolution and 10um spatial resolution**
  - **Sensor development to Module development (low noise readout ASIC)**
  - Hybrid type detector
    - Flip-chip sensor and ASIC → **Best performance** + radiation tolerance
  - Monolithic type detector
    - Sensor and readout is on the same wafer→**low material budget**+better spatial resolution(?)

3 type
New detector

<table>
<tr><th>Hybrid AC-LGAD</th><th>MAPS + gain layer</th><th>Monolithic AC-LGAD</th></tr>
<tr>
<td>
• Best performance (timing reso.)
• Radiation tolerance
• ASIC development only.


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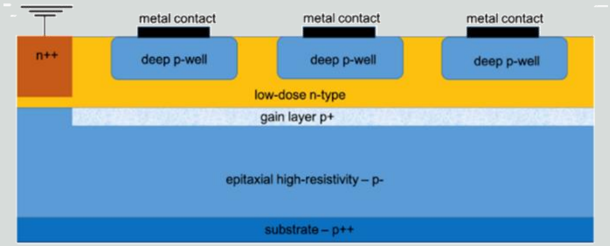
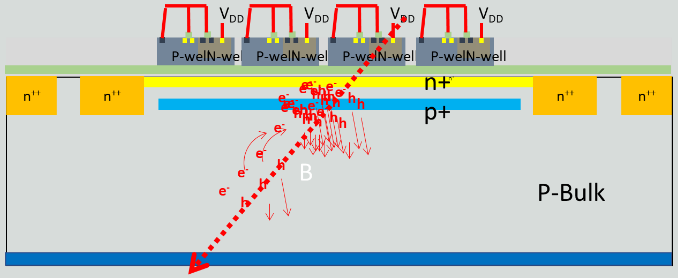
<td>
• Gain layer on existing MAPS detecotr
• Optimize gain in pre-amp?
• How to achieve uniformity?


</td>
<td>
• AC-LGAD on SOI wafer
• Collect charge from bulk of transistor.
• Expected good gain uniformity
• Completely new detector.


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Members

Japanese Collaboration Members			
No.	Name	Institution	Position
1	Koji Nakamura	KEK	Assistant Professor
2	Manabu Togawa	KEK	Associate Professor
3	Yuji Takeuchi	University of Tsukuba	Associate Professor
4	Masaya Miyahara	KEK	Associate Professor
5	Junya Nishino	University of Tsukuba	Master Graduate Student
6	Issei Horikoshi	University of Tsukuba	Master Graduate Student
7	Yuua Murayama	University of Tsukuba	Master Graduate Student
U.S. Collaboration Members			
No.	Name	Institution	Position
1	Artur Apresyan	FNAL	Scientist
2	Alessandro Tricol	BNL	Senior Scientist
3	Abraham Seiden	UCSC	Research Professor
4	Zhenyu Ye	LBNL	Scientist
5	Davide Braga	FNAL	Senior ASIC Engineer
6	Cristian Pena	FNAL	Associate Scientist
7	Si Xie	FNAL	Application Physist
8	Irene Dutta	FNAL	Research Associate
9	Chris Madrid	FNAL	Research Associate
10	Gabriele Giacomini	BNL	Scientist
11	Gabriele D’Amen	BNL	Staff Research Scientist
12	Hartmut Sadrozinski	UCSC	Research Professor
13	Bruce Schumm	UCSC	Professor
14	Jennifer Ott	UCSC	Postdoctoral scholar
15	Simone Mazza	UCSC	Research Scientist
16	Ryan Heller	LBNL	Applied Physicist Research Scientist

Plan for the development

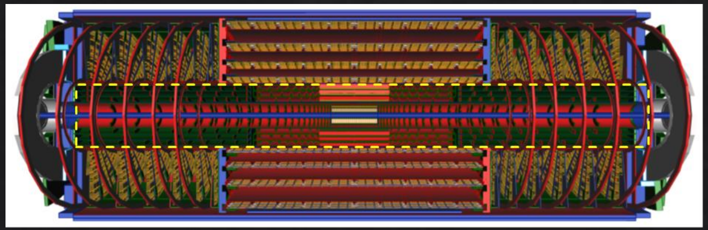
			Year 1				Year 2				Year 3			
	Task	Performed by	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
AC-LGAD Production #1	Design	BNL, KEK												
	Production	BNL, HPK		Run 1 Produced										
	Irradiation	BNL, KEK												
	Testing	FNAL, BNL, LBNL, UCSC, KEK				Run 1 Tested								
MAPS MPW Run	Design	FNAL												
	Production	FNAL				MPW Produced								
	Testing	FNAL, BNL, LBNL, UCSC, KEK						MPW Tested						
AC-LGAD Production #2	Design	BNL, KEK												
	Production	BNL, HPK					Run 2 Produced							
	Irradiation	BNL, KEK												
	Testing	FNAL, BNL, LBNL, UCSC, KEK							Run 2 Tested					
MAPS full wafer production	Design	FNAL												
	Production	FNAL								MAPS Produced				
	Testing	FNAL, BNL, LBNL, UCSC, KEK												Full Reticle MAPS Tested

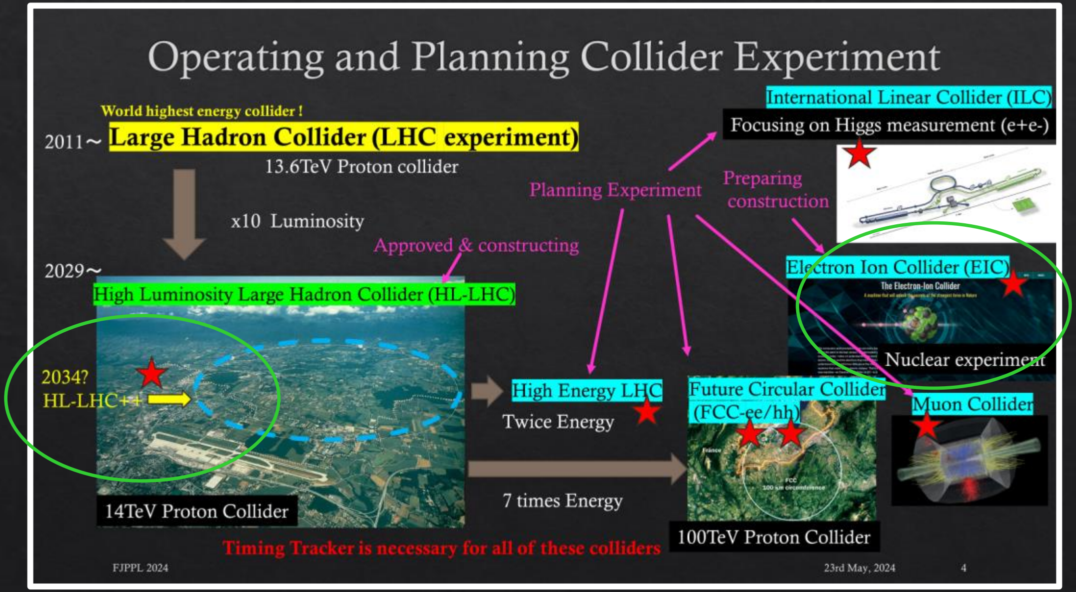
- Development of both Hybrid type and Monolithic type are in parallel.

Next install target?

- Closest and higher possibility upgrade is HL-LHC++
  - Should we need to target of this detector ?

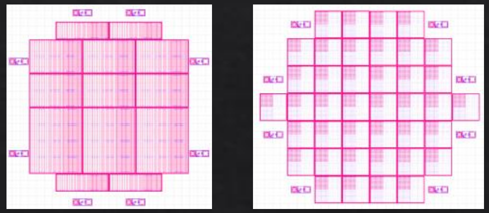
HL-LHC++:
- Need more development for radiation tolerance.
- Optimization of pixel size to maximize physics performance.
- ASIC for pixel type detector is really challenging.
- Monolithic AC-LGAD will be developed as ideal case.





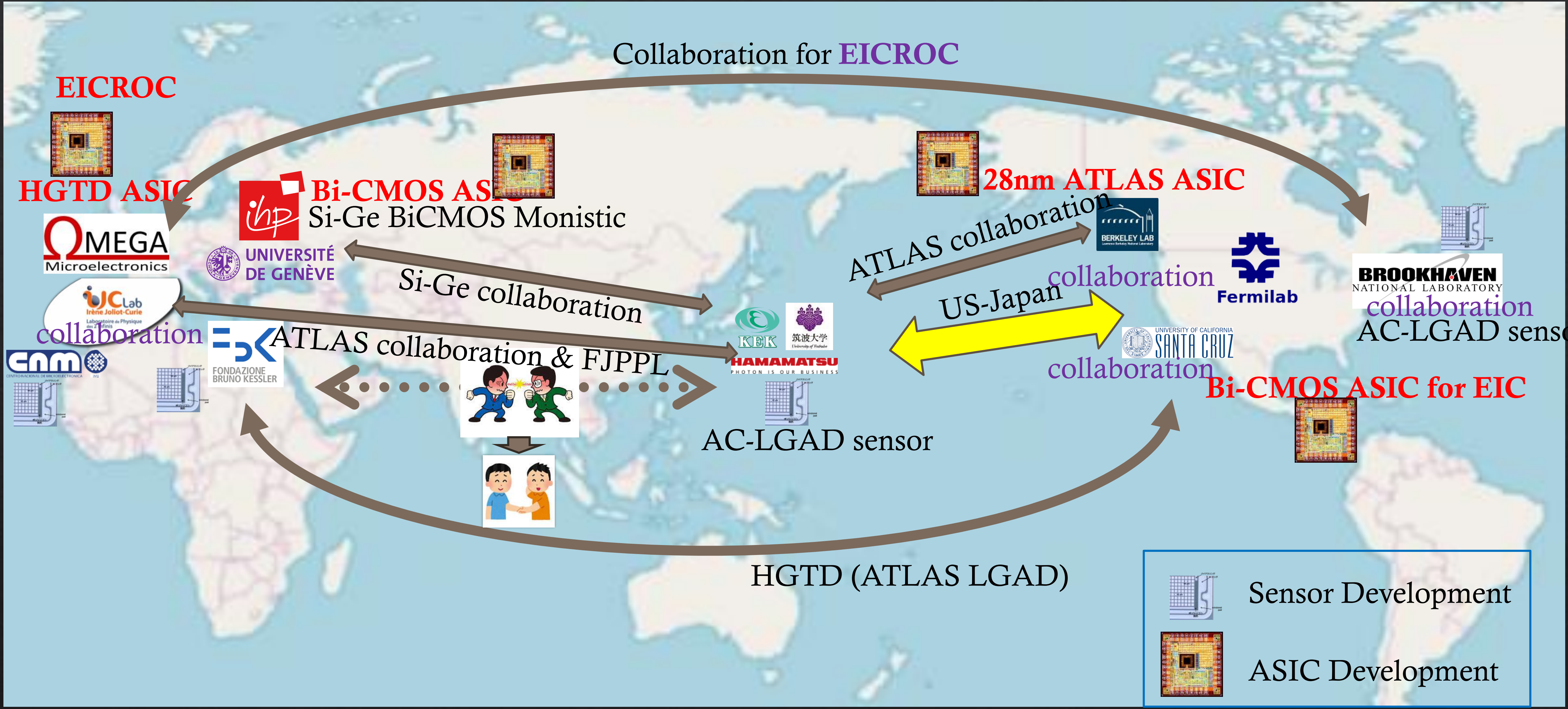
EIC:
- Providing AC-LGAD sensors (designed 500um pitch sensors and all parameters from us.)
- Not much development for sensor side necessary.
- OMEGA/IJClab are developing ASIC and readout

New submission :

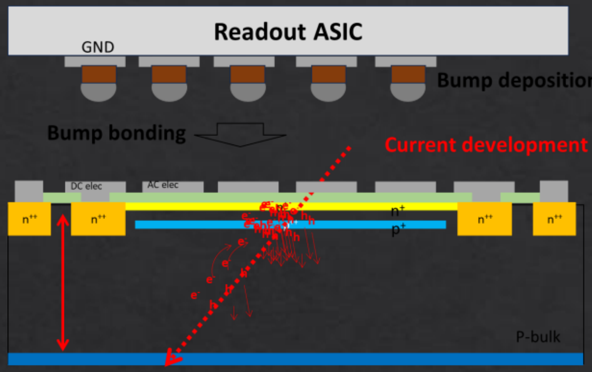


backup

AC-LGAD collaboration

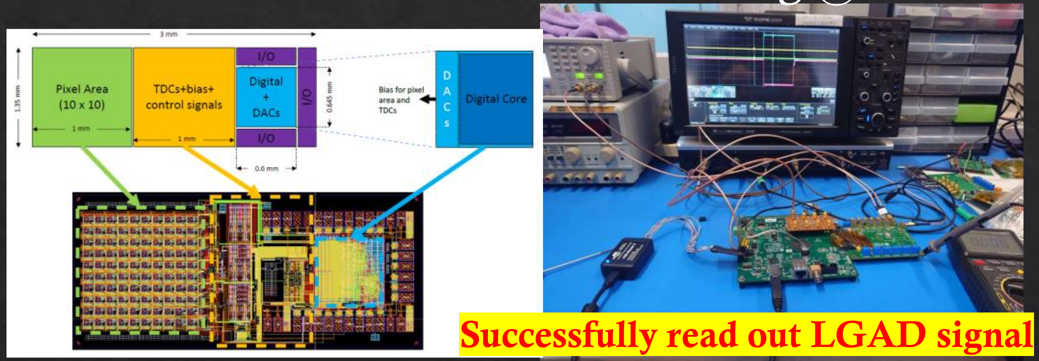


Hybrid type AC-LGAD

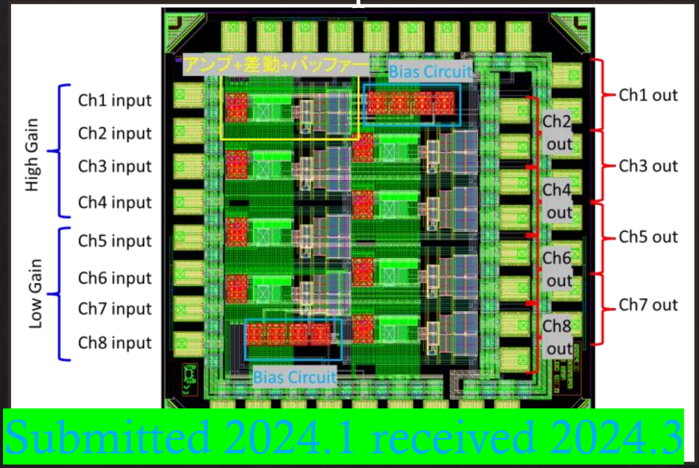


- Sensor development
  - Improvement of radiation tolerance→ just continue recent activity
  - Challenge to 10um thick detector (optimization of doping profile)
- ASIC development
  - Test with existing ASIC
    - Flip-chip to ITk ASIC (done.)
      - Itk ASIC have Precision ToT and ToA(1.5ns). Check uniformity.
      - Recently observed huge noise (600e) due to impedance between electrode.
    - Si-Ge ASIC(developed by Uni. Geneva)
      - IHP130nm process (originally for monolith project)
      - Existence of 100um pitch pixel sensor with 10 x 10 matrix
      - Available compatible sensor produced. (Flip-chip ongoing.) test by WB.
    - ATLAS/CMS/EIC developed ASIC for LGAD detector (PAD type)
  - Development of new ASIC
    - Pixel detector (low capacitance) ASIC
    - TSMC65nm process (Only Analog part submitted last JPY)
      - (First version is) Just for my education or trial.
      - Designed 6.2ps jitter for 10fC signal @Cdet=1pF
      - Discriminator (Constant Fraction) and TDC design will be next version.
    - Will collaborate with RD53-LBNL TSMC28nm process ASIC or TimeSpot ASIC

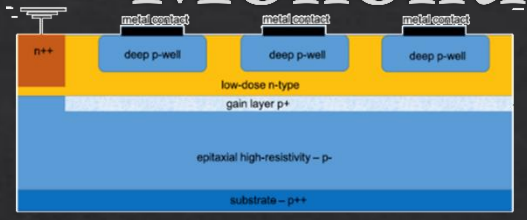
Si-Ge ASIC with AC-LGAD testing @KEK



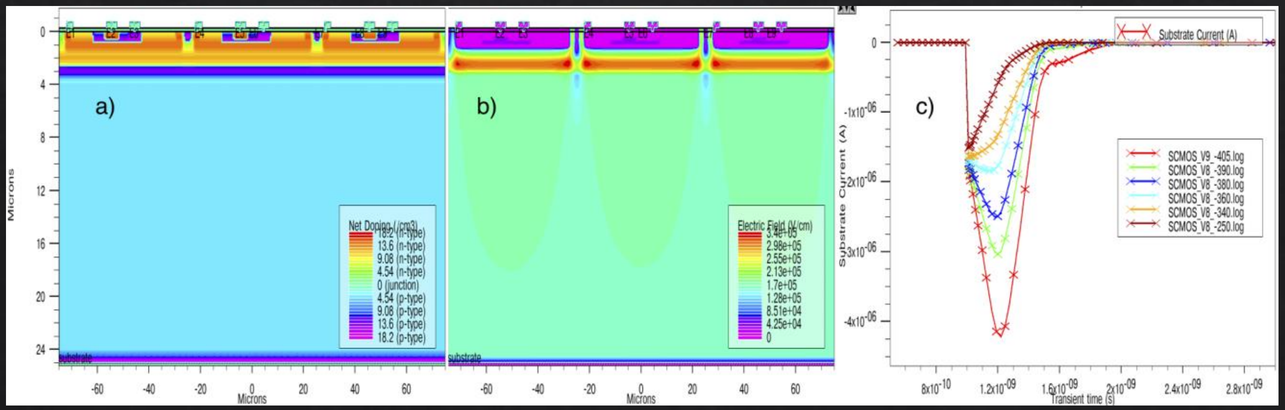
TSMC65nm process ASIC



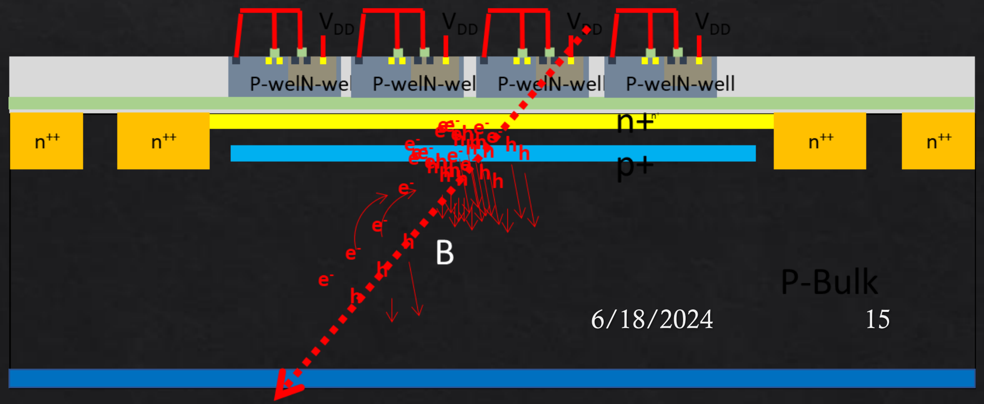
Monolithic LGAD



- MAPS + Gain
  - Belle and ITDC collaborate with TJ
  - US will make prototype with SkyWater (US)
  - Just started TCAD simulation
    - How to make good gain uniformity?
  - In the future, collaborate with (DRD3.1/7.6)

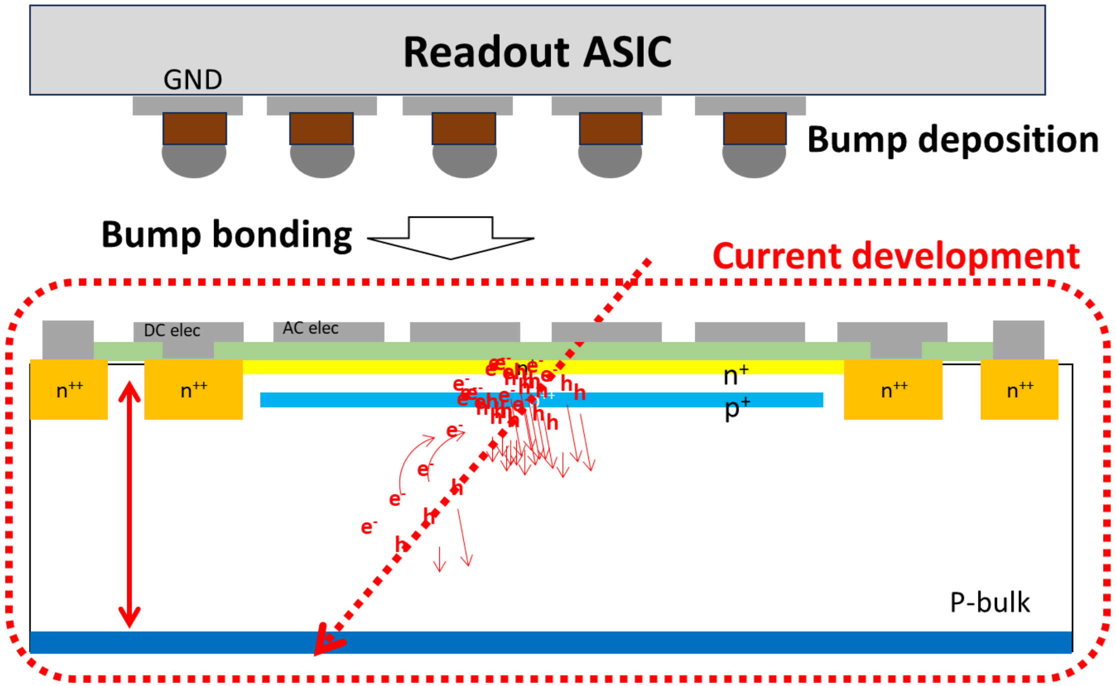


- SOI AC-LGAD
  - Middle to longer time scale
  - JPY 2024
    - TCAD simulation with input transistor and optimize the detector design.
    - Find vendor (XFAB, LAPIS, Tower, HPK)
  - 3 years term plan：
    - Minimal goal is to have Analog(Pre-Amp) readout detector and proof of consept.
    - Non-Pre-amp part of ASIC can be used hybrid type ASIC architecture.

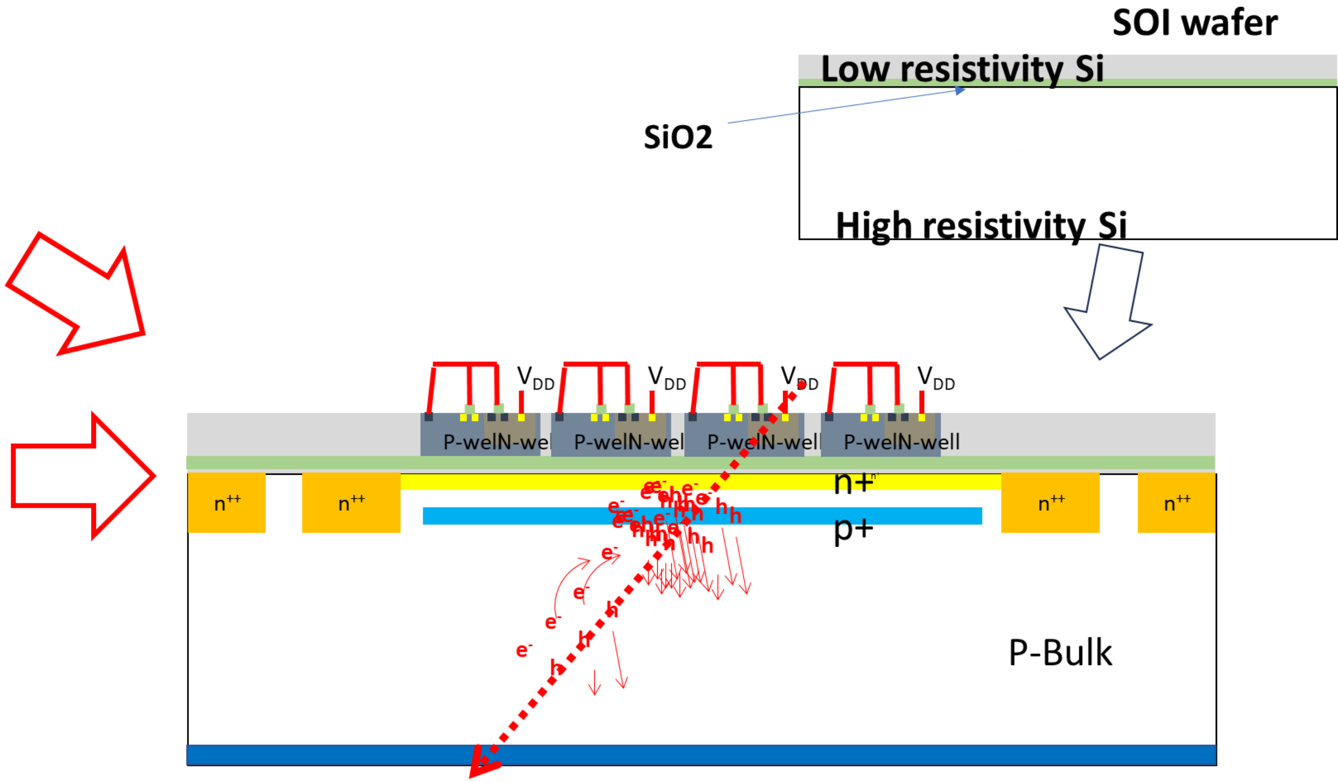


Idea for monolithic AC-LGAD detector

Hybrid Type AC-LGAD detector



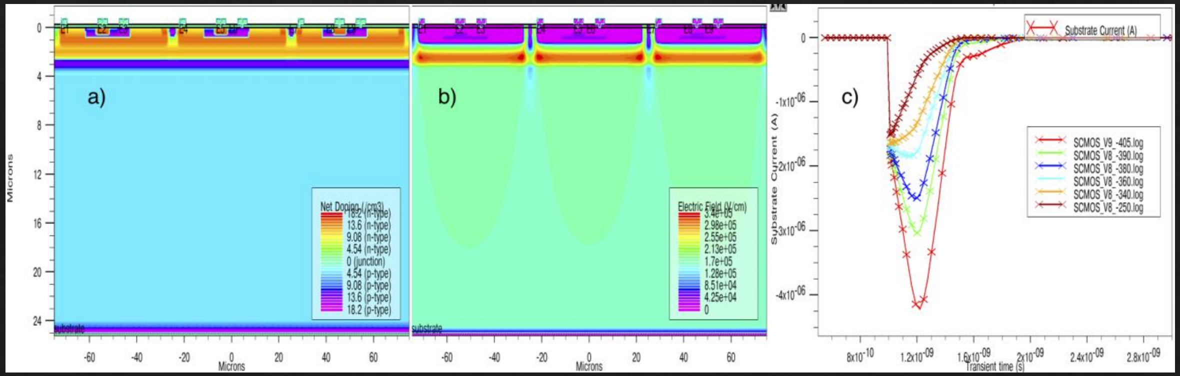
Monolithic type AC-LGAD detector



Why LGAD in the view of ASIC development?

- Recent trend of HEP R&D might be Low noise ASIC (TimeSPOT , Monolith, TSMC 28nm)
  - Probably because LGAD have issue of spatial resolution and radiation tolerance
    - We are fighting with these issue and solved spatial resolution issue already (100um x100um pixel available)
- Low noise ASIC should of cause have benefit for LGAD
  - LGAD＋Low noise ASIC should be perfect detector.
- Idea of using LGAD for reduction of power consumption
  - Only LGAD has internal gain (large signal with excellent S/N ratio)
  - Most of MAPS development teams think about placing gain layer. (Monolith also tried PicoAd)

- Future development should think about this situation.
  - Personal view :
    - 10-20ps fully uniform timing resolution.
    - 5e15neq/cm2 radiation tolerance.
    - (if possible) the device should be monolithic.



Two approach

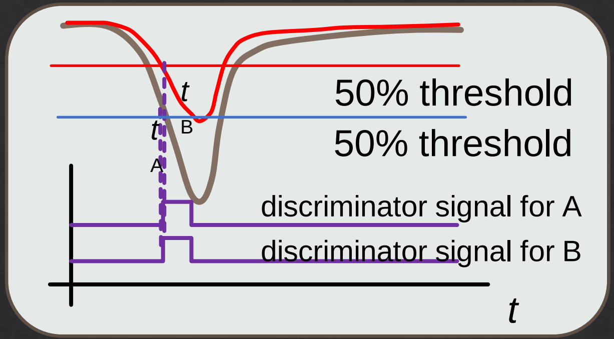
- ***<u>Readout ASIC (amplifier) with smaller noise</u>***
  - 3D detector with CMOS ASIC
    - Time Spot
    - RD53 ASIC (28nm)
  - Monolithic detector with Si-Ge BiCMOS
    - Monolith (Univ. of Geneva) by IHP
- ***<u>Making sensor with larger signal and faster turn on</u>***
  - **Low Gain Avalanche Diode (LGAD)**

$$\sigma_j = \frac{\sigma_n}{\left|\frac{dV}{dt}\right|} = \frac{\sigma_n}{\left|\frac{S}{t_r}\right|} = \frac{t_r}{\left|\frac{S}{\sigma_n}\right|}$$

- σ_n: Size of noise
- $\frac{dV}{dt}$: Slope of vol.
- S: Size of signal
- t_r: Ramping time

These two approaches may realize at the same time.

Readout Electronics



- Various ASIC developed for ATLAS/CMS/EIC detector (i.e. ALTIROC/ETROC/EICROC)
- Low noise pre-amplifier and Comparator with time walk correction is important for timing resolution.
  - Still signal size based time walk correction is popular method
  - Recently Constant Fraction Discriminator is implemented to the ASIC by Fermilab group.