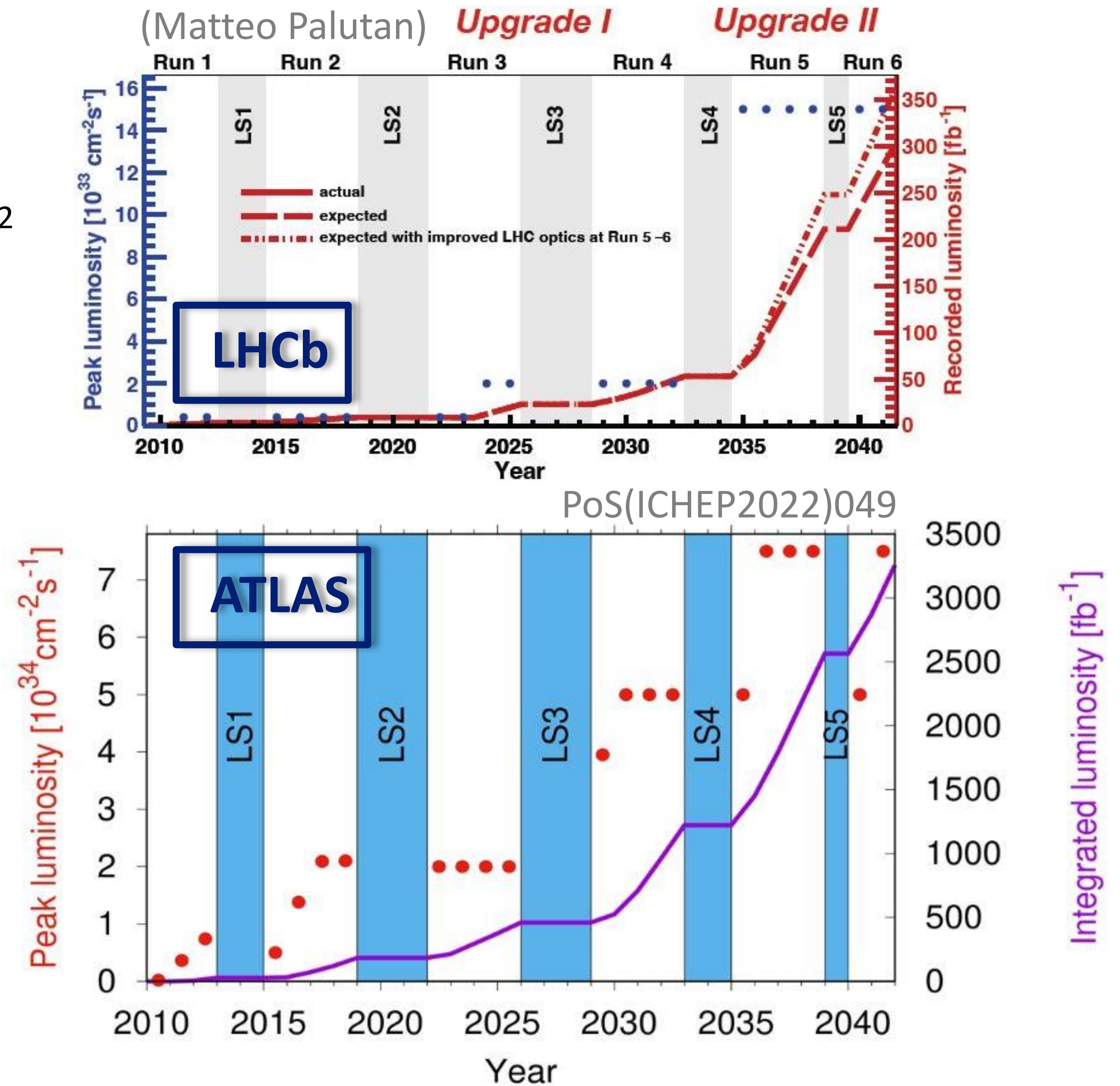
Thin monolithic High Voltage CMOS sensors with excellent radiation tolerance

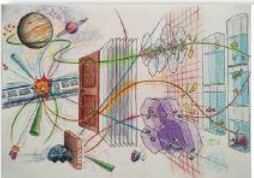
University of Liverpool – Jan Hammerich, Sam Powell, Eva Vilella, Ben Wade, Chenfan Zhang, Carleton University – Thomas Koffas, HEPHY – Thomas Bergauer, Christian Irmler, IFIC – Ricardo Marco-Hernández, JSI – Igor Mandic, NIKHEF – Uwe Kraemer, Jory Sonneveld, University of Bern – Silke Moebius, University of Sevilla – Rogelio Palomo

Preliminary

Motivation

- **High radiation levels**
  - High Luminosity LHC → > 10^{16} n_{eq}/cm^2
  - FCC-hh → > 10^{17} n_{eq}/cm^2
- **New detector technologies**
  - New detector technologies that need to be strategically developed and optimised for practical use





DRD3 WG1 Monolithic silicon sensors DRD3

Aim is to advance the performance of monolithic CMOS sensors for future tracking applications, tackling the challenges of

- very high spatial resolution;
- excellent timing resolution;
- high data rate;
- high radiation tolerance;
- low mass;
- covering large areas;
- reducing power;
- keeping an affordable cost;
- and ultimately combining these requirements in one single sensor device.

This proposal

WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤3 µm position resolution
RG 2.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad
RG 1.5	Low-cost large-area CMOS sensors

ECFA European Committee for Future Accelerators

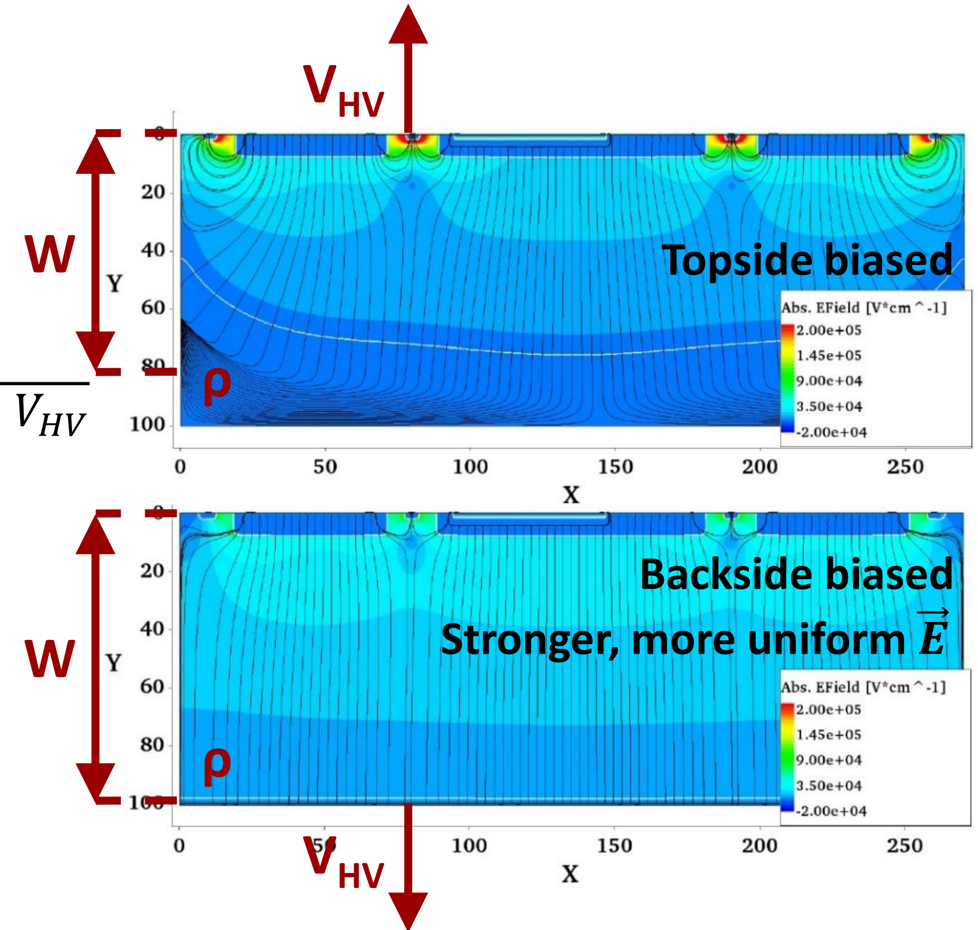
DRD3 WG1/WP1 kick-off meeting, 21st May 2024 1

Recipe for high radiation tolerance

- **Large substrate biasing voltage (V_{HV})**
  - Larger depletion region → larger signal
  - Faster charge collection
- **High resistivity silicon bulk (ρ)**

➔ $W \propto \sqrt{\rho \cdot V_{HV}}$

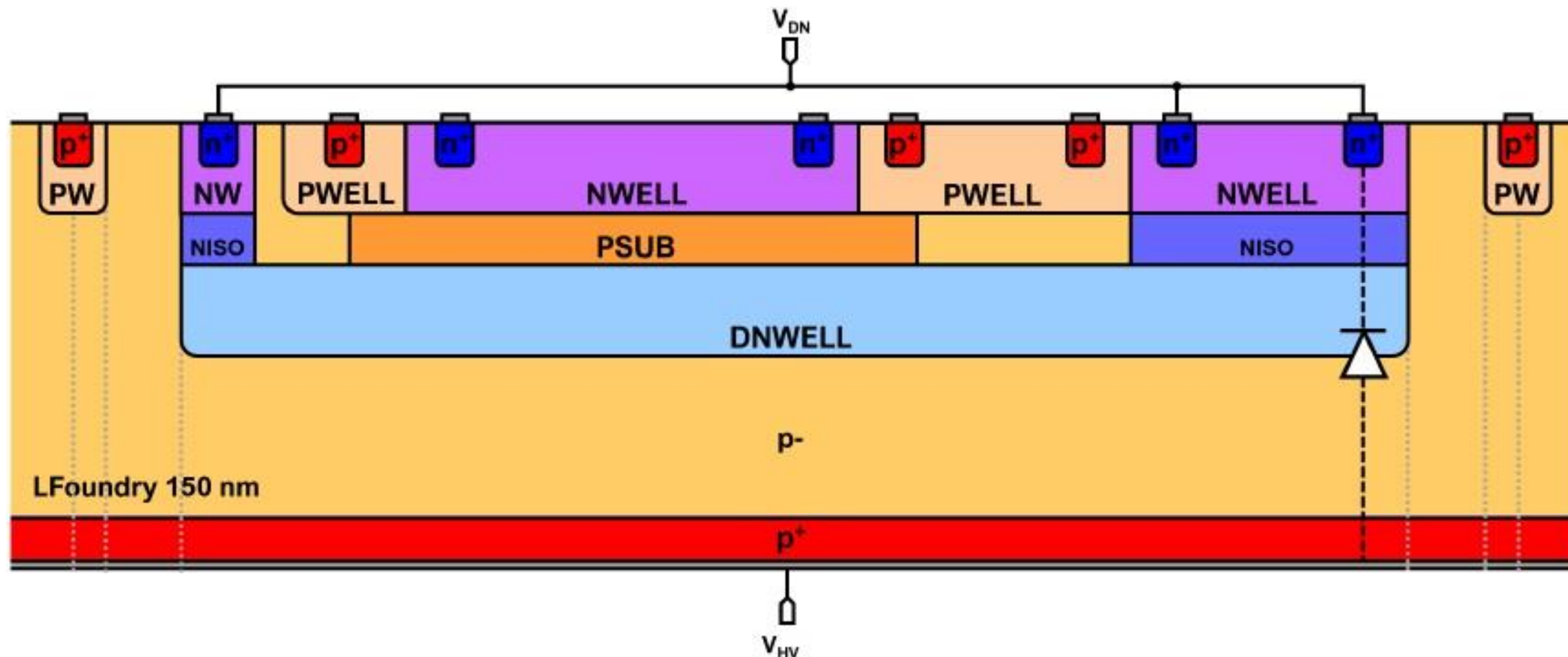
- **Substrate backside-biasing**
  - More uniform electric field lines
  - Improved charge collection efficiency
- **Sensor thinning**
  - Improved charge collection efficiency
- **Multiple nested wells**
  - In-pixel low-voltage CMOS readout electronics
  - Isolated from substrate biasing
- **Suitable technology design rules**
  - E.g. circular transistors



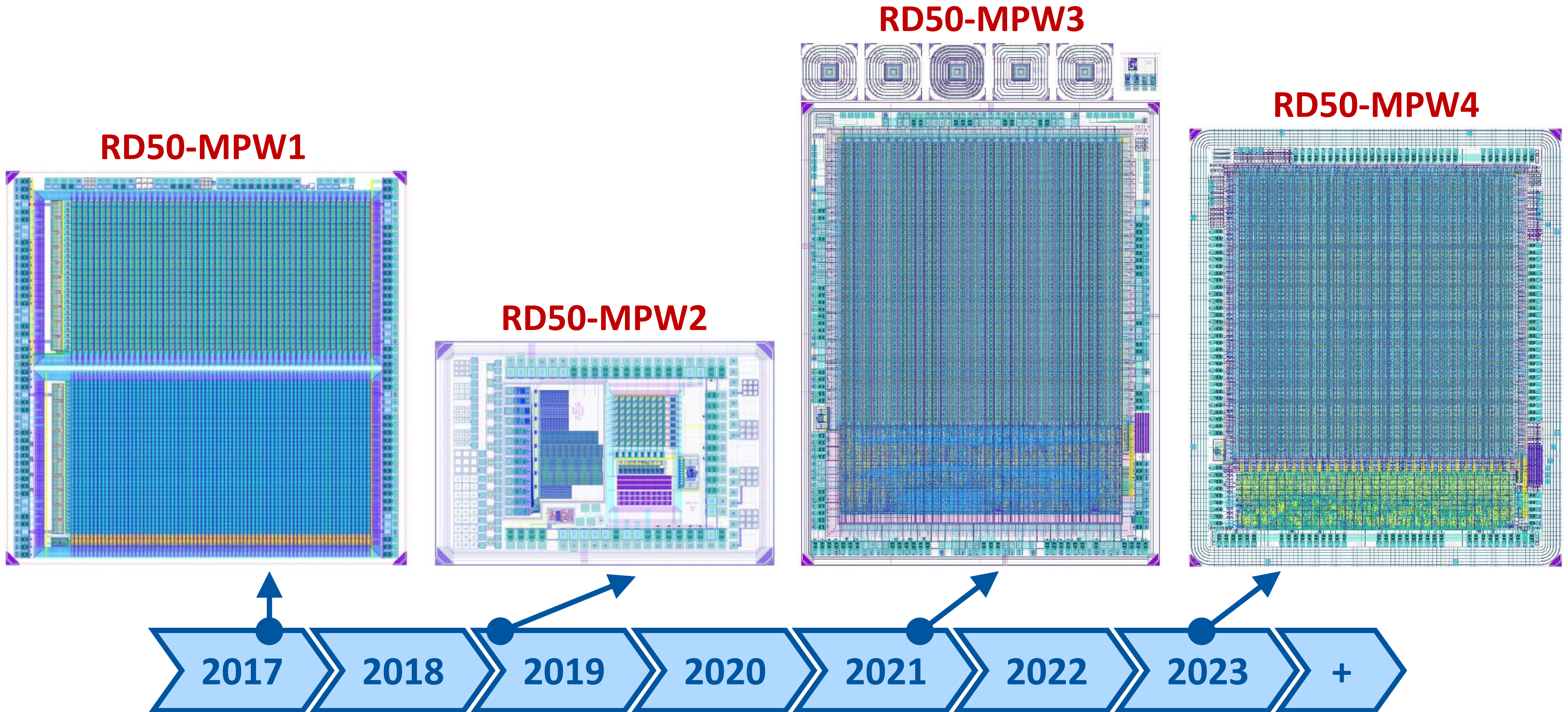
Electric field – TCAD simulated
H35DEMO (0.35 µm HV-CMOS ams)
1 kΩ·cm
100 µm
120 V Meng CERN-THESIS-2018-153

Technology process

- **150 nm High Voltage CMOS LFoundry (LF15A)**
  - P-substrate/DNWELL sensing junction (large collection electrode)
  - Pixel readout electronics embedded inside DNWELL
  - CMOS electronics in sensing diode & isolated from DNWELL with PSUB
  - Access to high resistivity substrates, thinning and backside biasing (complex wafer loan)

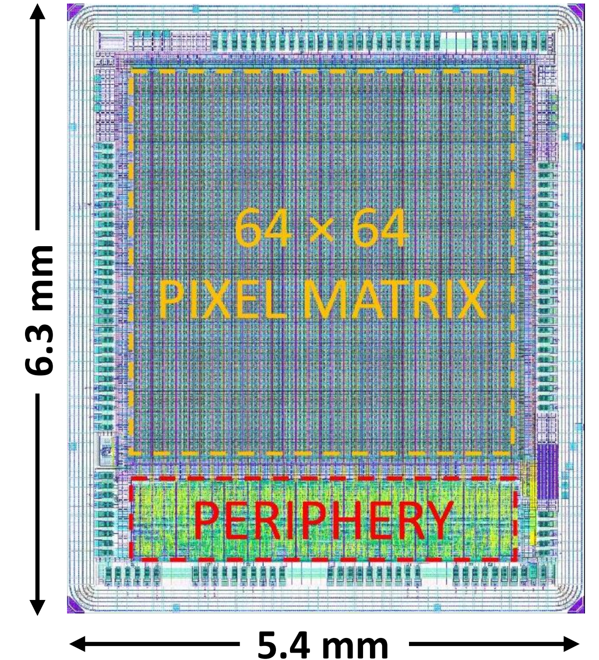


RD50-MPW chip series



RD50-MPW4

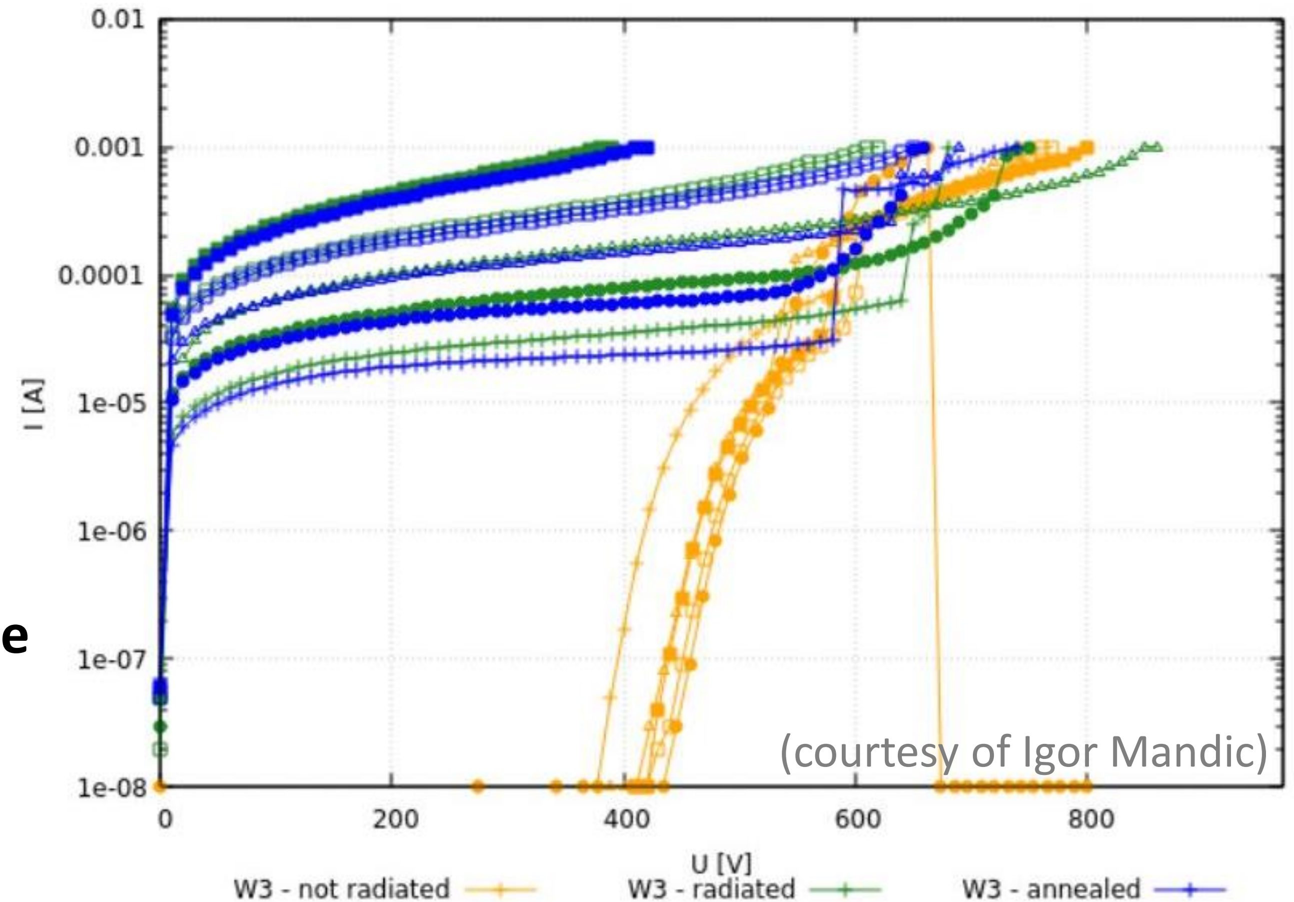
- **Significant improvements**
  - For high breakdown voltage and high radiation tolerance
  - Multiple ring structure around the chip edge
  - Substrate backside-biasing to high voltage
- **Fabrication details**
  - 150 nm High Voltage CMOS LFoundry (LF15A)
  - P-type substrate with nominal 3 kΩ·cm high resistivity
  - 280 µm thin
  - Backside processed via third party (complex wafer loan)
- **Chip contents**
  - Pixel matrix with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixels with large collection electrode
  - Digital periphery (slow control, hit data transmission)
  - Tests structures (e-TCT, DLTS)



Chip delivered in Q1 2024
Evaluation is going very well
See Bernhard Pilsl's presentation for details

There is always a but…

- **RD50-MPW4**
  - The chip works very well
  - It is a very nice technology
  - We are taking right steps to demonstrate very high radiation tolerance
- **Things can be further developed to tackle the challenges of**
  - Timing resolution
  - Power consumption
  - Chip fill-factor
  - While maintaining if not further improving the radiation tolerance



- **Experimental conditions**
  - Current measured at about 10 °C
  - Chips irradiated to 1e14, 3e14, 1e15, 3e15 and 1e16 n_{eq}/cm^2
  - Current measured after irradiation and annealing for 80 min at 60 °C

This proposal – Boosting the technology parameters

Parameter	Current value	Research goals
Spatial resolution	62 µm x 62 µm (pixel size)	62 µm x 62 µm (pixel size)
Timing resolution	10 ns (time-walk)	2 ns (time-walk)
Radiation tolerance	Several 10^{15} n_{eq}/cm^2, maybe 10^{16} n_{eq}/cm^2 (currently under test)	> 10^{16} n_{eq}/cm^2
Power consumption	Several 100 mW/cm^2 (currently under test)	A few 100 mW/cm^2
Fill-factor	Area hungry digital periphery Area hungry multiring structure	Reduced area digital periphery Reduced area ring structure

This proposal – Tasks

Tasks	Description
1	Technology simulation
2	Chip design and submission
3	Development of the specific DAQ with Caribou (e.g chip carrier board, firmware, software, integration with test beam instrumentation…)
4	Irradiation to high fluence and high dose
5	Evaluation of the fabricated prototypes in the laboratory (e.g. I-Vs, pixel gain and noise, timing response, sensitivity to radioactive sources…)
6	Evaluation in test beams

We are open to new collaborators who are interested in participating in this project

This proposal – Implementation plan

- **One small area chip**
  - To try a few different strategies to achieve our research goals
- **One larger area chip**
  - Going large is always a challenge

Detector community dedicated LF15A submissions

- **What is in the deal with LFoundry?**
  - Detector community joint submission(s) with several chips in the reticle
  - Price advantageous
  - Easy access to backside processing (potentially in-house at LFoundry)
  - Access to high resistivity wafers
  - Large number of fabricated wafers, so many samples for chip evaluation
  - Multi-layer mask type submission (MLM 1x3, maximum area is ~ 9 mm x 25 mm)
  - Including 6 metal layers and transistors
- **Challenges**
  - No invoice split! Invoice payment via one single customer
  - To do a joint submission in 2025, LFoundry needs to be informed by September 2024
  - All chips in the reticle need to have compatible specifications (e.g. passivation layers)
  - Need to identify a supplier for dicing and perhaps for backside processing (no problemo)
  - Need an agreement regarding IP protection between submitting institutes (no problemo)