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Thin monolithic High Voltage CMOS sensors with excellent radiation tolerance

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State-of-the-art silicon tracking detectors, used in the current generation of physics experiments such as the Large Hadron Collider (LHC) at CERN, are not able to meet in a single sensing device the challenging specifications anticipated by future experiments. These specifications include high radiation tolerance and low-mass, along with fast timing, high spatial resolution and low-power consumption. This contribution will present a new project proposal to tackle the strategic research goal of thin monolithic detectors with excellent radiation tolerance (200 μm, >10^{16} $\mathrm{n_{eq}/cm^2}$) for tracking charged particles in future physics experiments, such as the High Luminosity LHC major upgrades and beyond Phase II replacements initially. It will build on existing expertise in High Voltage CMOS sensor technology, the most promising route for achieving this goal.

The proposal will use the RD50-MPW prototypes, which are High Voltage CMOS pixel chips in the 150 nm technology from LFoundry S.r.l., as a starting point. RD50-MPW4, the latest prototype within this programme, implements significant improvements for a high breakdown voltage, and therefore an excellent radiation tolerance, through a multiple ring structure around the chip edge and substrate backside-biasing to high voltage. The chip was fabricated on a p-type substrate with a nominal 3 kΩ·cm high resistivity, thinned to 280 μm and backside processed. It is composed of a 64 rows × 64 columns matrix of 62 μm x 62 μm pixels with large collection electrode, and a digital periphery for slow control configuration and hit data transmission. The DAQ of the chip is based on the Caribou readout system. Non-irradiated RD50-MPW4 samples have been successfully evaluated in the laboratory and at a recent test beam at DESY. Samples have been irradiated with neutrons up to 3 x 10^{16} $\mathrm{n_{eq}/cm^2}$ and the evaluation of these irradiated samples is currently ongoing. Preliminary current-to-voltage measurements show a >400 V breakdown voltage before irradiation, and a close to 800 V breakdown voltage after irradiation. However, the multiple ring structure around the chip edge occupies a significant non-sensitive area. The timing resolution of the pixel matrix is too slow, the size of the digital periphery too large and the power consumption of both the pixel matrix and digital periphery too high. This proposal will boost the pixel chip parameters, especially tackling the challenges of fast timing resolution (2 ns goal), low-power consumption (a few 100 $\mathrm{mW/cm^2}$ goal) and increased fill-factor (>90% goal), while maintaining if not improving the radiation tolerance of this technology (>10^{16} $\mathrm{n_{eq}/cm^2}$ goal). The proposal comprises chip design and simulation, chip submission, development of the specific DAQ, and evaluation of the fabricated prototypes in the laboratory and at test beams before and after irradiation to high fluence and ionising dose. We are open to new collaborators who are interested in participating in this project.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (scientific results or project proposal)

project proposal for future work

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