Large area low-power Monolithic CMOS Tracking Detectors for future particle physics experiments

DRD3 Week

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For the ATLASPIX3 Silicon Tracker community

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

DRD3 WP1 Project proposal

- **Proponent teams**
  - Karlsruhe Institute of Technology (KIT) (*), Hochschule RheinMain, INFN Milano, INFN Pisa (*), University of Edinburgh, Lancaster University, Queen Mary University of London, STFC RAL PPD, STFC Daresbury, IHEP (*)yet to be confirmed

  Groups involved in many HEP experiments and upgrades (ITk, ALICE, EIC, Belle II, LHCb Mighty Tracker)

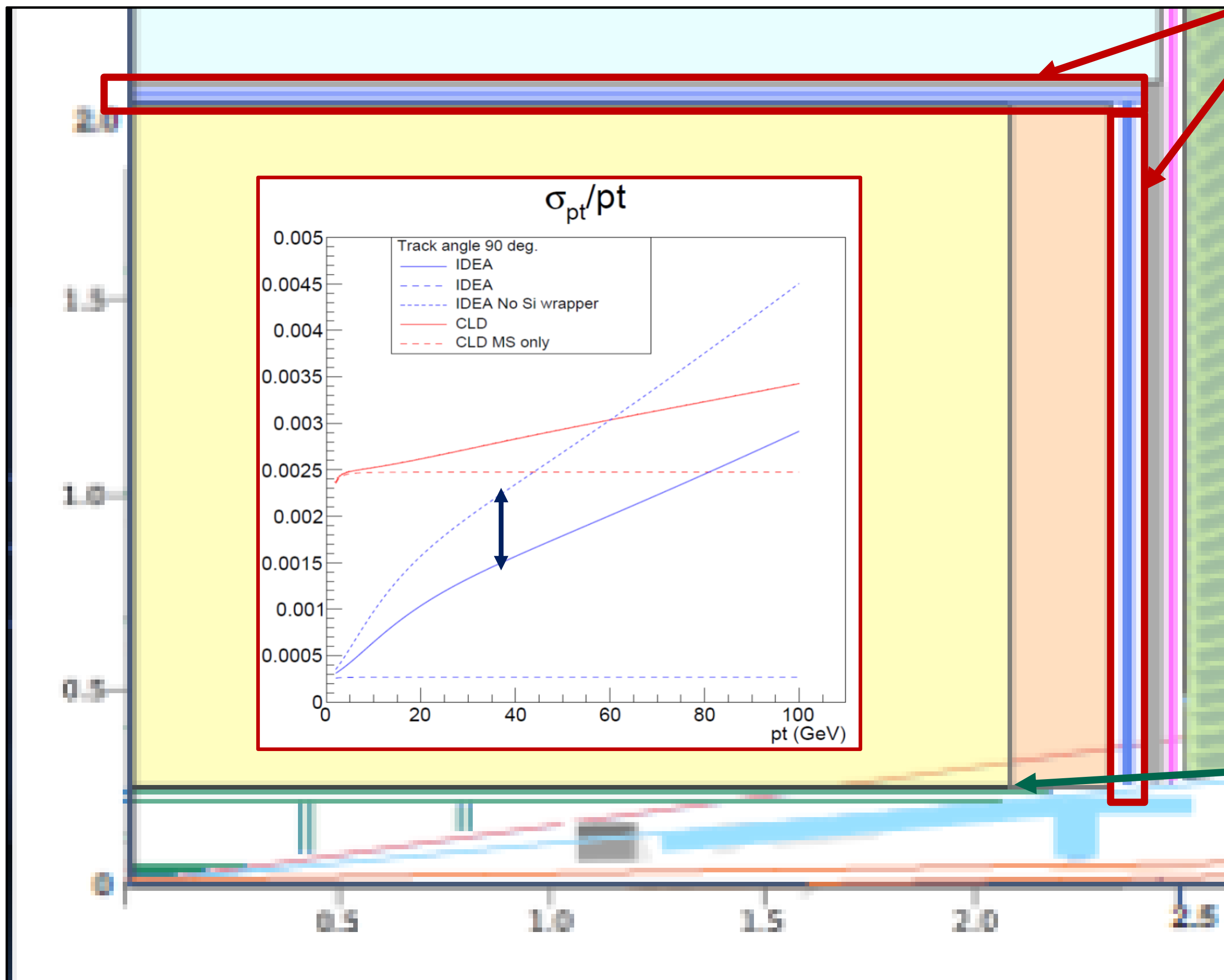
  Most institutes already involved in common R&D for Large Area CMOS Pixel Trackers at Z/Higgs factories (**see ATLASPIX3 status report this morning**)

  The team is not complete yet and we are open to more DRD3 parties

- **Project goal**
  1. New MAPS designs targeting low-power and high granularity, featuring smaller nodes (SMIC foundry 55nm), on-chip solutions allowing for efficient data aggregation (e.g. chip-to-chip communication) and Shunt LDO regulators allowing for serial powering, and multi-chip aggregation via hybrids or on wafer stitching
  2. development of a large-scale system demonstrator, using state-of-the-art CMOS sensors, that has scalability for large area production as a core element of its design and includes a low-mass mechanical support and efficient cooling strategy. Ultra thin and curved designs will be investigated in the context of vertexing to minimize material budget.

  Detailed layout of the project is being developed: scope of this presentation is to trigger a discussion about how it can fit (or be merged) with other WP1 projects

Large Area Trackers



- **Precision silicon layer around the central tracker**
  - **improve momentum resolution**
  - **extend tracking coverage in the forward/backward region** by providing an additional point to particles with few measurements in the drift chamber
  - precise and stable ruler for acceptance definition
  - Covered area ~90 m^2
  - important impact on services
  - need a technology suitable for large size production
- **Long staves in front of the central tracker**
  - limited space for services
  - material is a concern.

55nm High Voltage CMOS Technology

Started development in SMIC 55 nm HVCMOS technology

- Smaller technology node with respect to other technologies we are working with
  - AMS/TSI 180 nm, LF 150 nm
  - comparable to TPSCo 65 nm
  - also considering HLMC 55 nm
- The 55nm logic technology combines improved performance and reduced power consumption with increased design possibilities and cost efficiencies.
- Low voltage power supply is 1.2V
- The maximum voltage for HV transistors is 32V
- Deep n-well to p-substrate should have higher breakdown
- Metal layers 1 – 5 can be used for fine pitch routing
- There are 3 more thick metal layers, suitable for power

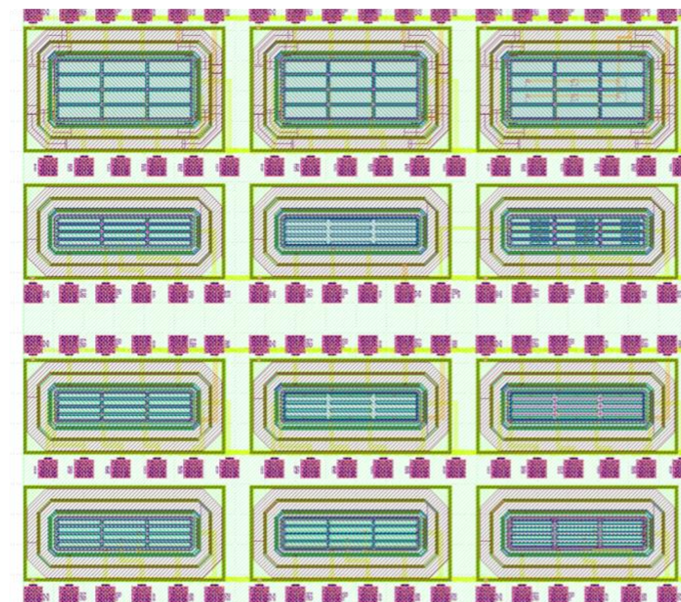
Technology suitable for both the inner vertex and the external layers

- Available on 12" wafers (smaller production that 8" for the same detector area)
- Worthwhile to explore ultra-thinning and stitching to develo

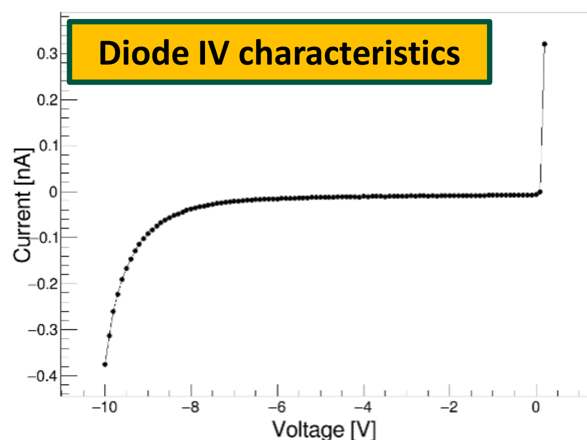
COFFEE1 (SMIC 55 nm process)

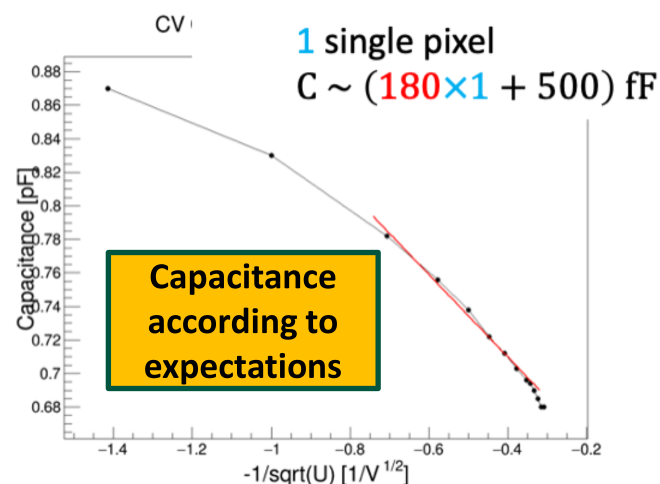
- **Low-Leakage process (no HVCMOS)**
- **Test various passive diode designs**
  - pixel size
  - w/o p-stop
  - pixel separation 5µm, 10µm, 15µm
- Simple amplifiers added
- Submitted: October 2022
  Received: April 2023

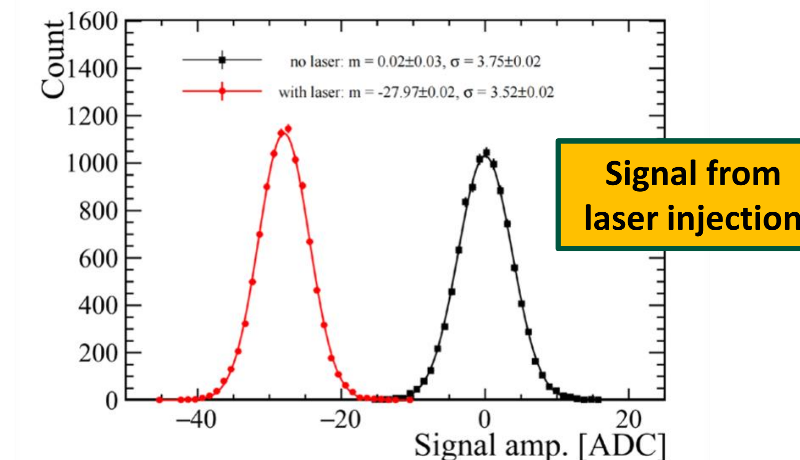
Pixel size:50x150um



Pixel size:25x150um





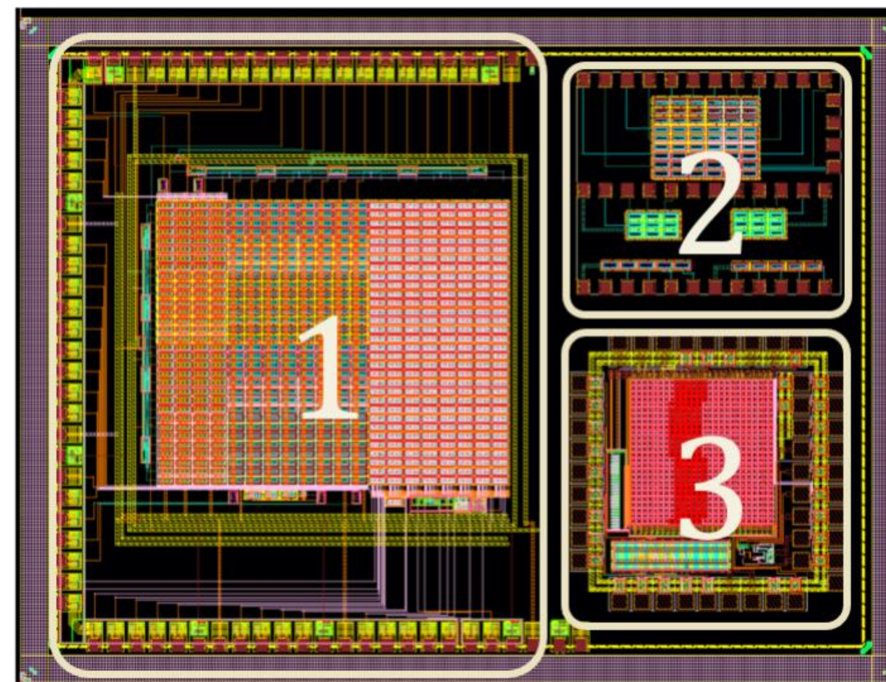


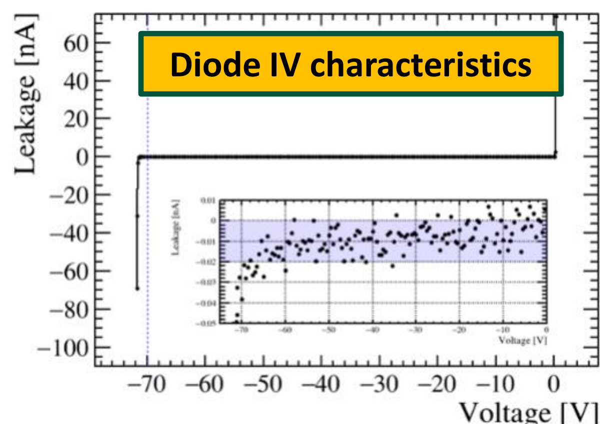
COFFEE2 (SMIC 55 nm process)

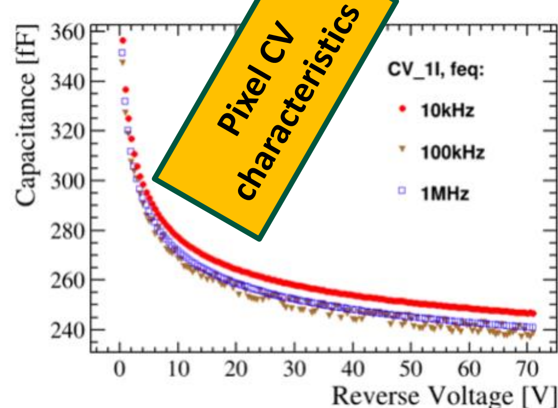
HVCMOS process 1 kΩcm high resistivity substrate

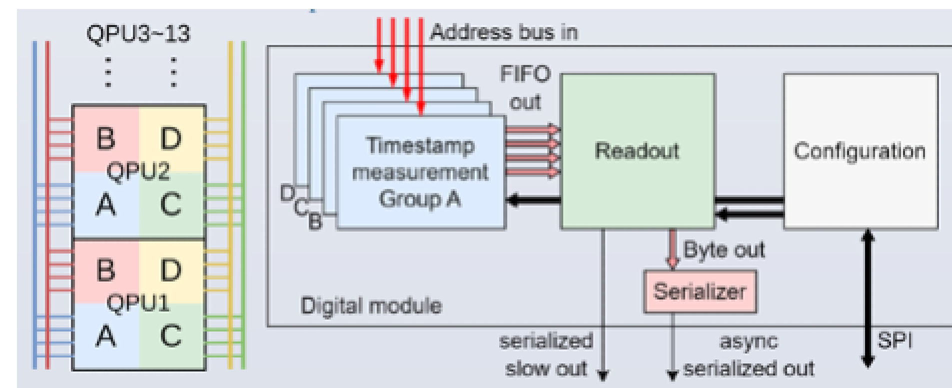
1. 32 × 20 pixel matrix pixel size
   - 40µm × 80µm, 5µm, 10µm, 15µm
   - w/o p-stop
   - 2 versions of in-pixel electronics
2. passive diodes array
3. 26 × 26 pixel matrix 25 µm × 25 µm with peripheral readout testing novel readout structure: **analog address encoding**

- Submitted: August 2023
  Received: December 2023









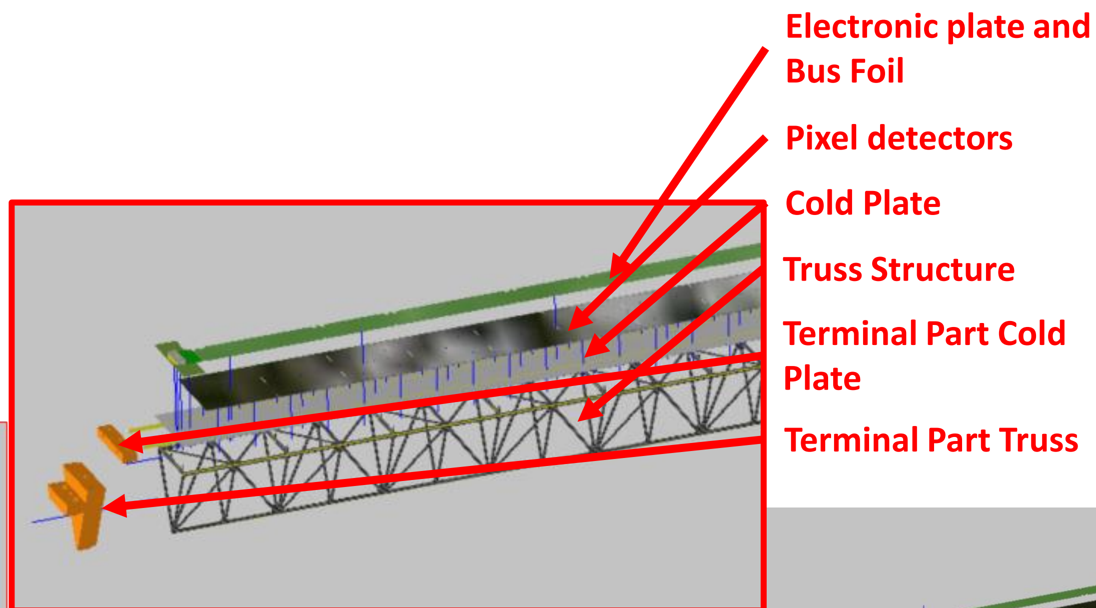
Mechanics and cooling

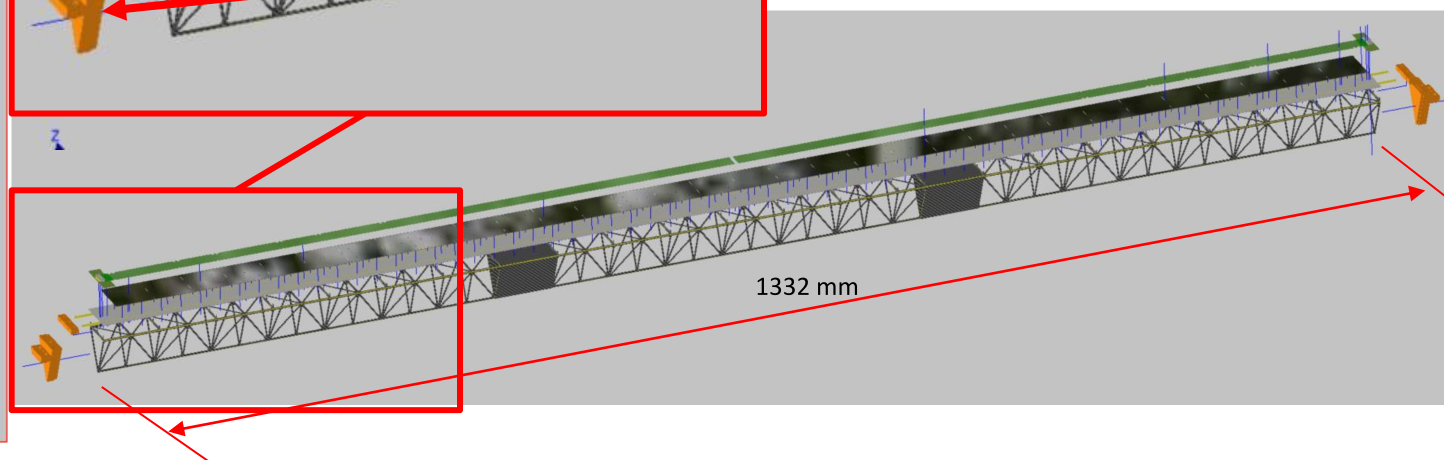
Long stave (1.3 m) mechanical structure fabricated in Pisa

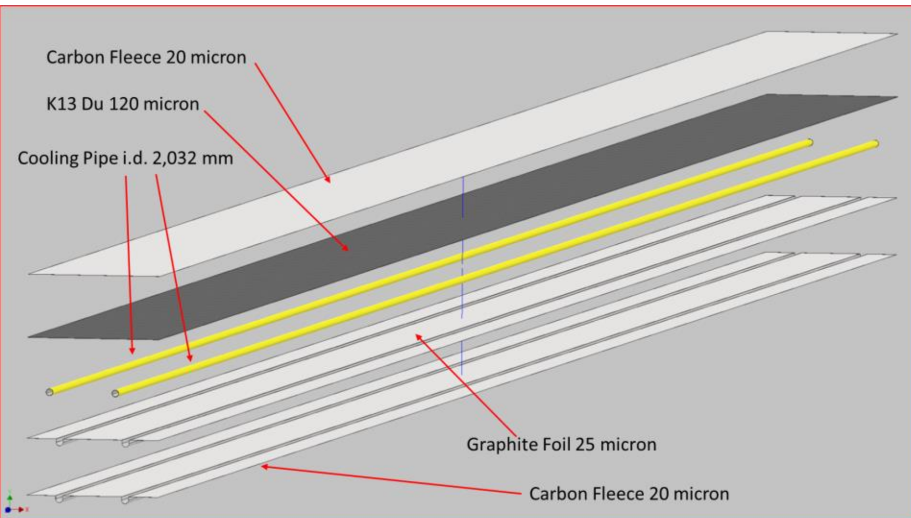
- Truss assembled from water-jet cutout components and glued together
- Thin cold plate with monophase cooling

Solution for the Si-Wrapper structure not yet developed

Connections with DRD8







Stave electrical bus

Distribution of power and data signals along the stave

- reducing power dissipation on the distribution lines
- minimize the number of connections

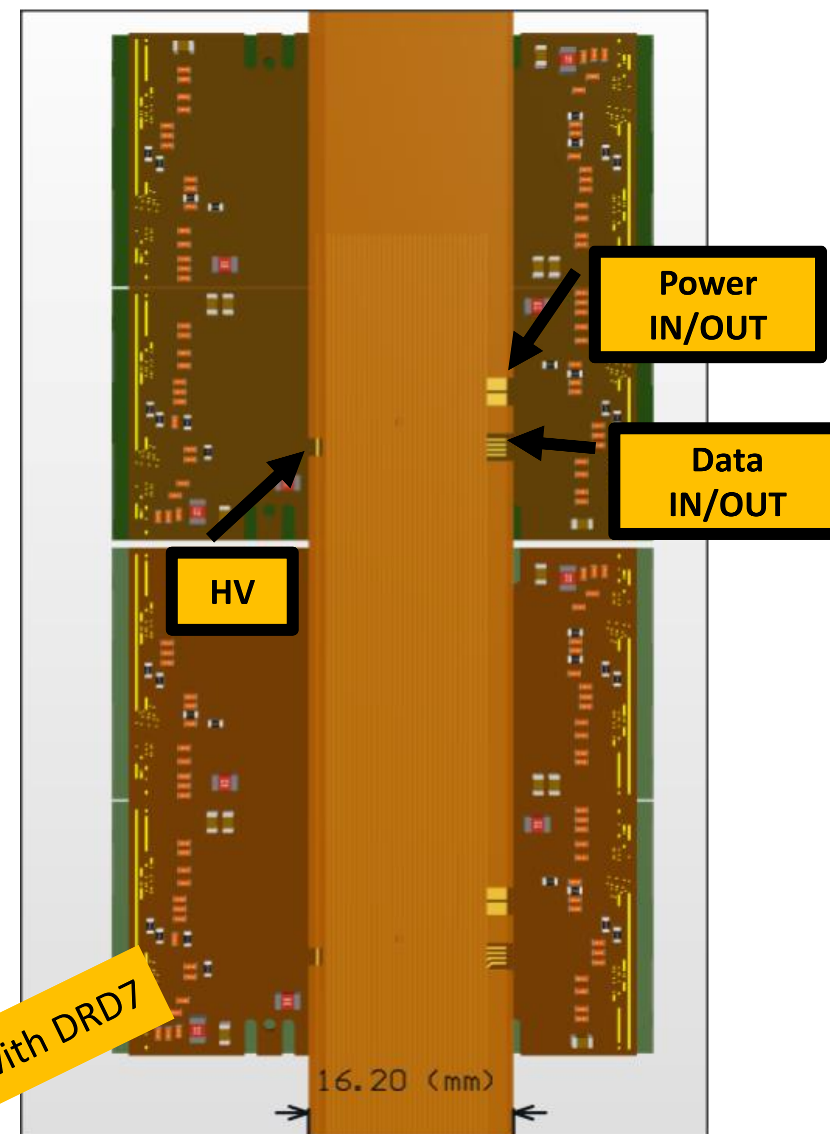
Read-out units are:

- **multi-chip modules** (example 2x2 quad modules)
- large stitched detectors
- bias is in parallel within the components of a module

Minimal I/O connection on chip requires:

- Serial powering chain: all biases generated internally by shunt-LDO regulators
- chip-to-chip data transmissions: local data aggregation on module
- clock data recovery

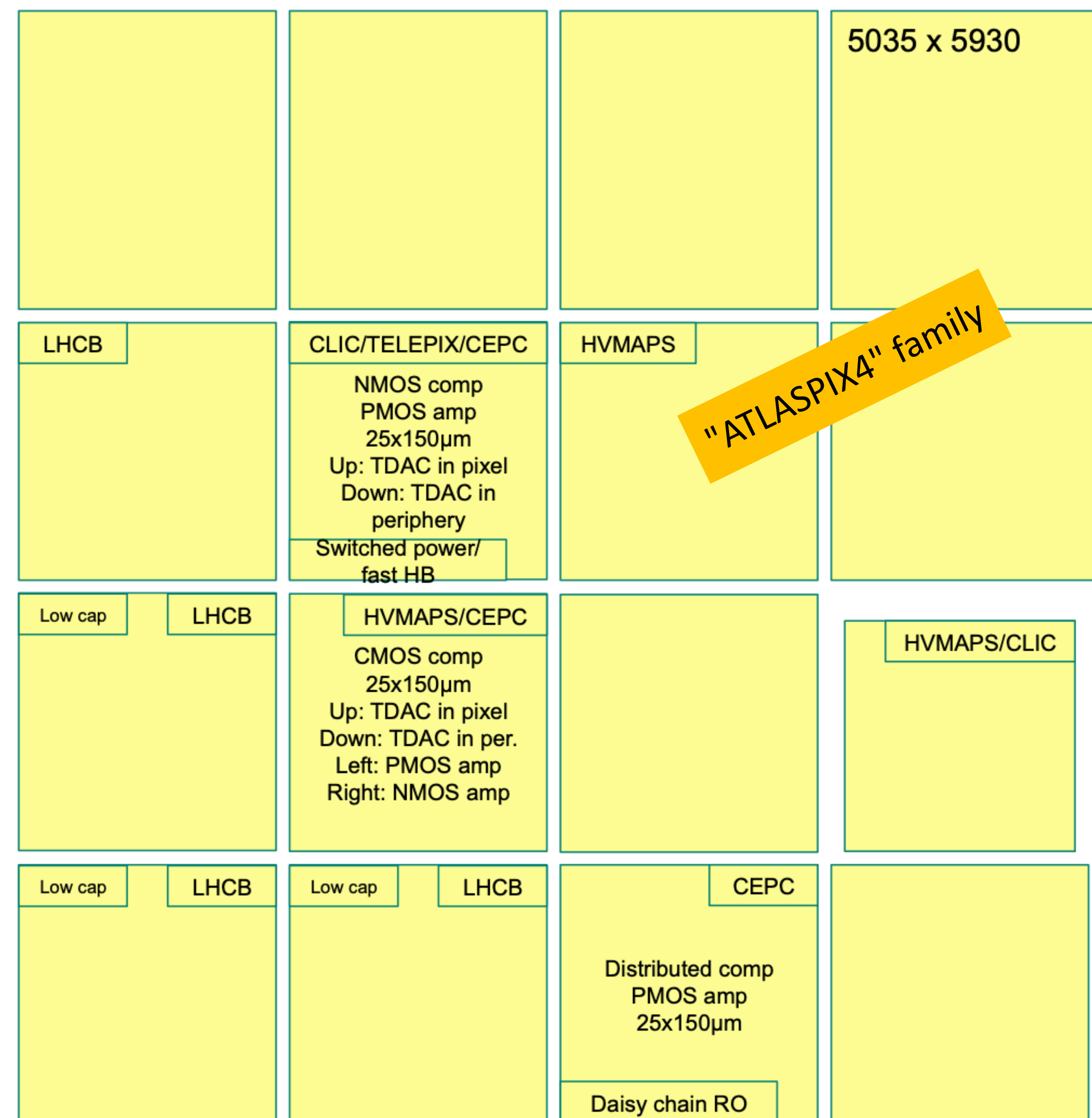
Reduce material by developing PCB with Al as conductor



Connections with DRD7

Workplan

- ATLASPIX3 does not contains all the features needed for efficient integration
  - chip-to-chip data transmission
  - 4 input lines
- Some are available as part of engineering runs developing the ATLAPIX4 family or from LHCb Mighty Tracker
- With FCCee feasibility study and CEPC Detector TDR coming in the next months, we consider a demonstration of the integration process of significant value
- Relevant IPs should also be developed in new technologies, like SMIC 55 nm, to facilitate the convergence of sensor developments into full scale system-on-chip, like ATLASPIX3



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