UNIVERSITÄT BONN

FTD

SI LAB
Silizium Labor Bonn

1ST DRD3 WEEK ON
SOLID STATE DETECTORS R&D

ALL-SILICON LADDER CONCEPT FOR CMOS MONOLITHIC PIXEL DETECTORS

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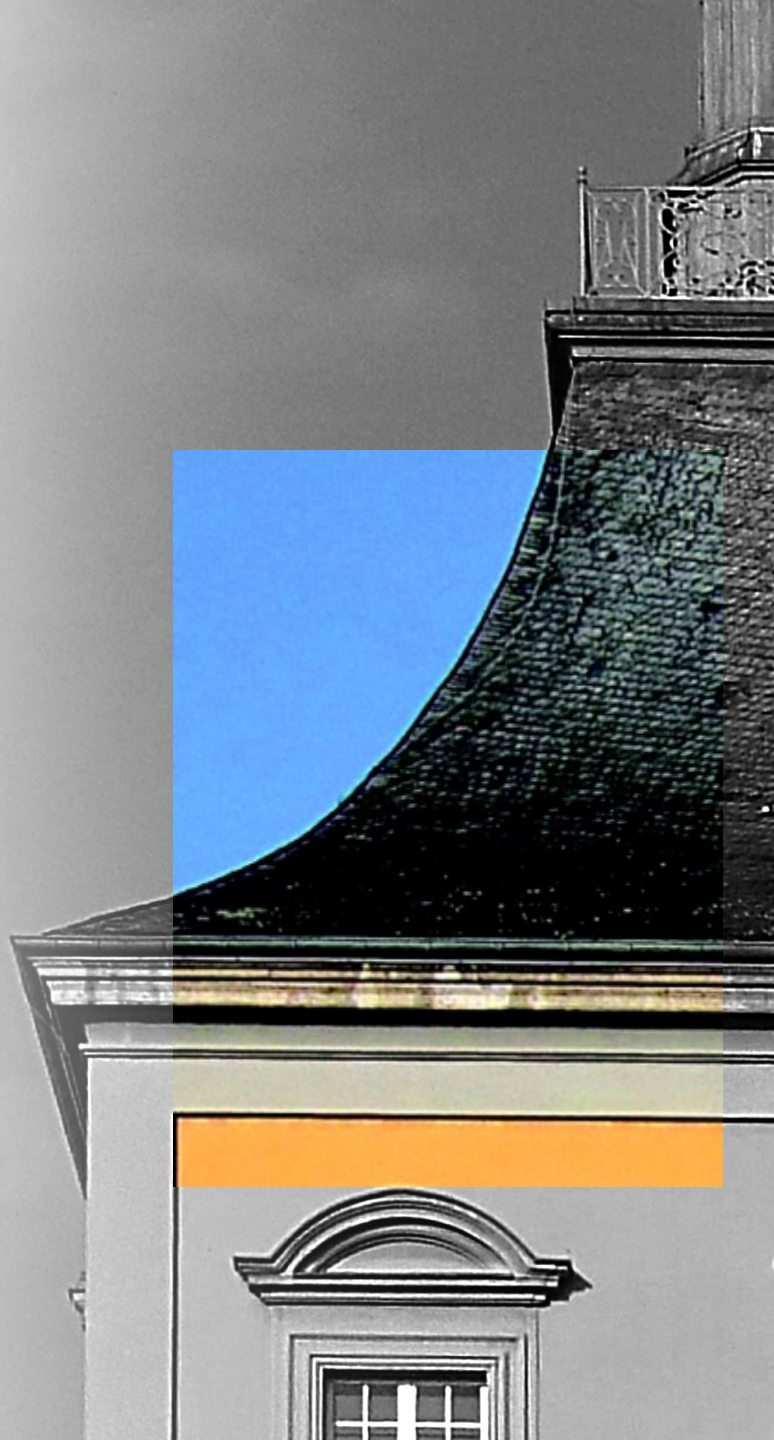
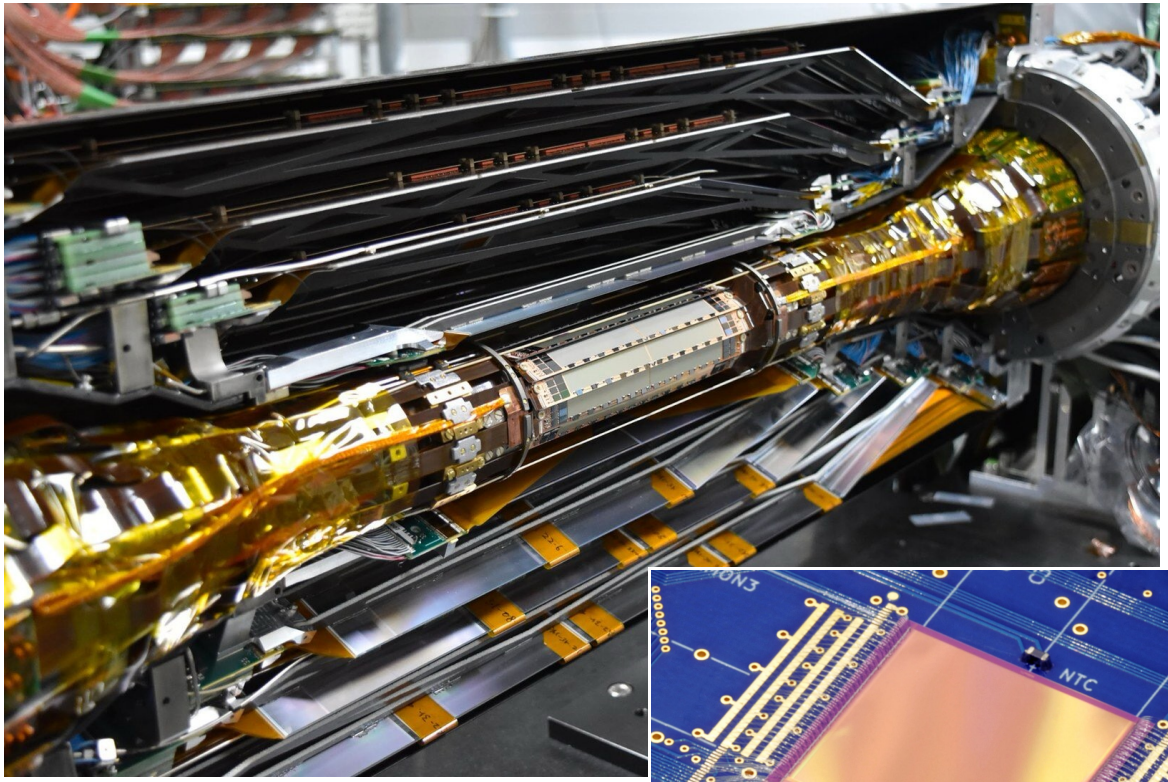
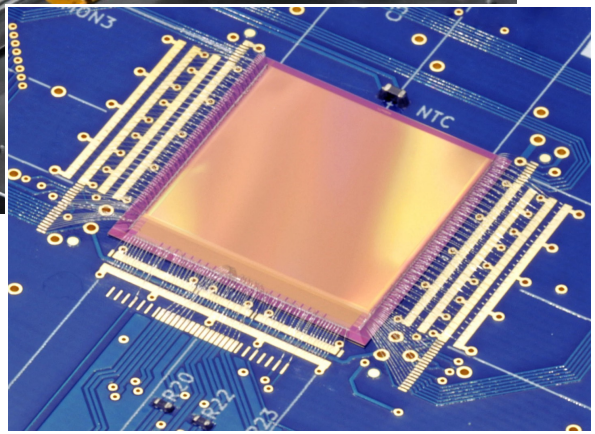
Affiliations: U. Bonn (B), U. Göttingen (G), IFIC Valencia (V)



MOTIVATION



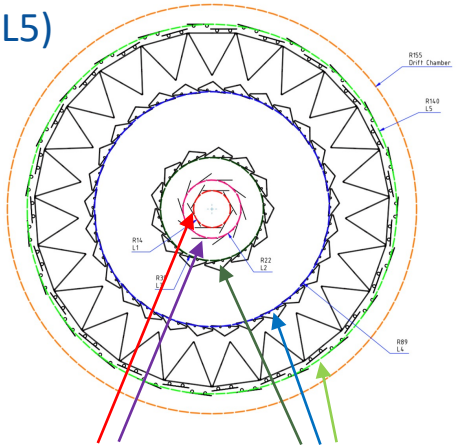
Vertex detector (VXD), Belle II



CMOS sensor TJ-Monopix2

Belle II LS2 in ~2030

- Opportunity to upgrade the vertex detector
- Monolithic active CMOS pixel sensor OBELIX, evolving from TJ-Monopix2
- L1+L2: self-supporting, air cooled
- L3-L5: CF structure, water cooled
- Low material budged
  0.2% X_0 (L1+L2) … 0.8% X_0 (L4+L5)

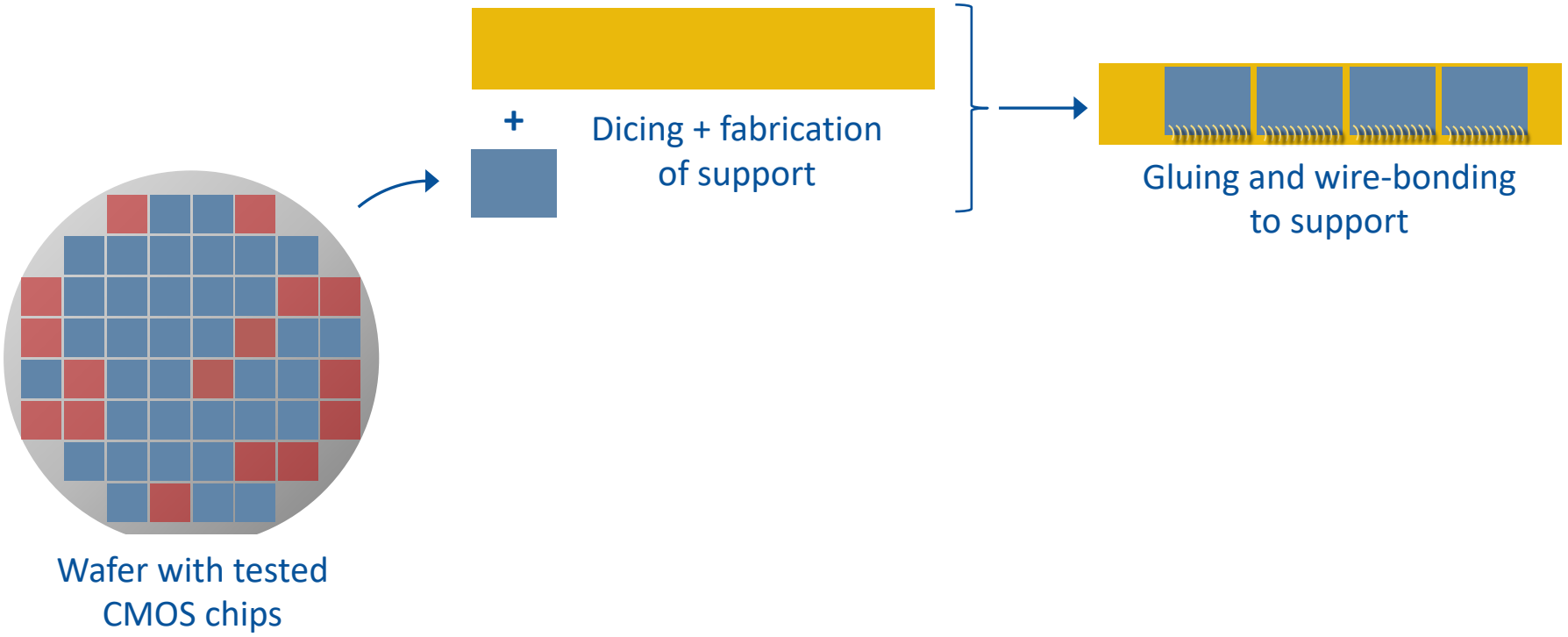


L1, L2: **iVTX**

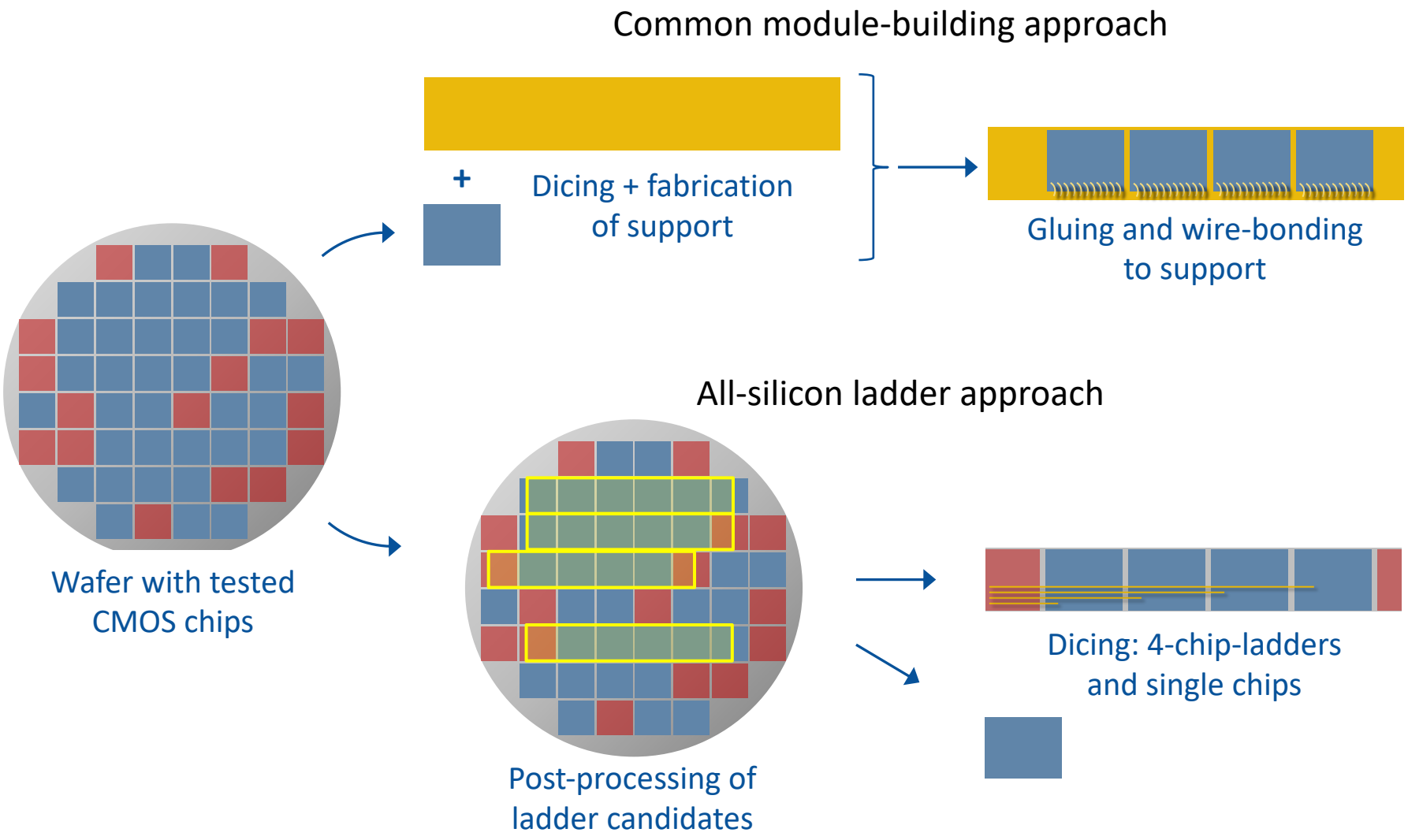
L3-L5: **oVTX**

ALL-SILICON LADDER CONCEPT

Common module-building approach



ALL-SILICON LADDER CONCEPT



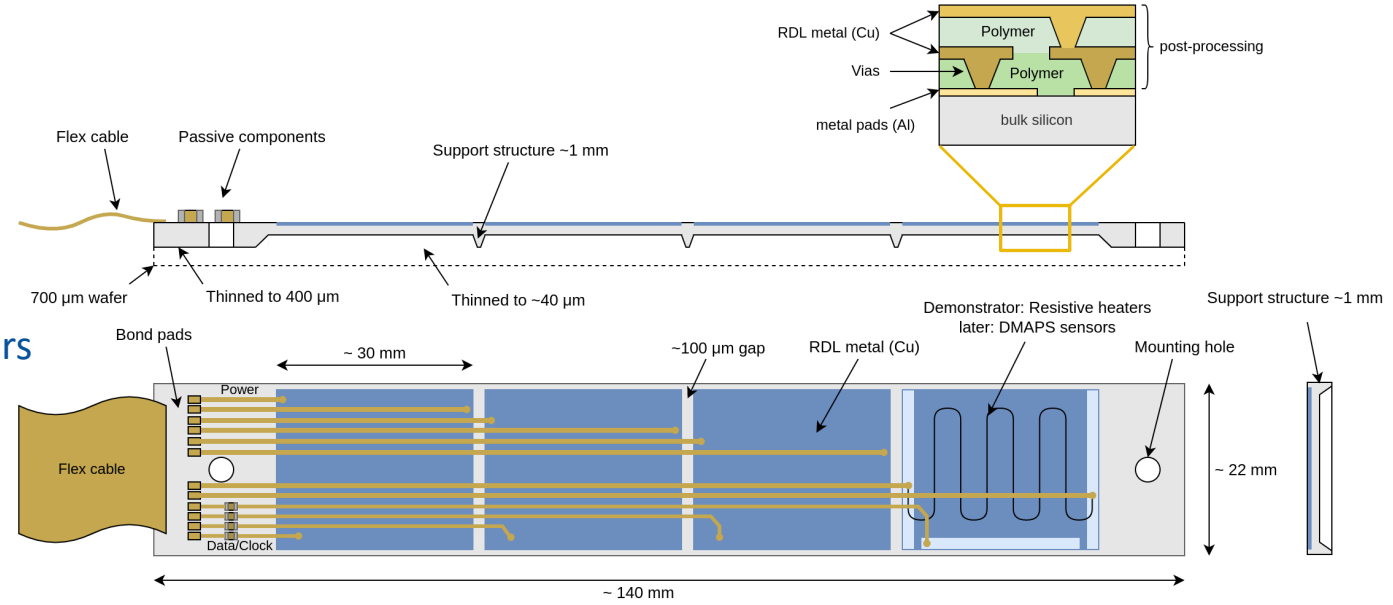
ALL-SILICON LADDER CONCEPT

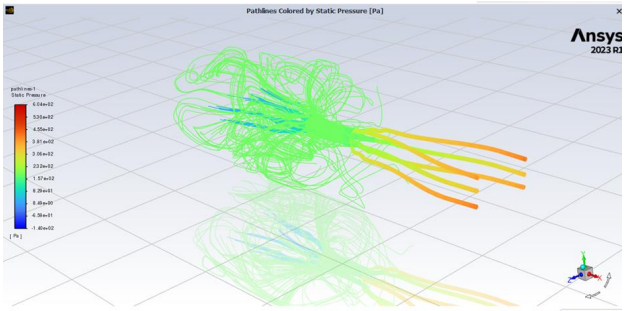
All-silicon ladder

- Single piece of silicon
- 4 sensors cut in one piece from the wafer

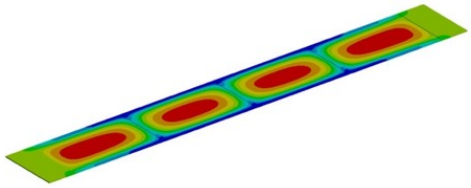
Post-processing of wafer

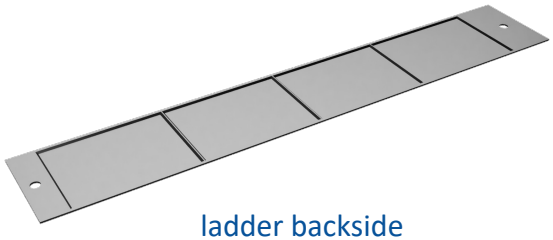
- Redistribution metal layers for data and power
- Heterogeneous backside thinning





T_{MAX} ~ 20°C
ΔT < 5°C



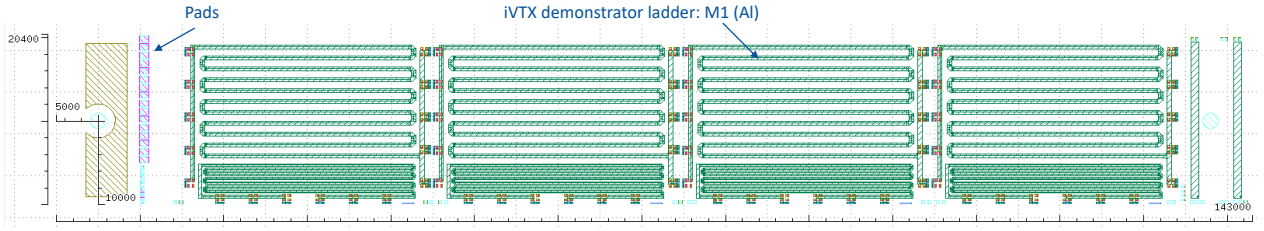


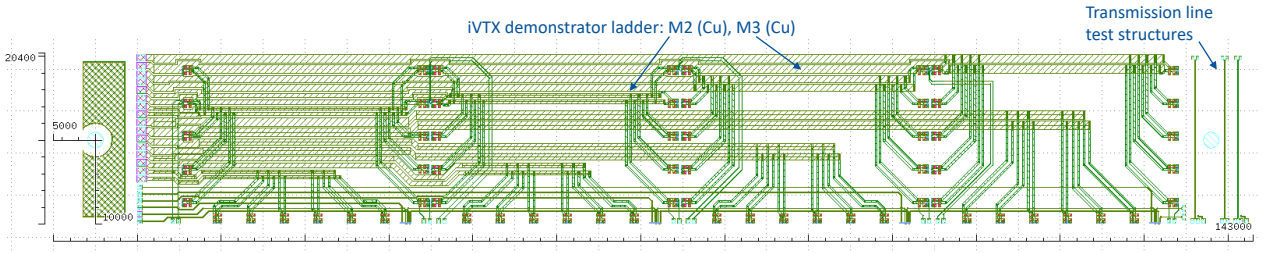
ladder backside

Thermal and airflow simulations for Belle II iVTX (IJClab, Paris)

ALL-SILICON LADDER LAYOUT

First RDL demonstrator with resistive heaters instead of CMOS sensors

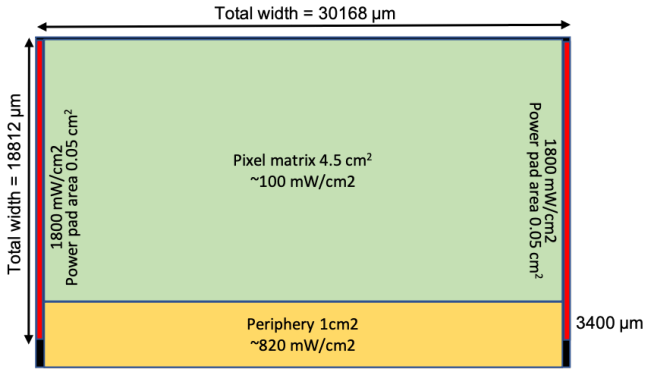




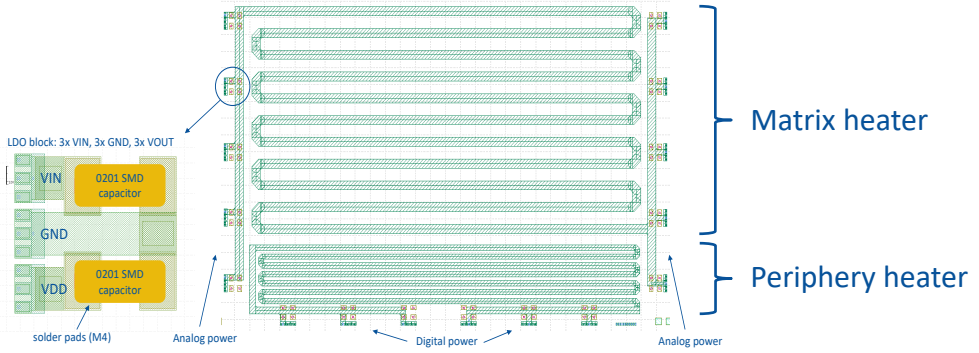
Metal system:

- Resistive heaters: 1.5 µm Al
- 2 RDL metal layers: 4 µm Cu
- Top metal finish: NiAu for wire-bonding, SMD soldering

Ladder dimension: 143 x 20.4 mm²
Dummy heaters (~10 Ω): 30 x 20 mm²



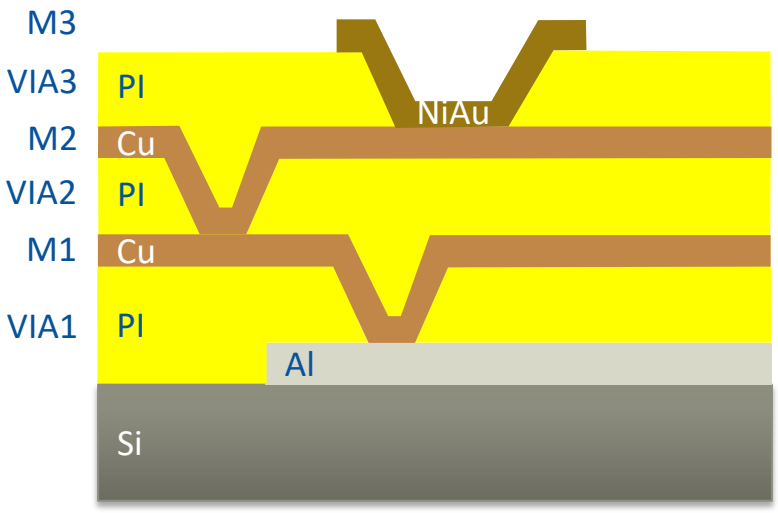
CMOS sensor example: Power domains, power pad locations



ALL-SILICON LADDER FABRICATION

Main fabrication steps:

- Alternating deposition of metal (4 µm Cu) and polymer (7 µm Polyimide)
- Photo lithography, wet chemical patterning

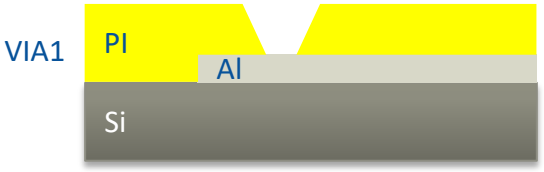


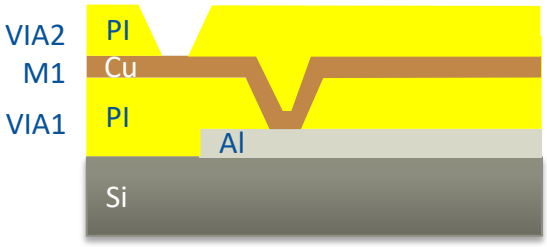
- First polymer layer “VIA1”
  - Openings above sensor bond pads
- First RDL metal “M1”
  - Contacts to sensor bond pads
- Second polymer layer “VIA2”
  - Openings to M1
- Second RDL metal “M2”
  - Contacts to M1
- Passivation layer “VIA3”
  - Openings to M2
- NiAu bond pads “M3”
  - Contacts to M2

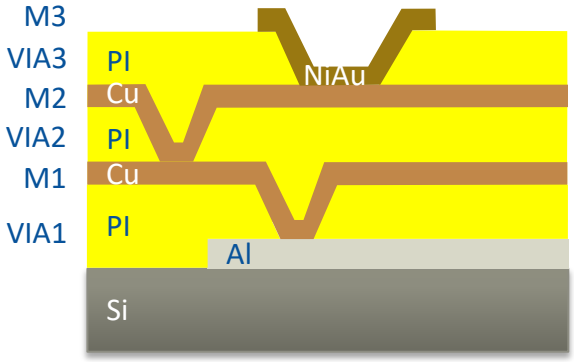
ALL-SILICON LADDER FABRICATION

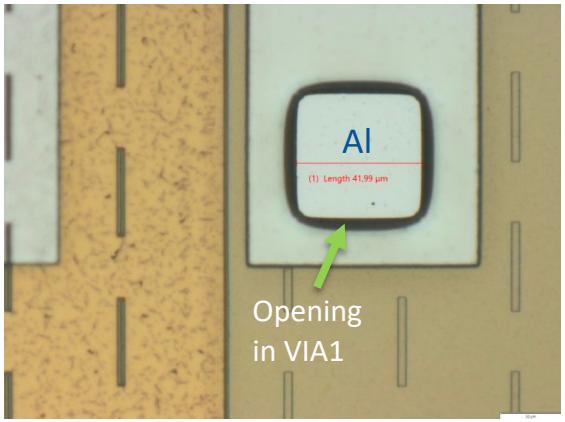
RDL process documentation of the first demonstrator produced by IZM Berlin

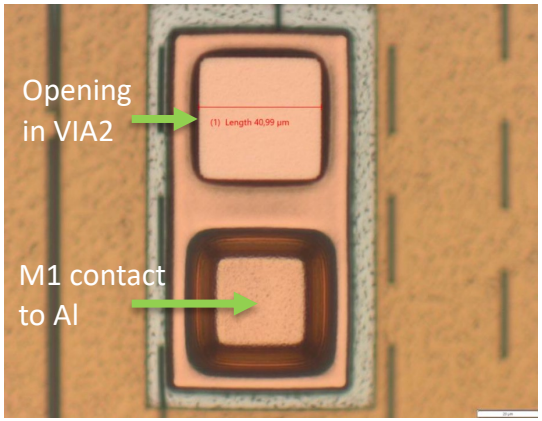
Characterization of layer topography, wafer flatness etc.

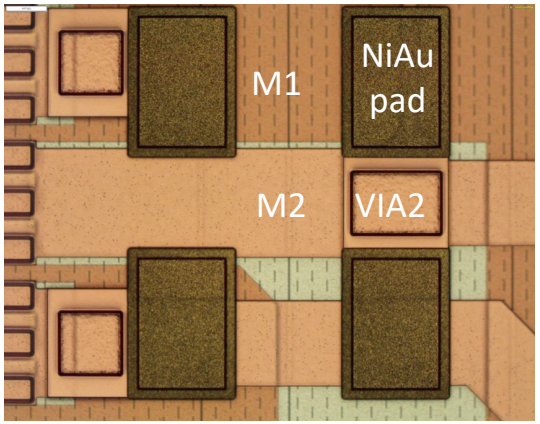










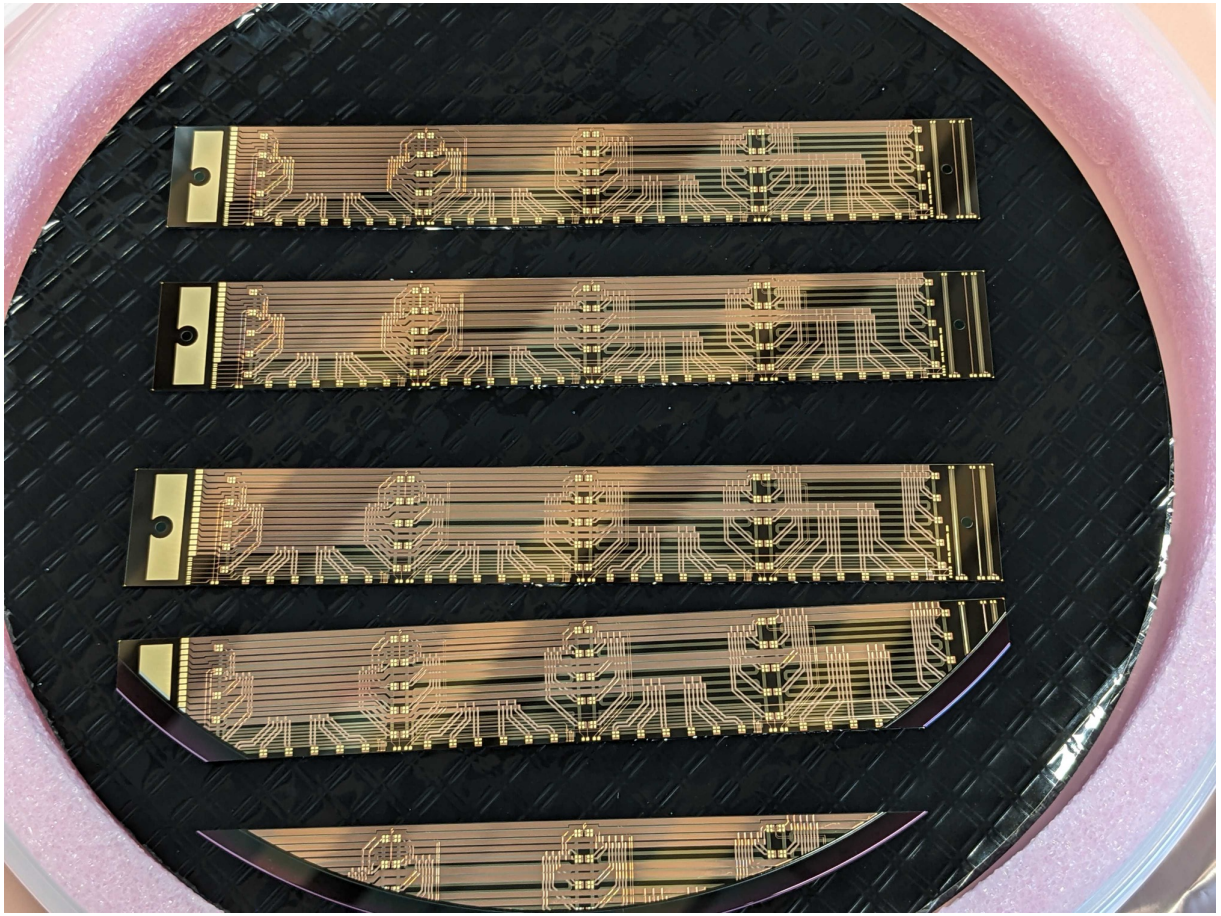


Pictures by IZM Berlin

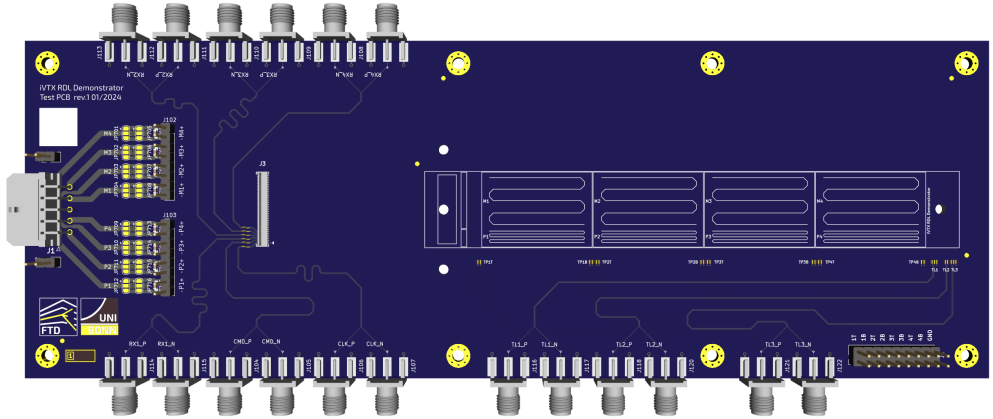
ALL-SILICON LADDER DEMONSTRATOR

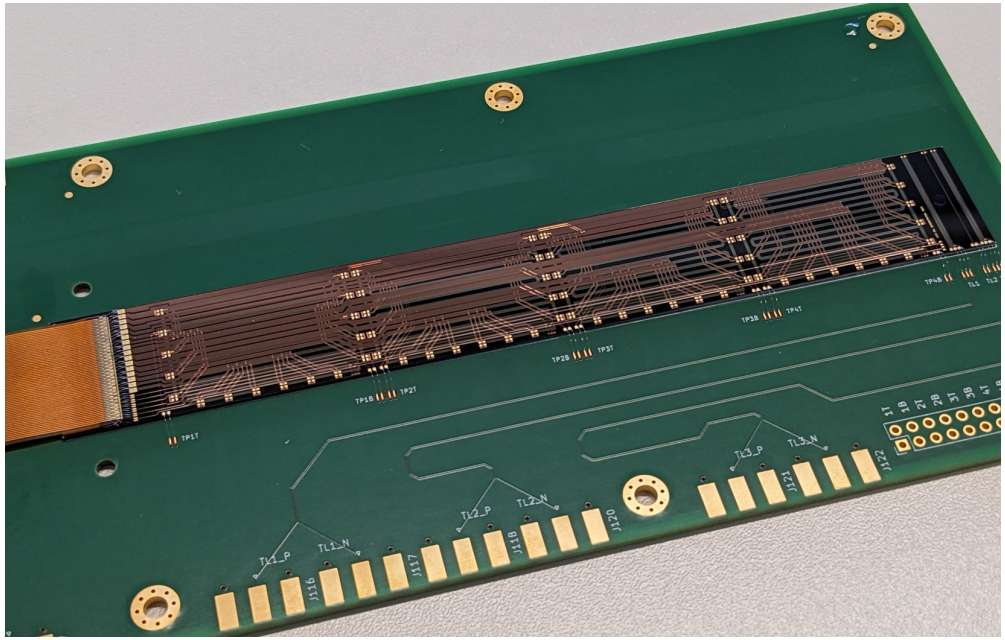
First RDL demonstrators: 8 Wafers (725 µm, 400 µm, 300 µm)

Production finished smoothly



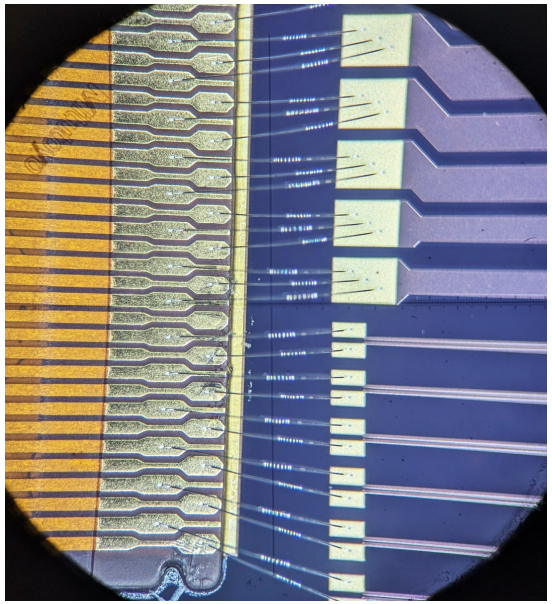
ALL-SILICON LADDER DEMONSTRATOR





PCBs for electrical tests

- Configurable power routing and test points for I*R drop measurements
- SMA connectors for differential lanes (TDR measurements)
- PCB mockups of the ladder for SMD soldering studies



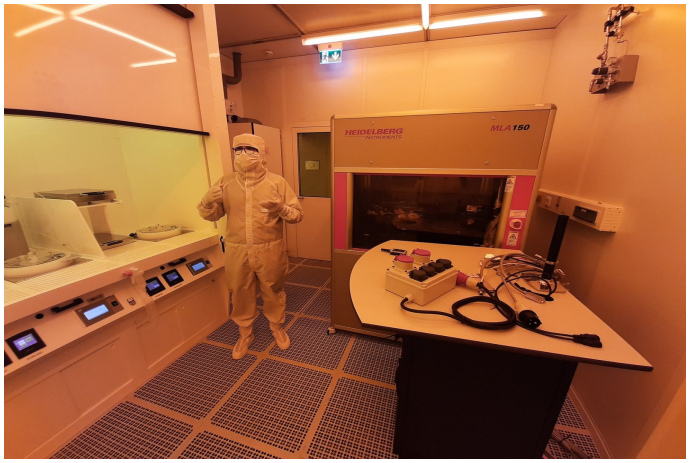
OUTLOOK

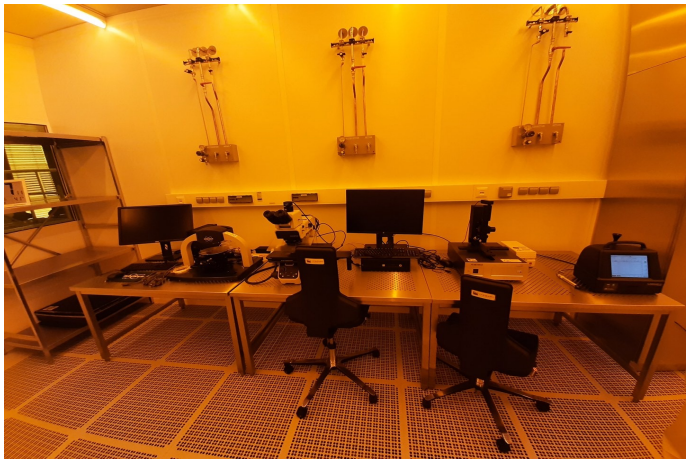
Generic R&D for future colliders (e.g. FCC)
→ German Si-D Consortium

- U. Bonn, TU Dortmund, U. Göttingen, HLL
- Sharing of infrastructure
- Development of designs and methods for low-material all-silicon CMOS modules
- Design & Simulation, wafer processing, characterization, system integration

Prototyping:

- 360 m^2 clean room area in Bonn
- Processing of 200 mm wafers
- Micro structuring (MLA, chemical patterning)
- Micro interconnect technology





Cleanroom in Bonn: MLA, wetbenches, characterization

SUMMARY

All-silicon ladder concept evaluation

- Low material budget applications
- Reduction of components
- First RDL demonstrator

Use case: Belle II iVTX

- Opportunity for vertex detector upgrade in 2030
- Evaluation of system aspects (Valencia)

Generic R&D for future colliders

- Collaboration to develop designs and methods
- Starting cleanroom activities