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# All-silicon ladder concept for CMOS monolithic pixel detectors

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CMOS sensor technology leverages the production of fully monolithic pixel detectors with smaller pixel size and without costly interconnections between sensors and readout electronics. This results in cost reduction and lower material budget in the detector volume.

An additional opportunity for further improvement is the module assembly method. By integrating power- and data lines directly on the CMOS wafer, all-silicon ladders are created, eliminating the need for hybrid PCBs and reducing material. Wafer-scale post-processing methods can be used to deposit alternating layers of metal and polymer on the surface, creating electrical redistribution layers (RDL).
Each ladder, consisting of multiple neighboring sensors on the wafer, is diced in one large self-supporting piece, allowing for direct assembly in the detector. Within power constraints, direct air cooling can be applied.

Initial technology demonstrators are constructed and evaluated to validate the feasibility of this approach for low material budget applications like the upgrade of the Belle II vertex detector.

This presentation will outline the all-silicon ladder concept, the RDL processing steps and the design of first demonstrators.

## Type of presentation (in-person/online)

online presentation (zoom)

## Type of presentation (scientific results or project proposal)

Presentation on scientific results

**Primary author:** VOGT, Marco (Universitaet Bonn (DE))

**Co-authors:** MARINAS, Carlos (University of Bonn); KRUEGER, Hans (University of Bonn); DINGFELDER, Jochen Christian (University of Bonn (DE))

**Presenter:** VOGT, Marco (Universitaet Bonn (DE))

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