CMOS Active SenSor with Internal Amplification – CASSIA

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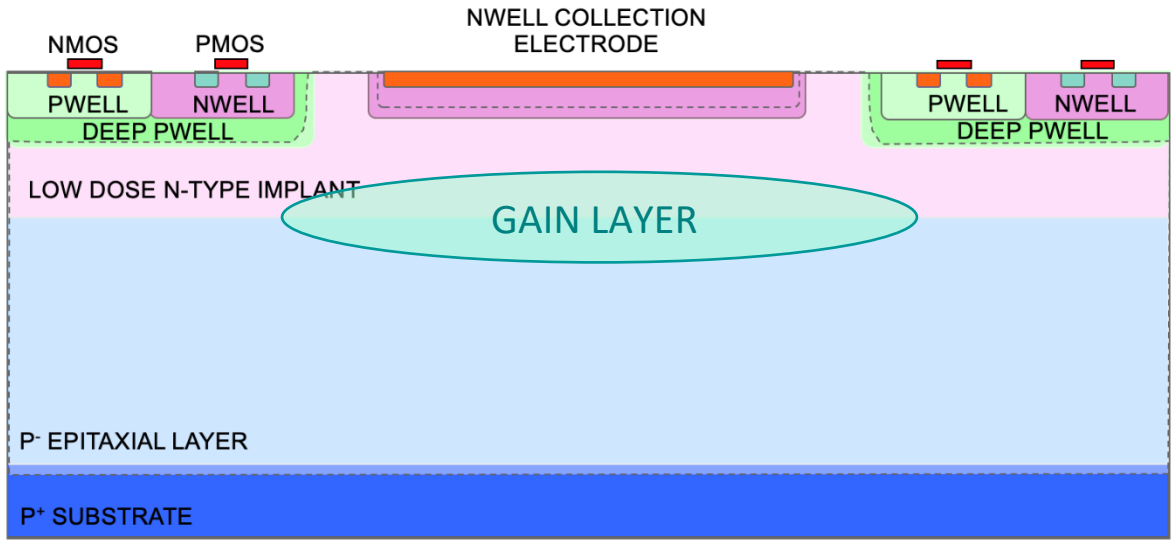
CMOS Active SenSor with Internal Amplification – CASSIA

Goal:

- Active sensor with in-pixel internal gain
- CMOS-compatible technology



Internal amplification:

- In-pixel integration with read-out electronics
- Avalanche multiplication:
  - Low-gain avalanche diode (LGAD)
  - Single-photon avalanche diode (SPAD)
- Strong signal: low-power read-out
- Improved signal-to-noise ratio
- High timing resolution, short response time

Implementation:

- Gain layer
  - Standard foundry CMOS layer
  - Additional process
- Sensor integrated with deep p-well isolation (to accommodate read-out electronics)
- Breakdown voltage engineering possible with Gain layer selection

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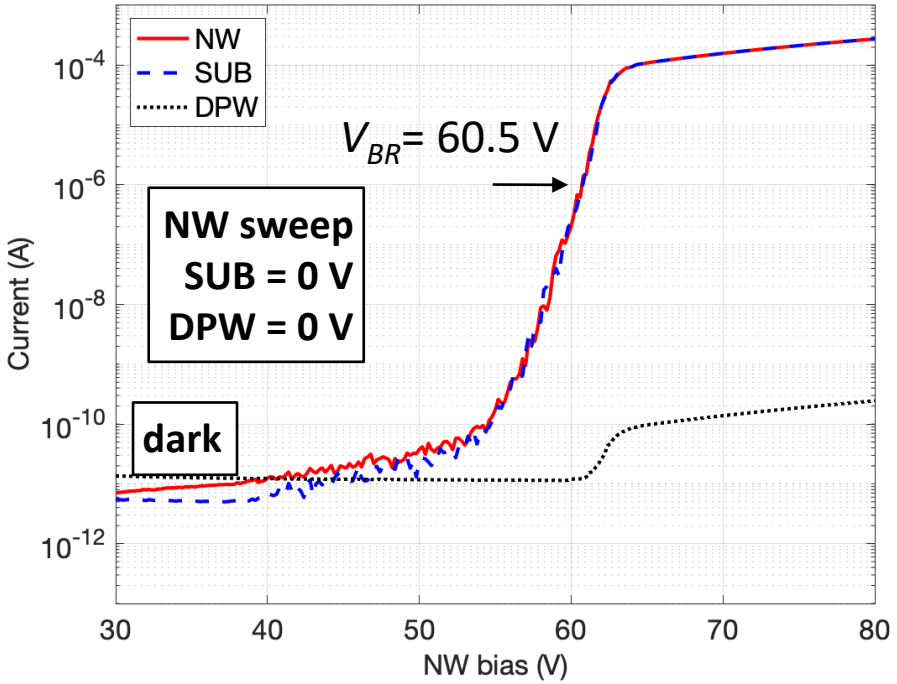
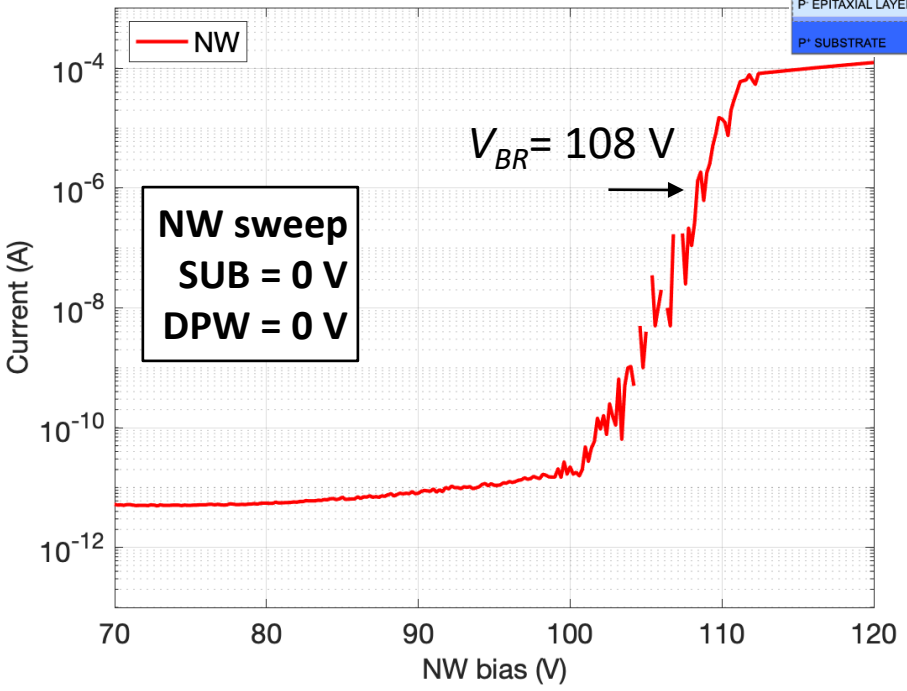
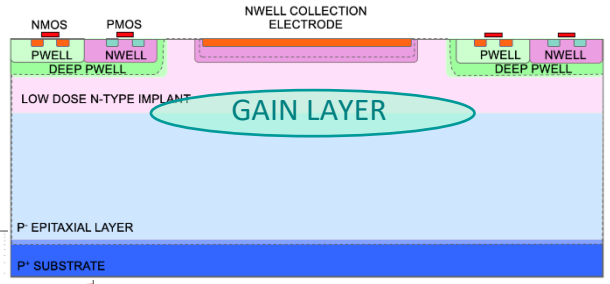
- Prototype: 180nm TJ CMOS image process technology
- On-chip measurements:







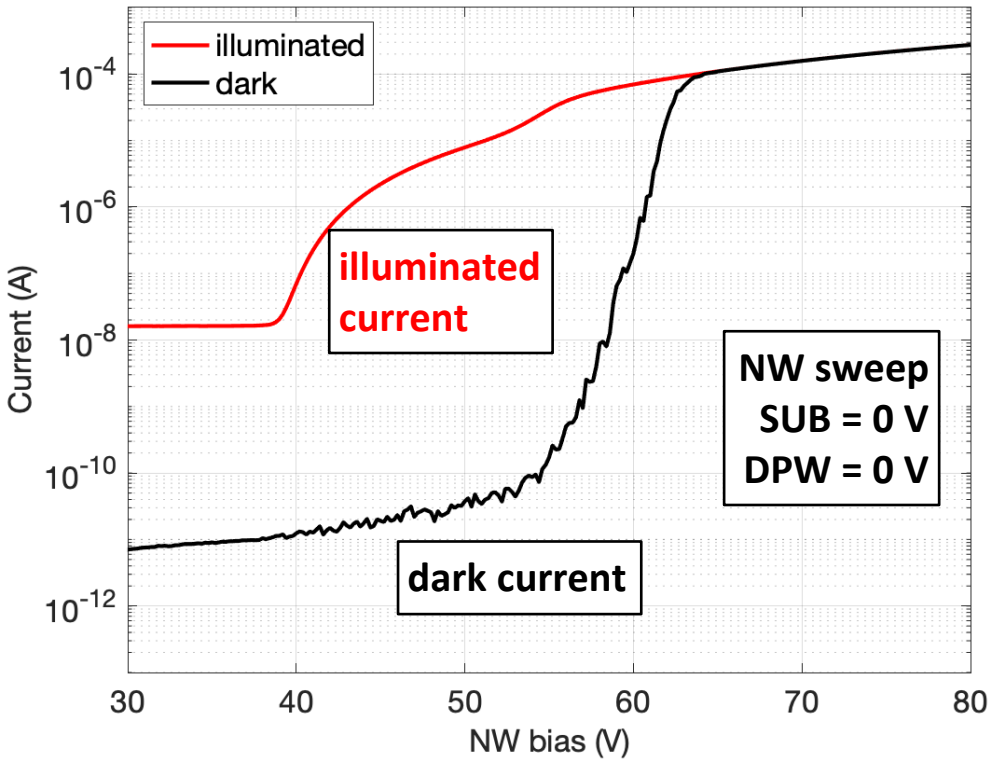
Gain layer 1

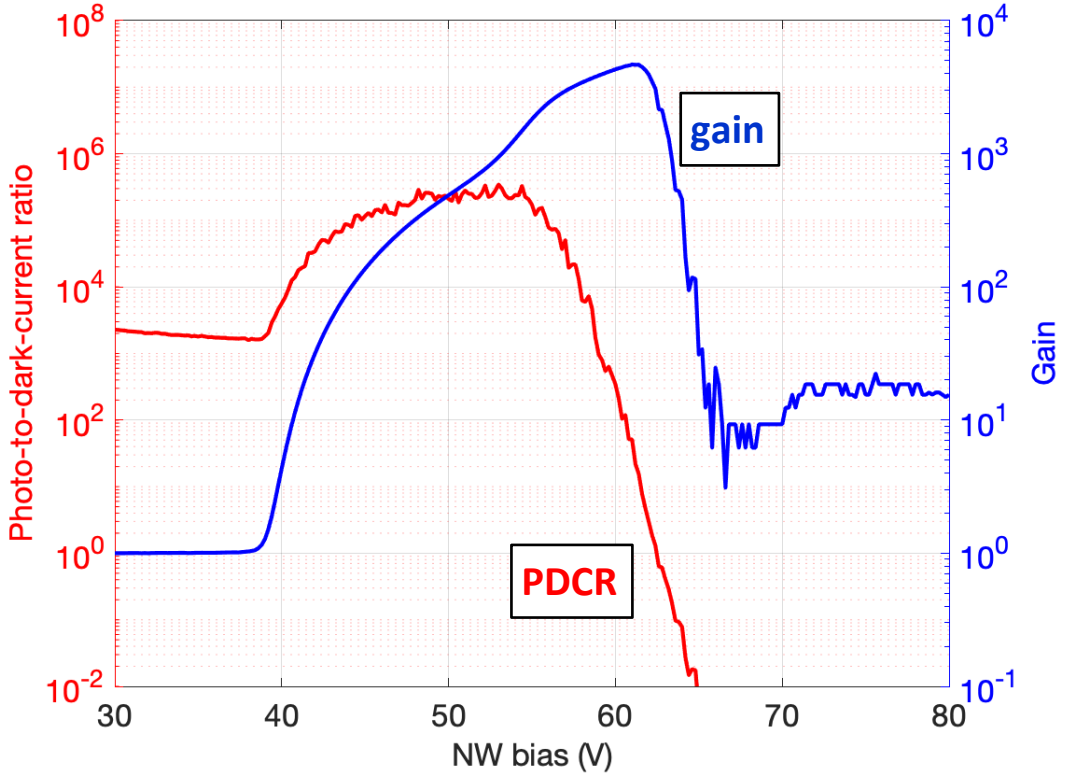
- Avalanche multiplication starts ~55 V
- Low leakage currents in the range < pA

Gain layer 2

- Avalanche multiplication starts ~100 V
- Low leakage currents in the range < pA

CASSIA response to illumination – Gain layer 1

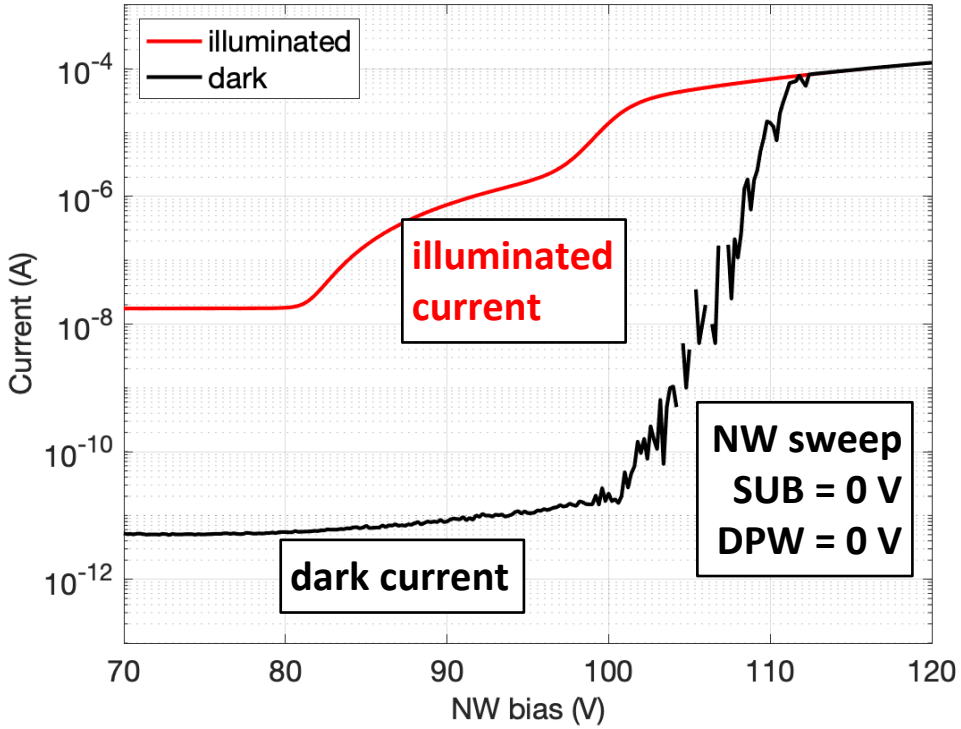


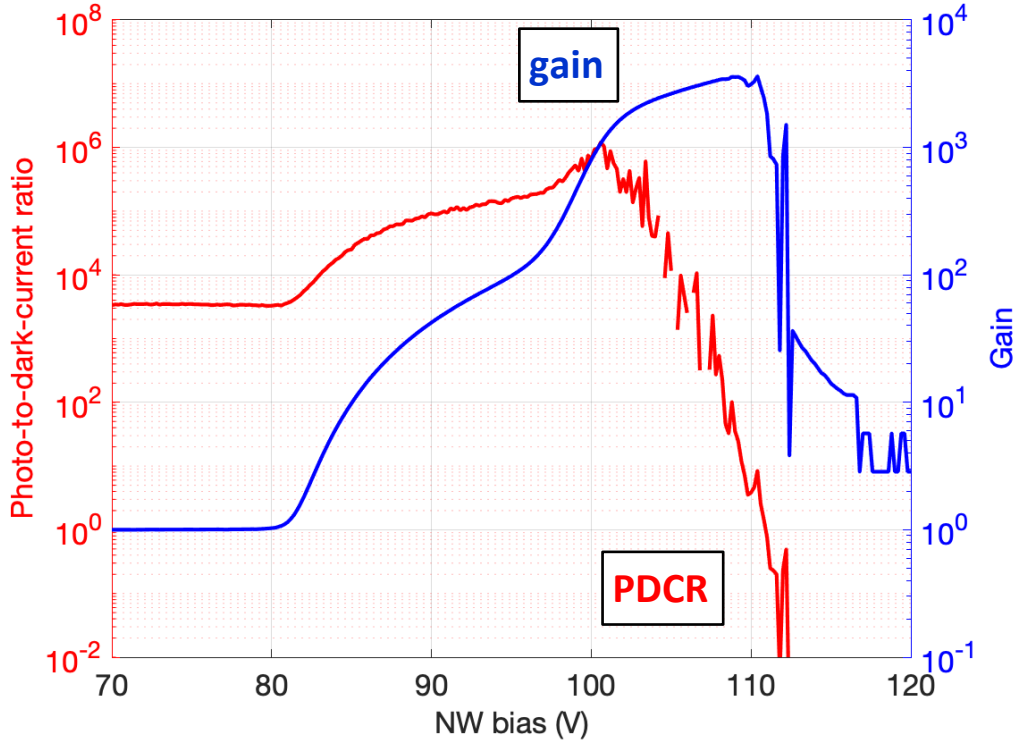


- Illuminated by continuous visible light
- avalanche multiplication of photogenerated carriers already at biases above ~39 V

- photo-to-dark-current ratio (PDCR) up to >10^5
- gain reaching values >5000
- Fine gain adjustment by reverse voltage, 25 V span

CASSIA response to illumination – Gain layer 2

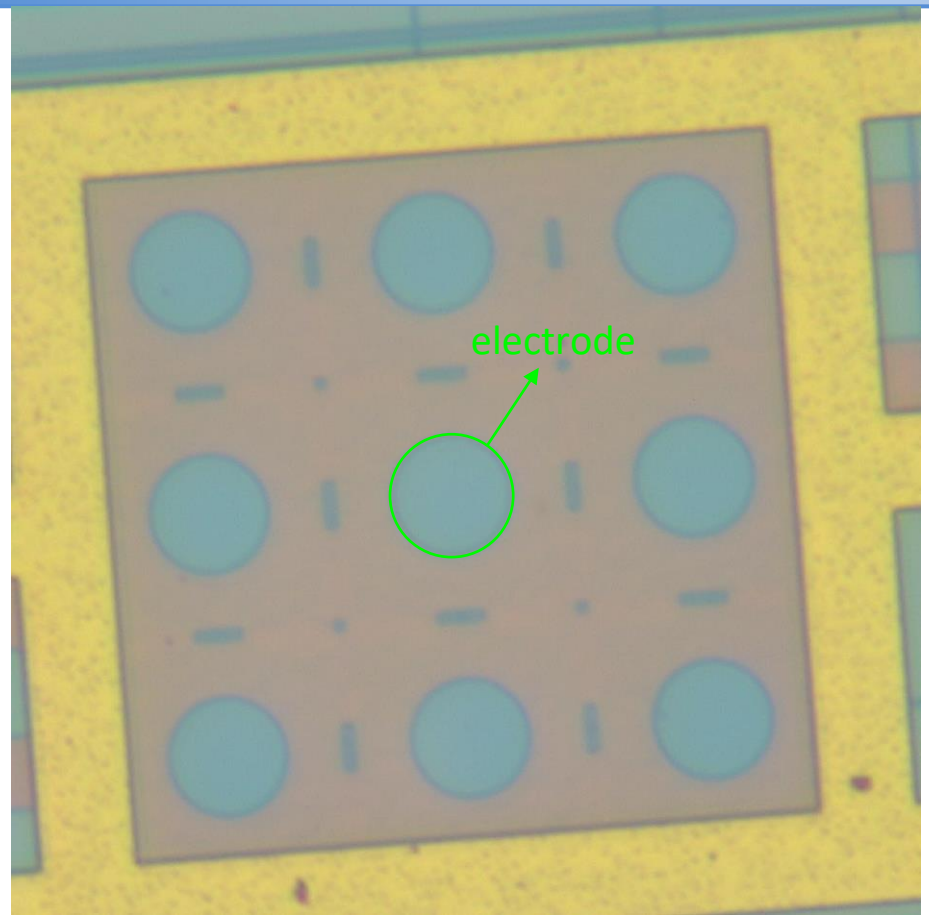




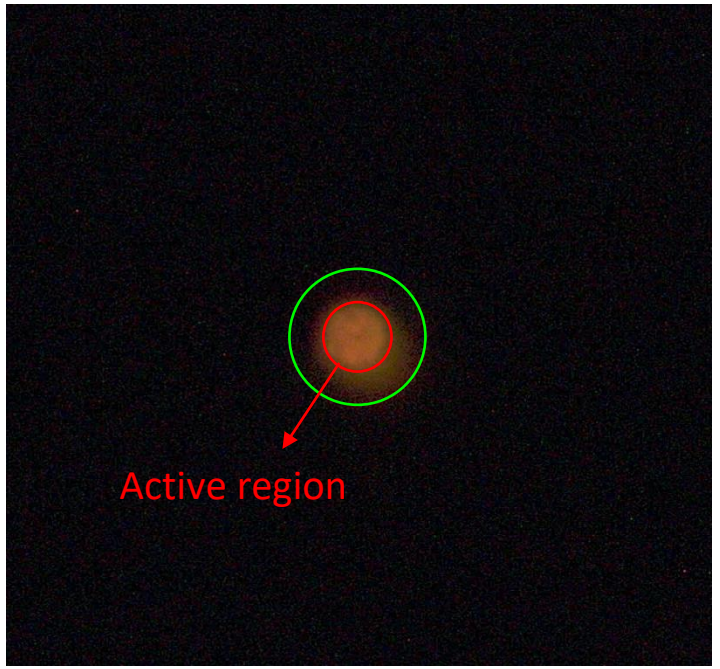
- Illuminated by visible light
- avalanche multiplication of photogenerated carriers already at biases above ~82 V

- photo-to-dark-current ratio (PDCR) up to >10^6
- gain reaching values >5000
- Fine gain adjustment by reverse voltage, 30 V span

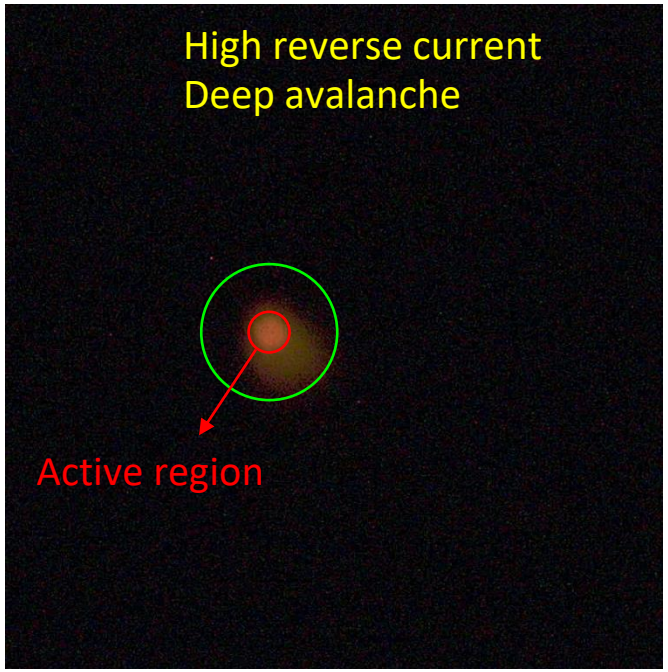
CASSIA light emission test



- Fabricated CASSIA sensor micrograph

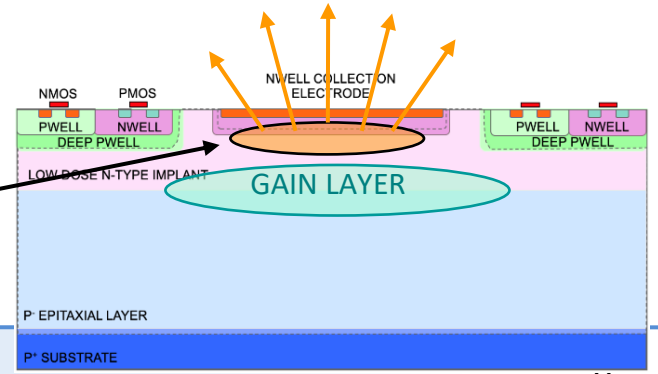


Gain layer 1

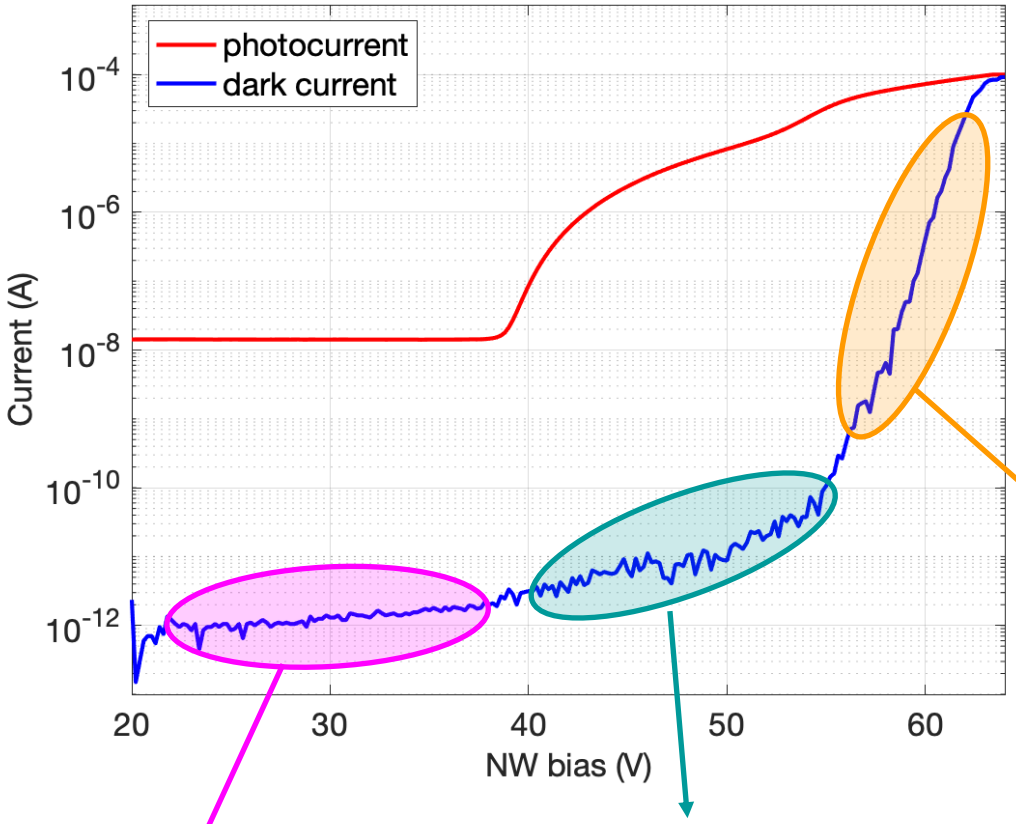


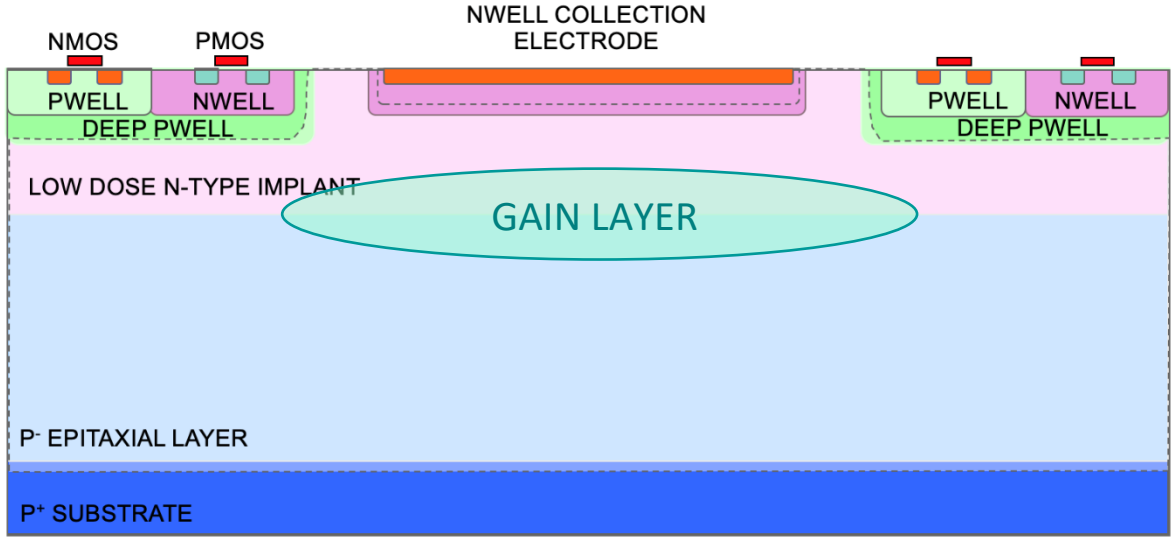
Gain layer 2

- Approx uniform emission
- Avalanche multiplication across the active junction
- No perimeter breakdown



CASSIA – LGAD & SPAD regimes





Same device, different operating bias

No-gain regime

LGAD regime:

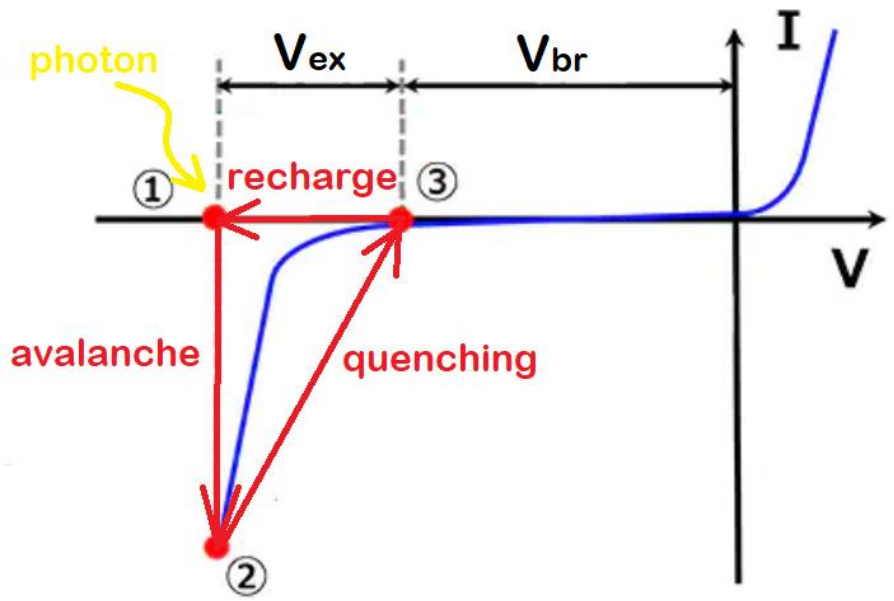
- Control circuits
- Read-out amplifiers

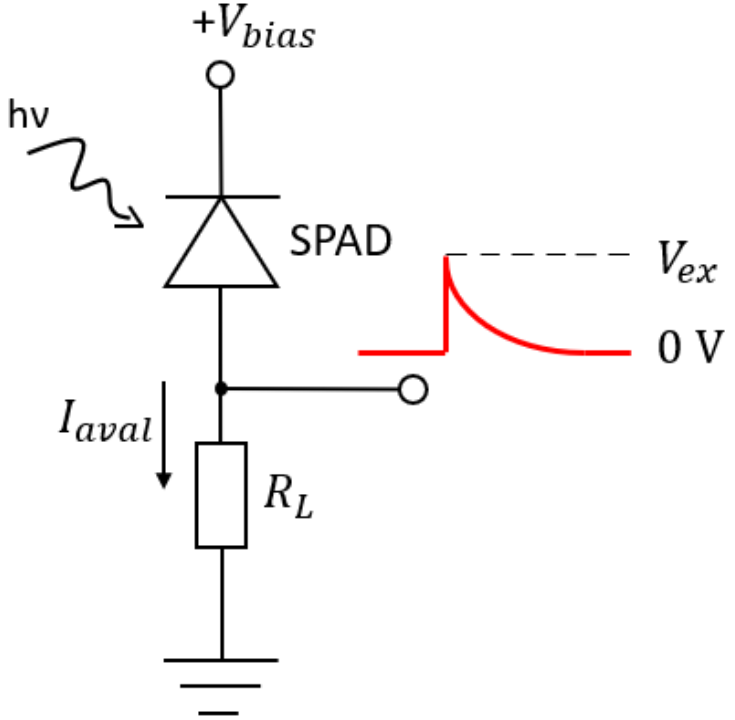
SPAD regime:

- Quenching circuits
- Signal processing circuits

CASSIA – SPAD regime

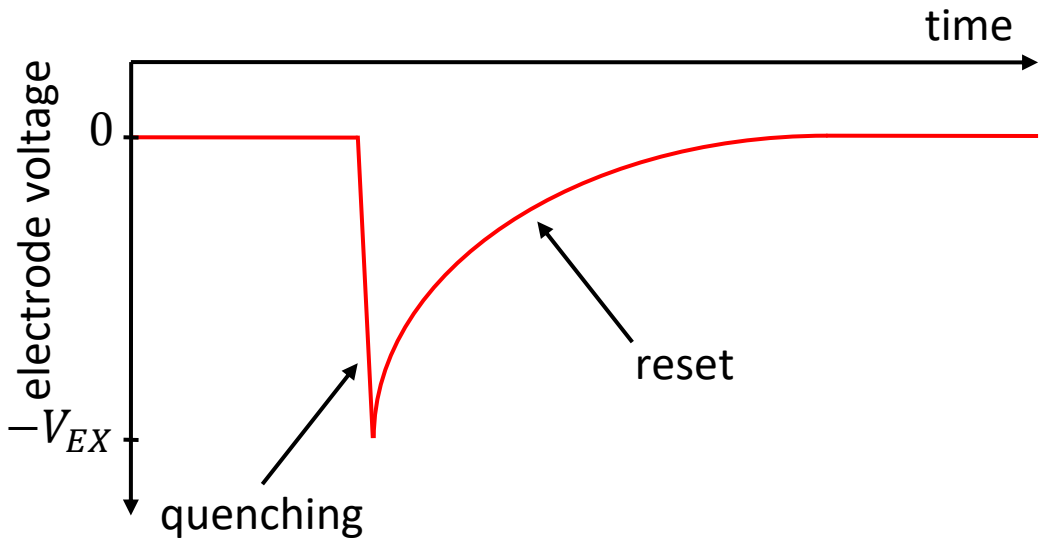
- biased above V_{BR} by excess voltage V_{EX} (Geiger mode)
- single carrier can cause avalanche multiplication and high avalanche current I_{aval}
- voltage drop on load resistor R_L reduces diode voltage below V_{BR} and quenches avalanche

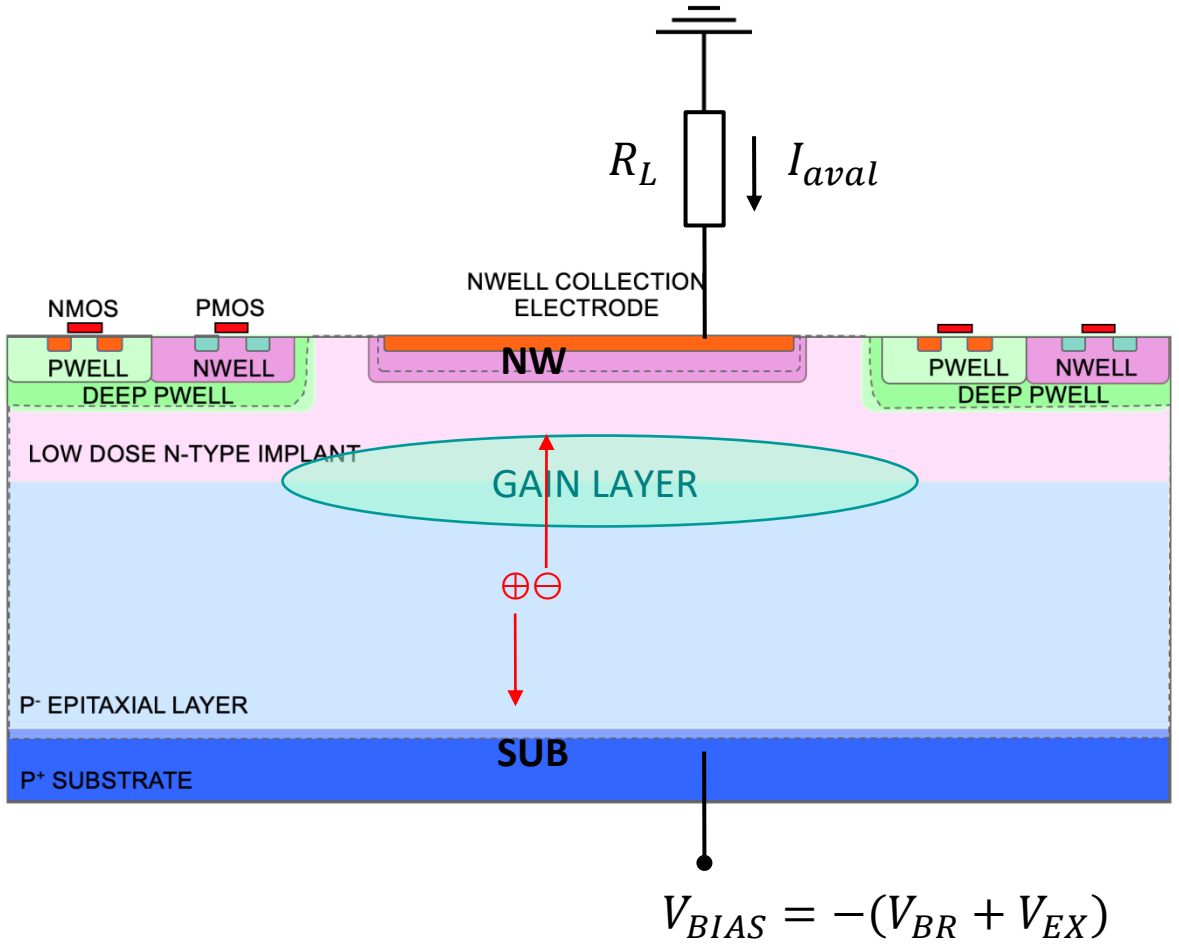




CASSIA – SPAD regime

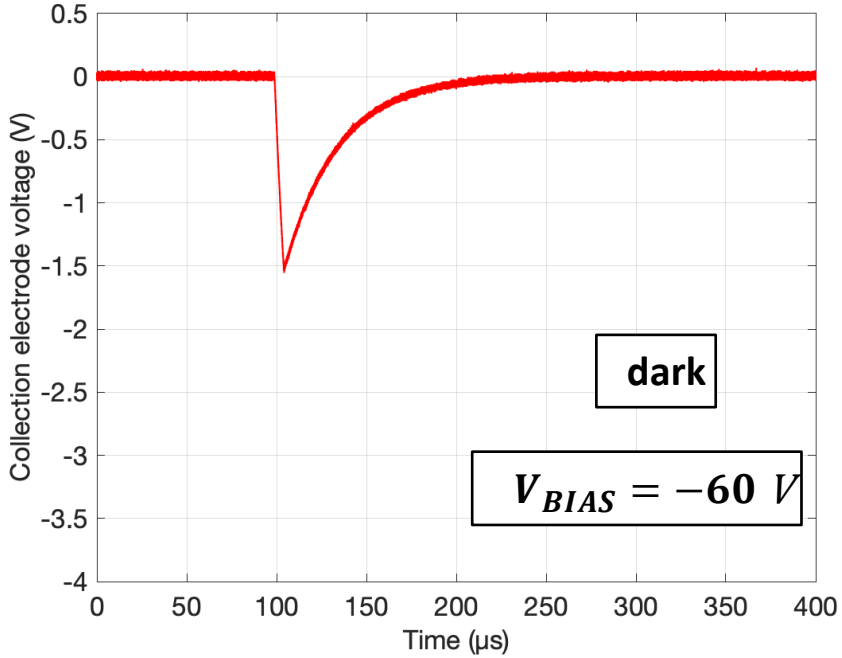
- Passive quenching
- N-collection electrode – negative pulse
- Without illumination: Dark Count Rate (DCR)
- **DCR:**
  - Shockley-Read-Hall (SHR) recombination dominant
  - Minimum sensitivity (noise limit)

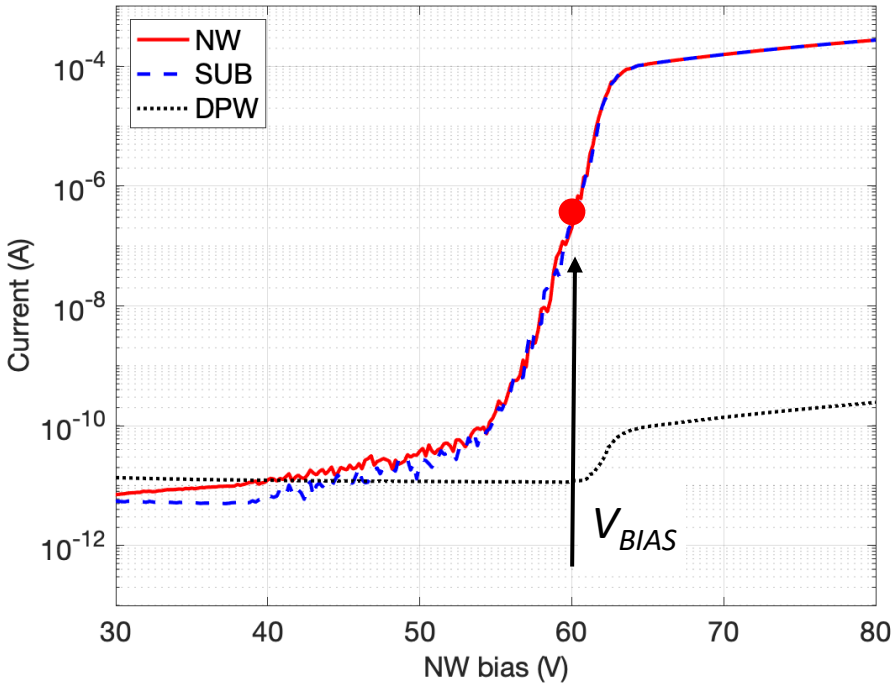


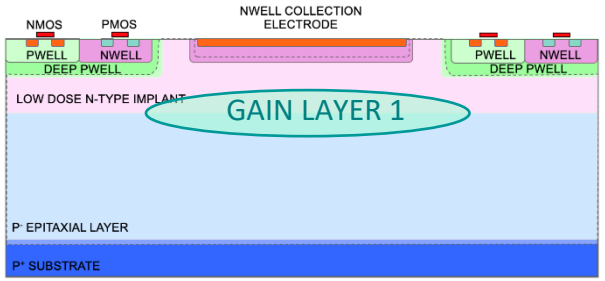


CASSIA – SPAD regime, Gain layer 1

- External quenching resistor: $R_L = 150\ k\Omega$
- On-chip measurements:







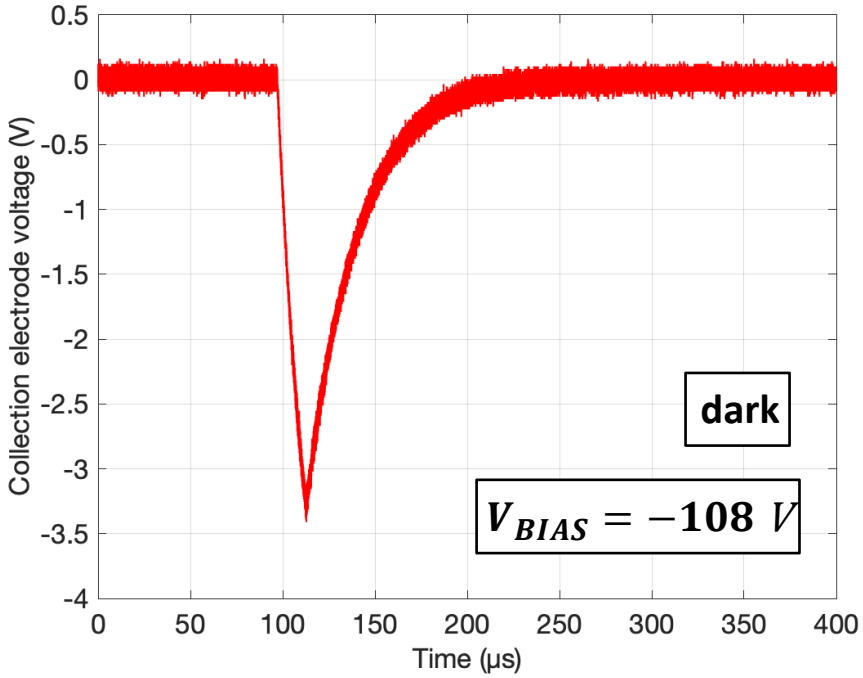
Gain layer 1

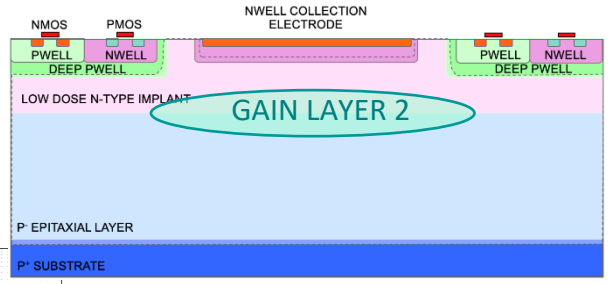
- IV_{BIAS}I= 60 V

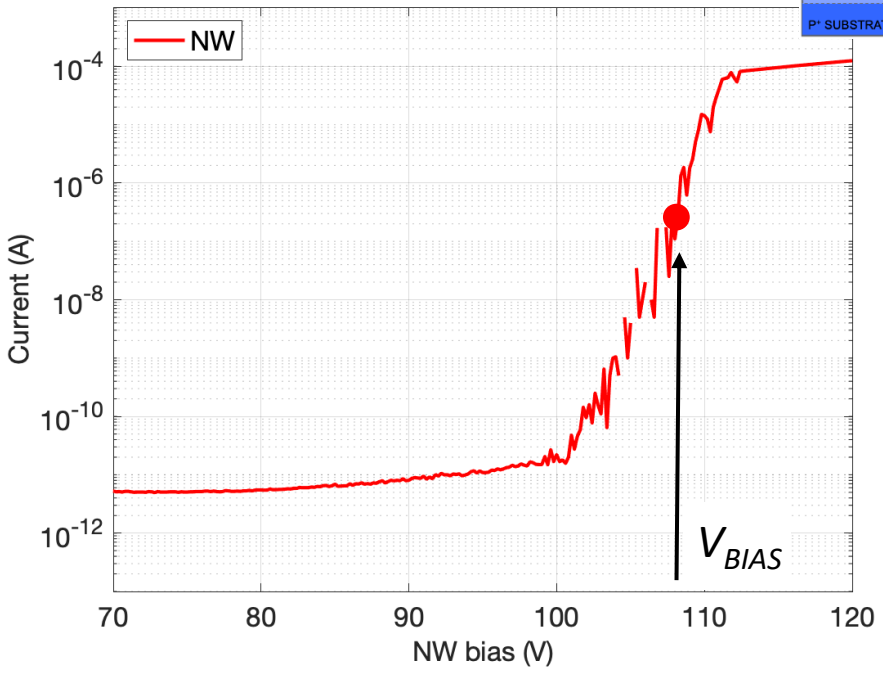
(~5 V above onset of multiplication)

CASSIA – SPAD regime, Gain layer 2

- External quenching resistor: $R_L = 150\ k\Omega$
- On-chip measurements:







Gain layer 2

- IV_{BIAS}I= 108 V

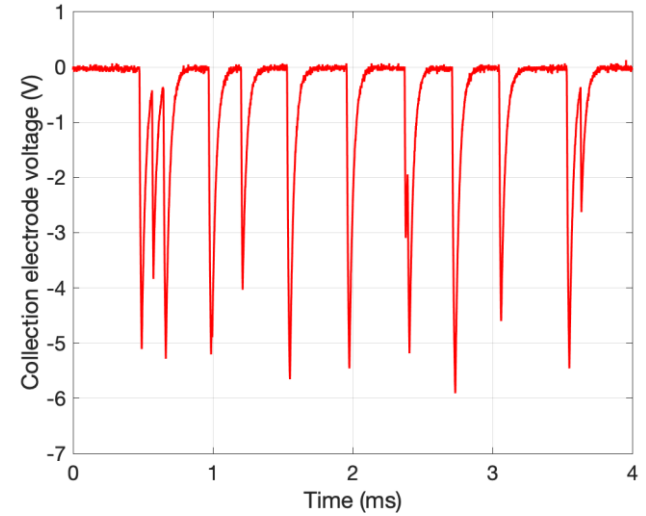
(~5 V above onset of multiplication)

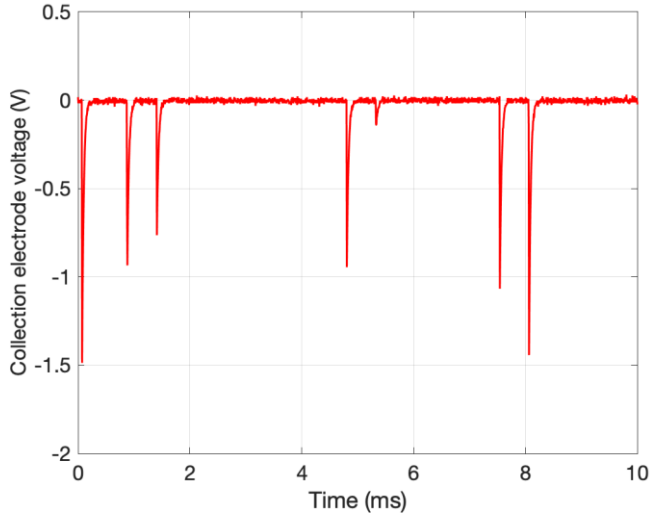
higher amplitude due to steeper breakdown?

CASSIA – SPAD regime, DCR

- counting the number of dark pulses for central pixels of matrices

Gain layer	(V)	DCR (Hz/µm²)	
		V_{EX1}	V_{EX2}
#1	55	2.03	16.59
#2	105	**0.061**	**0.084**



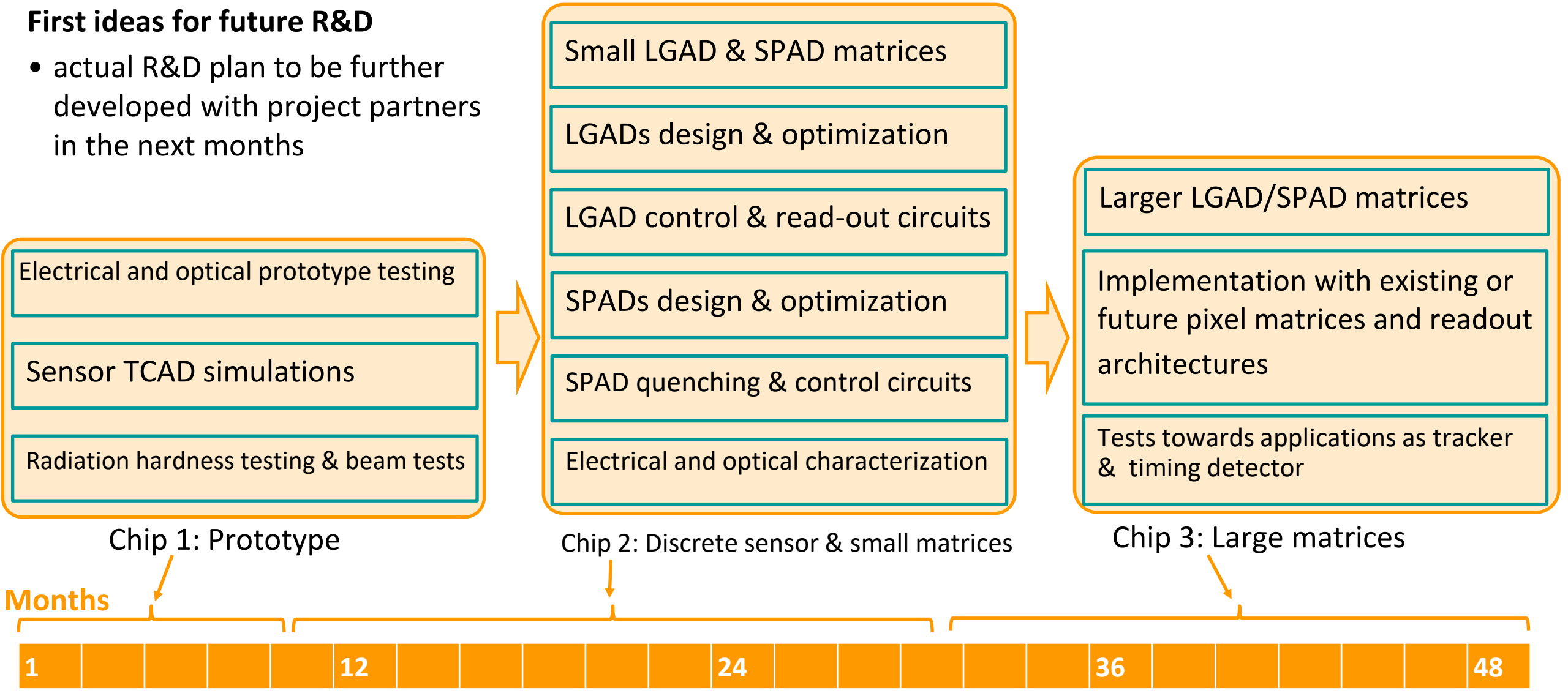


- only collection electrode/gain layer junction considered for calculation of active area (worst case)
- State-of-the-art DCR at 300 K with Gain layer 2
- Low-defect substrate in 180nm TJ CMOS technology

CASSIA – Proposal to DRD3 WG 1

First ideas for future R&D

- actual R&D plan to be further developed with project partners in the next months



CASSIA – Initial interests and project work areas

Initial ideas of different development contributions

- more refinement over next months
- develop milestone/deliverable plan together with project consortium

- Pixel design and simulation
- In-pixel electronics design
- Chip integration and verification
- Test system development
- Lab characterisations
- Irradiation studies
- Beam tests

Interests received form the following groups to participate in the project consortium

- CERN EP-ADE-TK
- University of Zagreb - FER, MiNEL
- Centre de Physique des Particules de Marseille (CPPM)
- Universite de Strasbourg (IPHC)
- Universität Bonn
- KEK and Kyushu University
- IIT Madras Chennai
- University of Glasgow

The project is open to further collaborators who wish to contribute to any of the work areas

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Summary

- In-pixel gain demonstrated in standard CMOS image technology
- Soft breakdown characteristics enables precise gain adjustment in wide voltage range
- Low dark current improves sensitivity
- Uniform light emission demonstrates avalanche multiplication in the active region
- Possibility of various implementation of gain layer

- ***Challenges:*** *fill factor, perimeter gain, series resistance, radiation hardness….*

- **With this project we would like to contribute to the R&D programme of DRD3 CMOS specifically with the development of sensors with internal gain to address future challenges in**
  - **high signal-to-noise ratio for low-power sensor designs**
  - **high time resolution in smaller pitch pixel matrices for future trackers and timing/time-tagging detectors**
  - **extending radiation hardness, …**