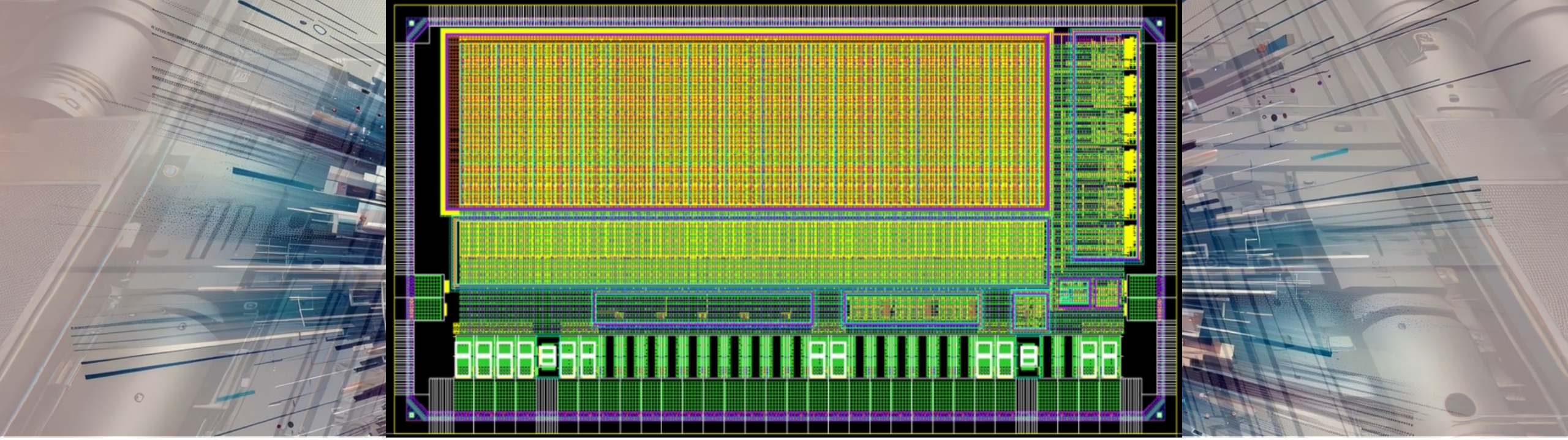


The H2M project: Porting the functionality of a hybrid readout chip into a monolithic 65 nm CMOS imaging process

Rafael Ballabriga, Eric Buschmann, Michael Campbell, Raimon Casanova Mohr, Dominik Dannheim, Ana Dorda, Finn Feindt, **Philipp Gadow**, Ingrid-Maria Gregor, Karsten Hansen, Yajun He, Lennart Huth, Iraklis Kremastiotis, Corentin Lemoine, Stefano Maffessanti, Larissa Mendes, Younes Otarid, Christian Reckleben, Sebastien Rettie, Manuel Alejandro del Rio Viera, Sara Ruiz Daza, Judith Schlaadt, Adriana Simancas, Walter Snoeys, Simon Spannagel, Tomas Vanat, Anastasiia Velyka, Gianpiero Vignola, Håkan Wennlöf

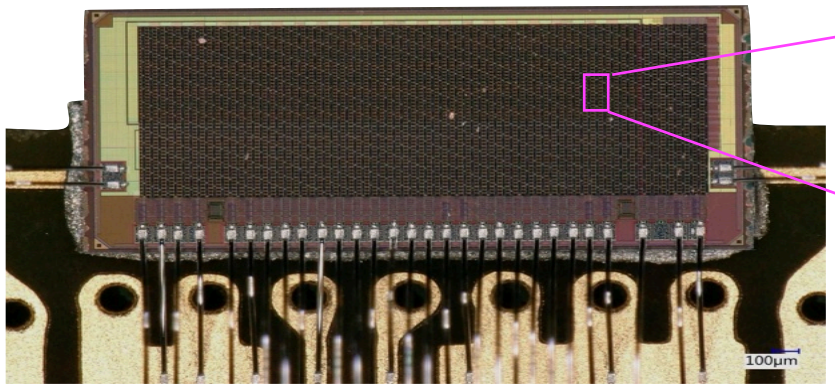
17.06.2024 1st DRD3 week on Solid State Detectors R&D

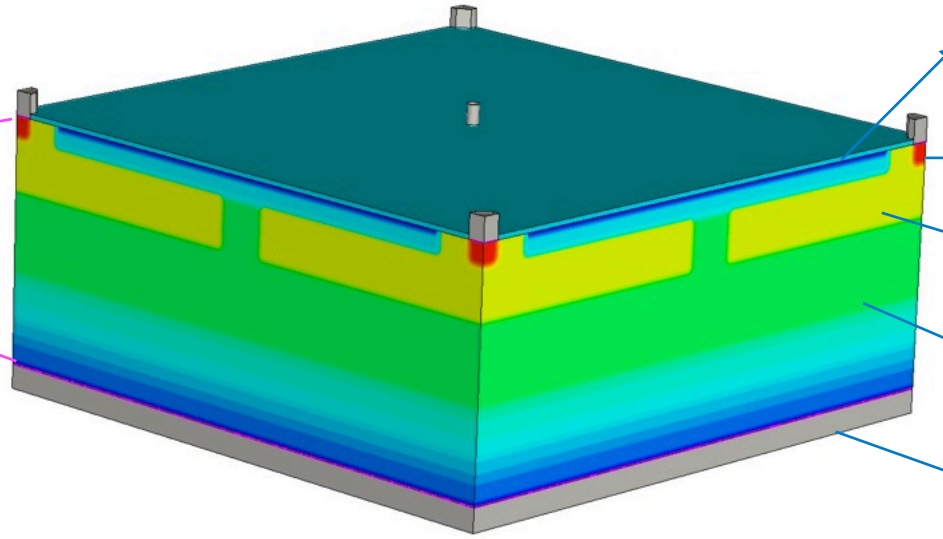
H2M (Hybrid-to-Monolithic)

- Ports a **hybrid pixel detector architecture into a monolithic chip**.
- **Digital-on-top** design workflow.
- Manufactured in a TPSCo **65 nm CMOS imaging process**.

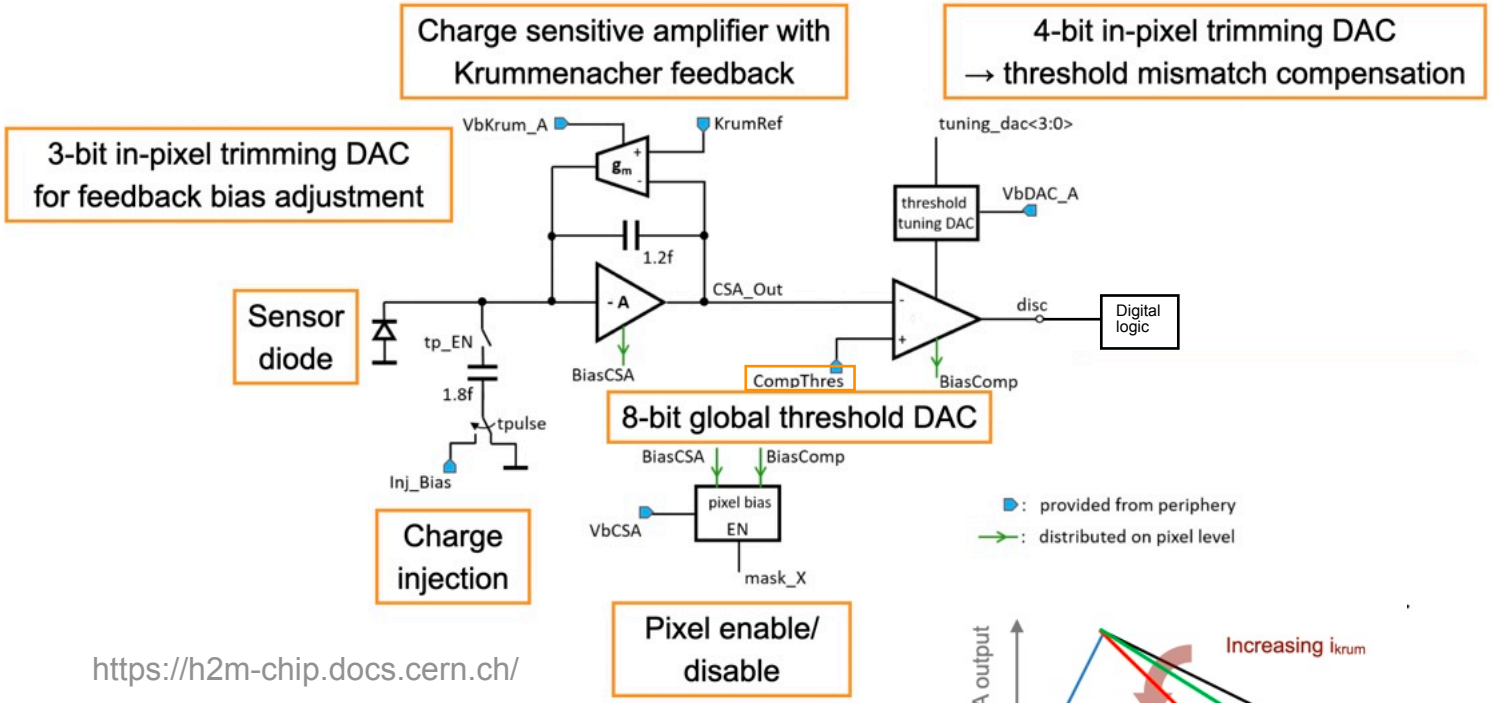
- **35 µm pixel pitch in 64x16 pixel matrix** (total sensitive area: 2.24 × 0.56 mm^2). Total thickness ~ 50 µm.
  ↪ (p-epitaxial layer ~ 10 µm)

- Analog and digital front-end per pixel.

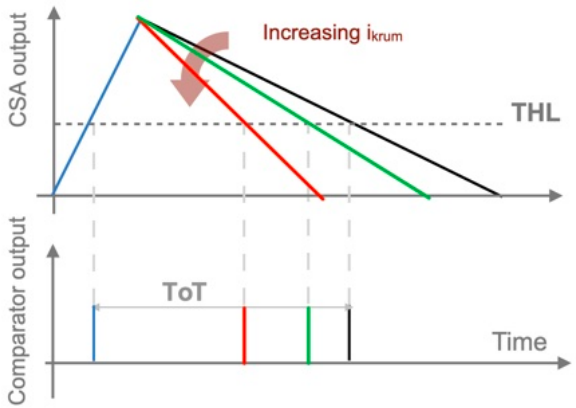




Analog front-end design

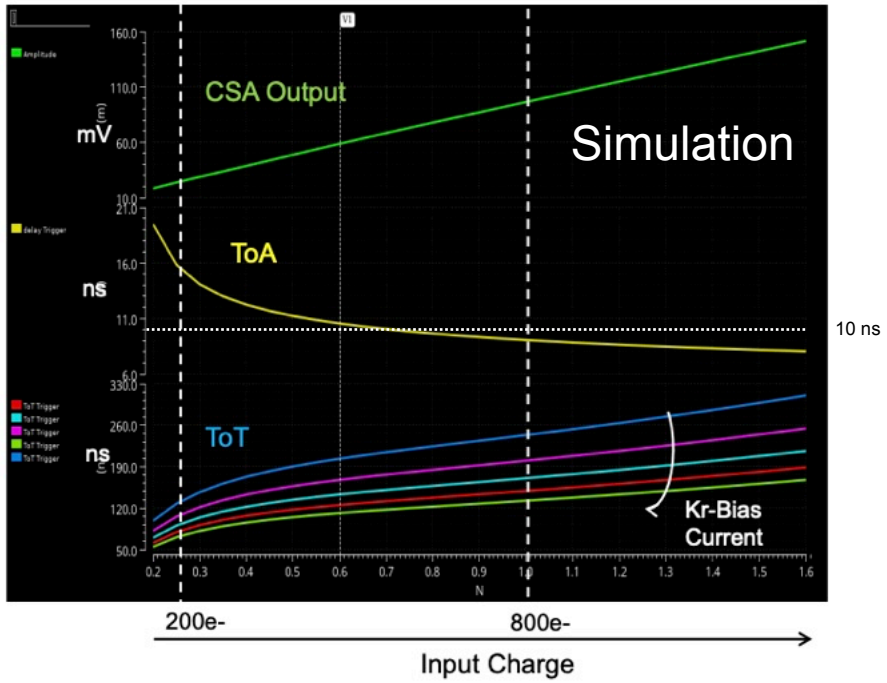


https://h2m-chip.docs.cern.ch/



Slope of falling edge tuned with Krummenacher feedback current (ikrum).

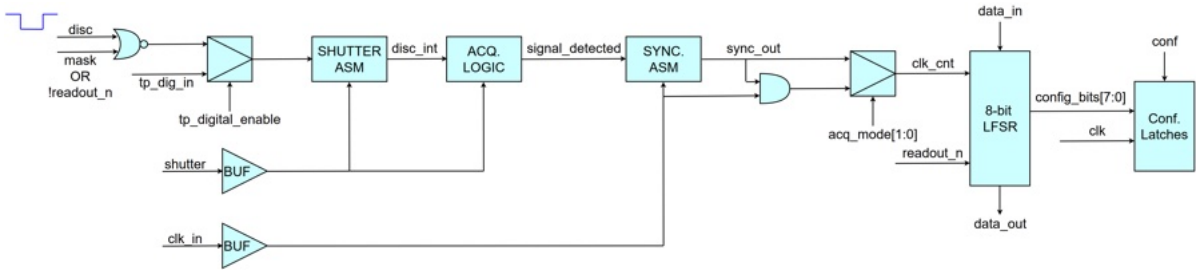
ToA/ToT as function of input charge



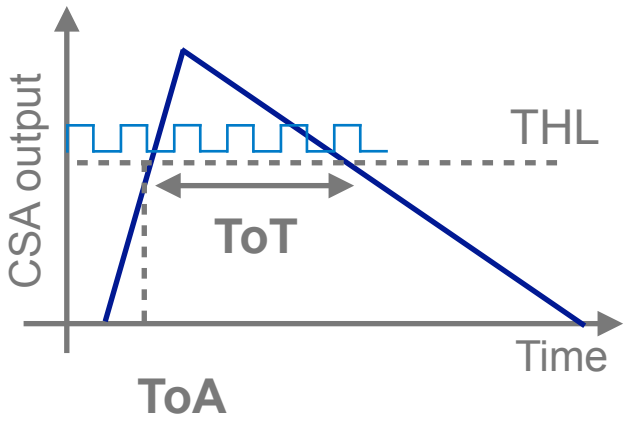
Timewalk below 10 ns for input charges larger than 400 electrons.

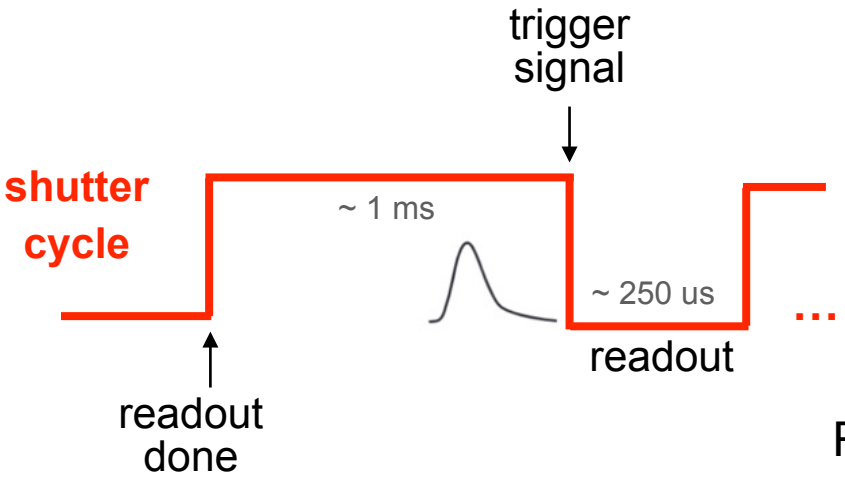
Data Acquisition

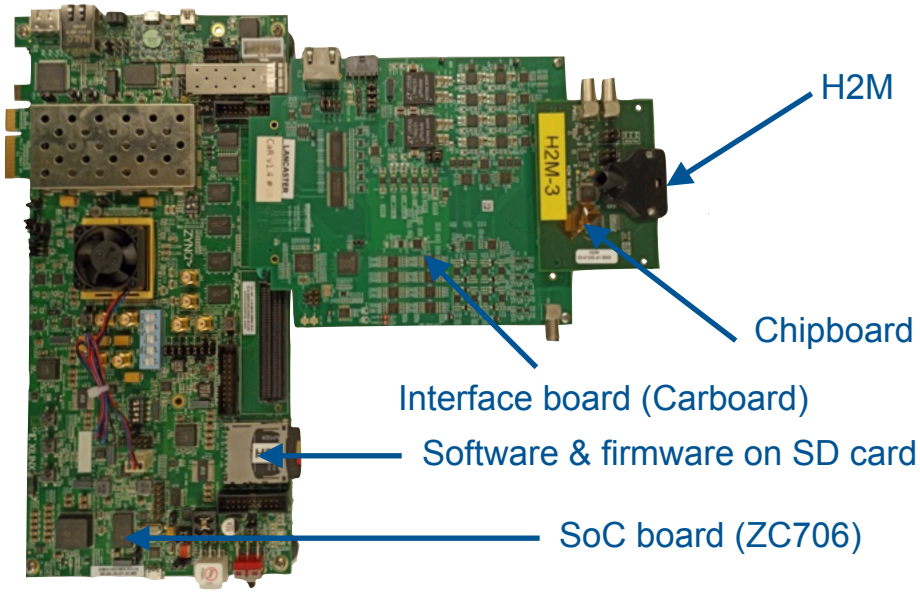
- **Non-simultaneous 4 acquisition modes** per pixel:
  - 8 bit ToT,
  - 8 bit ToA (100 MHz clock - 10 ns binning),
  - counting (#number of hits above threshold),
  - triggered.
- **Readout**: 40 MHz clock, frame-based without zero-suppression.



Digital Front-End



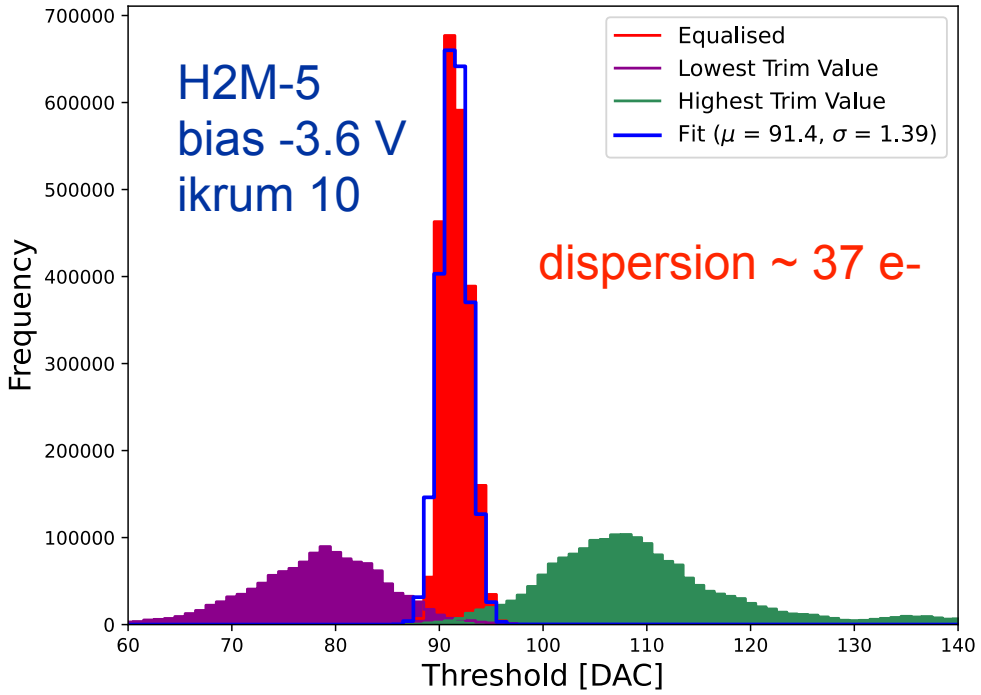


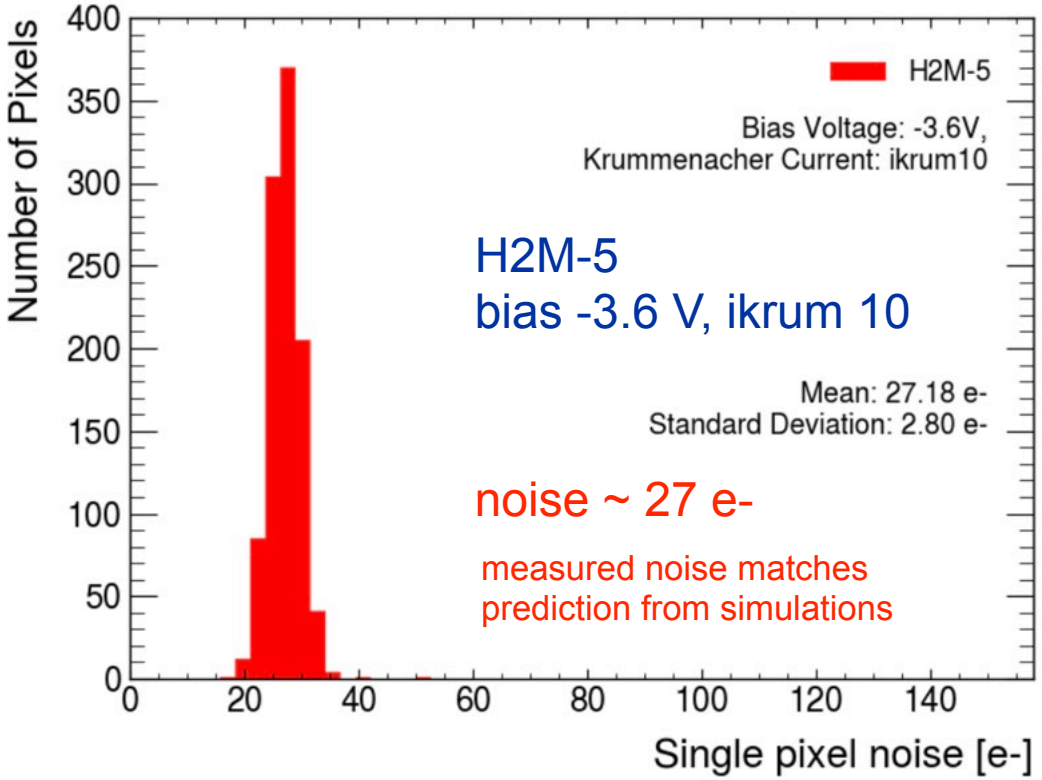


T. Vanat, TWEPP2019:100, 2020.

Readout system based on the **Caribou DAQ**.

Threshold equalisation and single-pixel noise

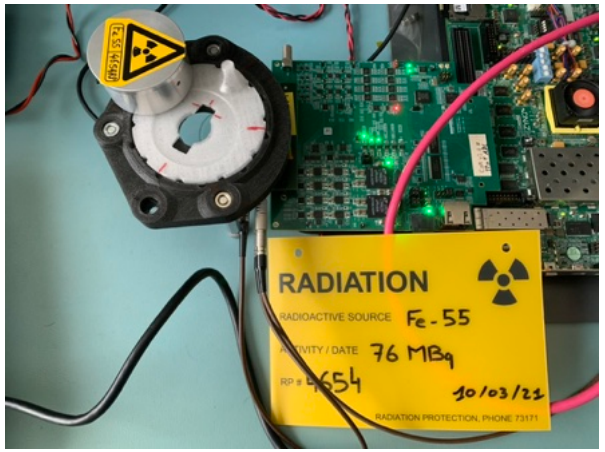




Equalisation of the hit detection threshold:

1) Threshold scan in counting mode for the 16 trimming values.
2) Determine the baseline for each pixel for each trimming value.
3) For each pixel, the trimming DAC is adjusted to the one with baseline closest to a fixed trimming target.
4) Single-pixel noise obtained from width of threshold turn-on curves.

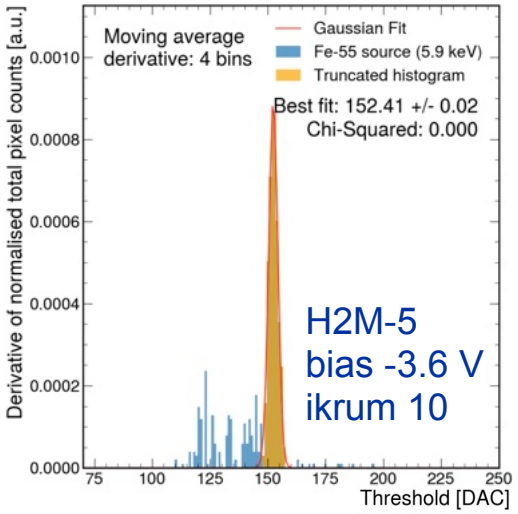
Threshold and ToT calibration

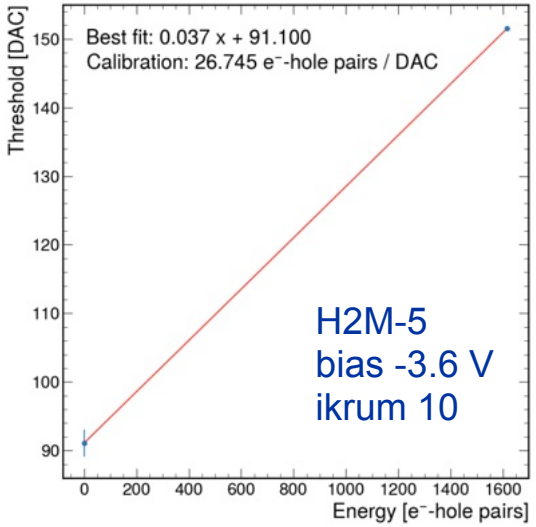


Source measurement (Fe-55) to calibrate the threshold into electrons.

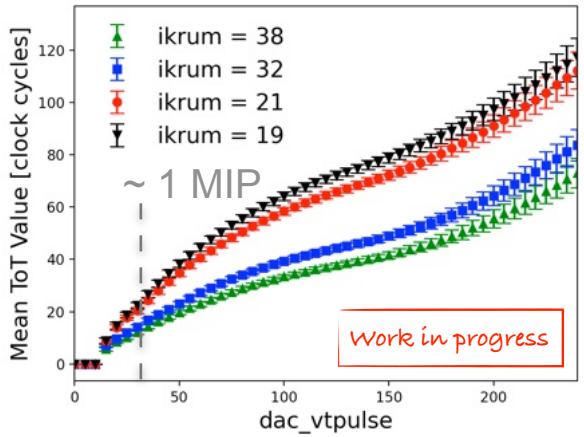
	H2M-2	H2M-3	H2M-4	H2M-5	design value
bias voltage [V]	-3.6	-3.6	-3.6	-3.6	-1.2
ikrum	21	21	21	21	21
calibration [e- / DAC](*)	27.4 ± 0.1	27.9 ± 0.1	26.1 ± 0.1	25.0 ± 0.1	~40 (**)
minimum operational threshold above baseline [e-]	329	390	*(n/a), will be added*	375	320

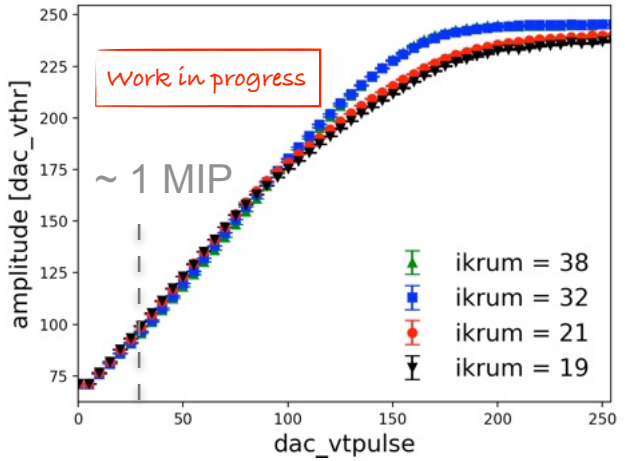
(*) Uncertainty on calibration represents statistical uncertainty from fit, preliminary estimate of systematic uncertainty of ~1 e- / DAC.
(**) Calculated value of 32e- / DAC from measured DAC_VTHR gain of ~3.91 mV / DAC and simulated CSA gain of ~120 mV / ke-.



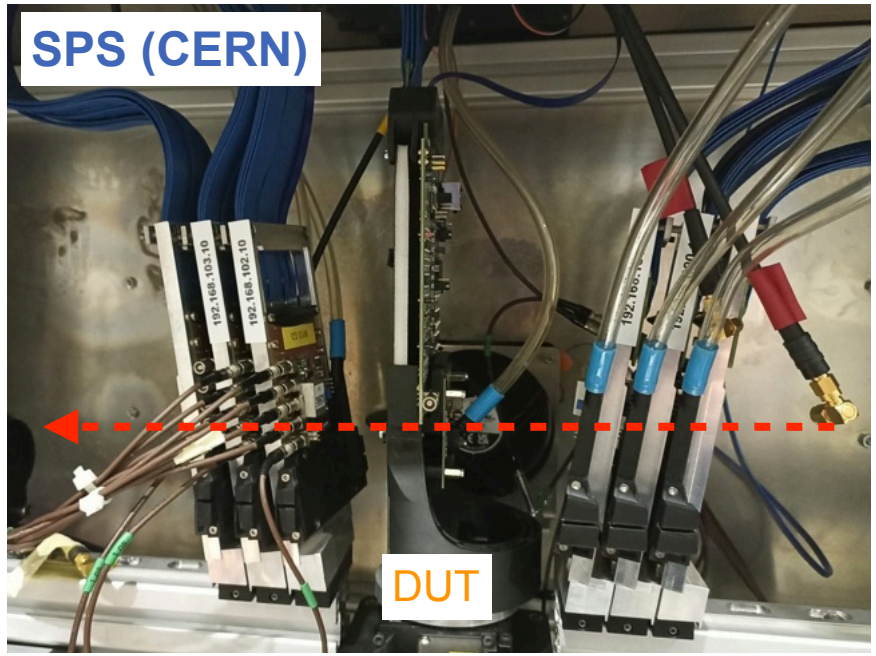


Test pulse measurements to find the relation between ToT and signal height per pixel.

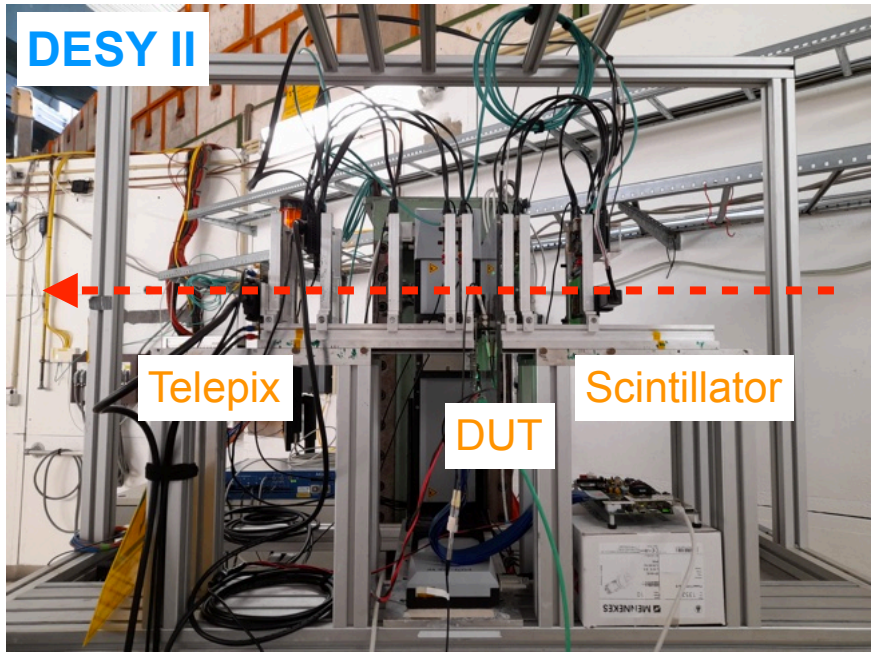




Test beam campaigns

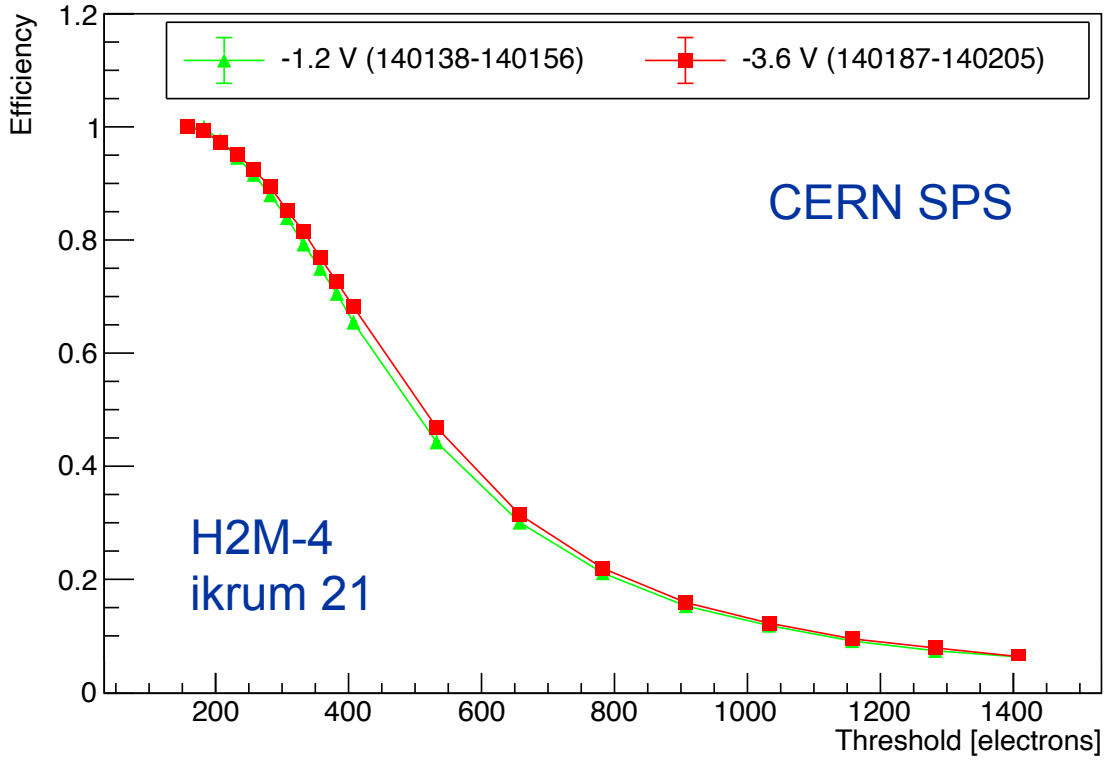


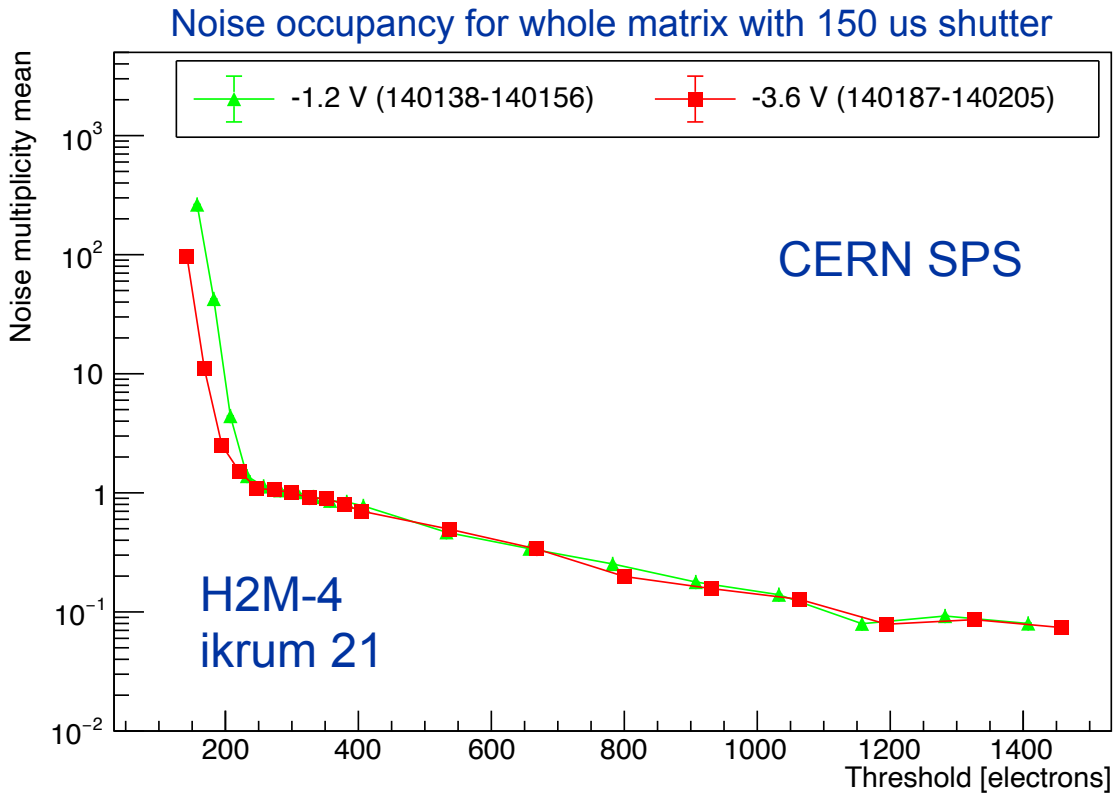
- H6 beam line, 120 GeV charged pions.
- **Timepix3 reference telescope.**
  - Pointing resolution ~ 1.5 µm,
  - Track time resolution ~ 1 ns,
  - Continuous readout with 150 us (2.56 us) shutter duration for ToT (ToA) mode.



- Beamline 22, electron beam ~4.8 GeV.
- **ALPIDE reference telescope.**
  - Pointing resolution ~ 3 µm
- Scintillator & Telepix used as region-of-interest triggers (~5ns resolution).

Efficiency and fake hit rate



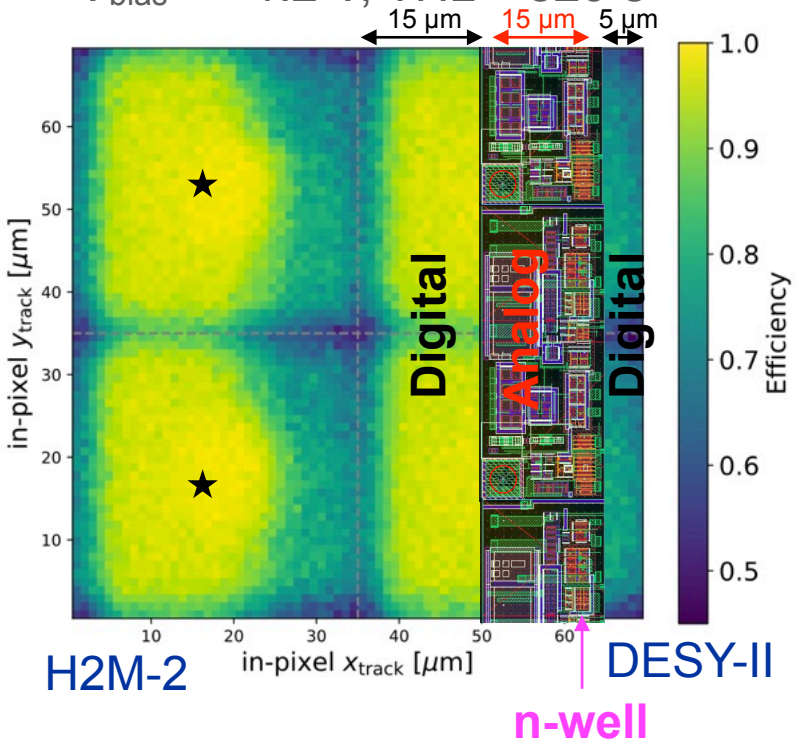


- **Expected efficiency** and **fake-hit rate** shown as function of threshold (THL).
- Significant noise contribution below 7 DACs (~200 electrons).
- Efficiency for "noise-free" operation: >99.1%.

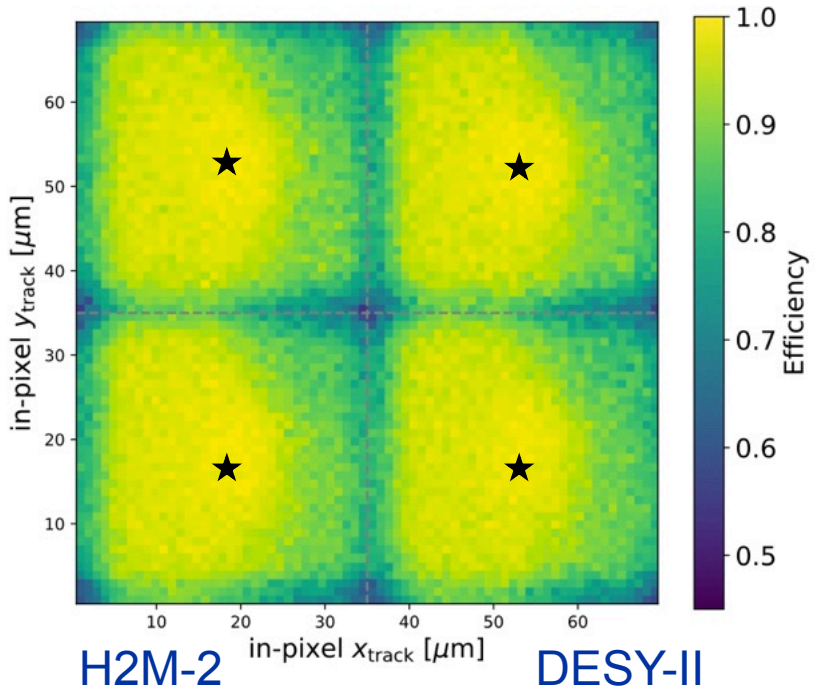
In-pixel efficiency map

★ Collection electrode

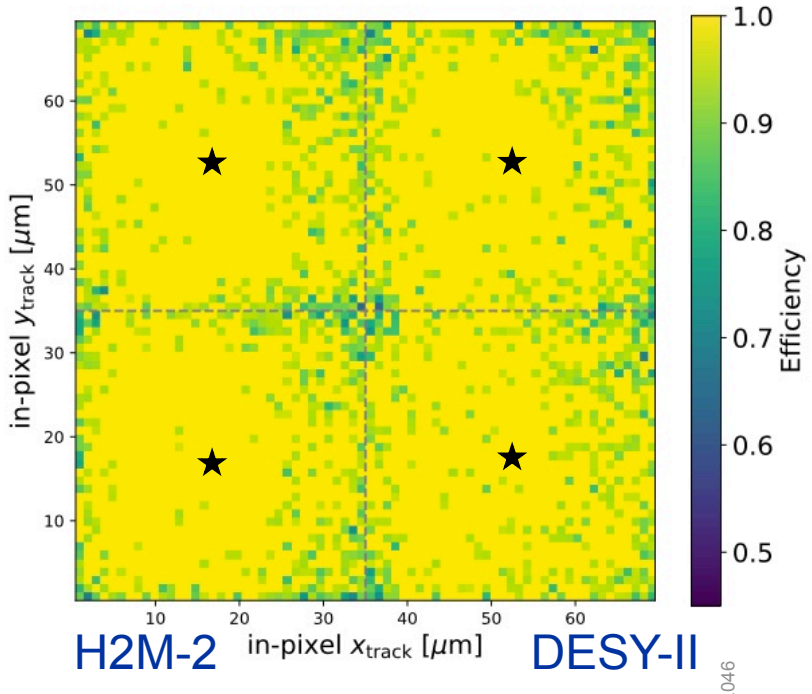
V_{bias} = - 1.2 V, THL ≈ 520 e⁻



V_{bias} = - 3.6 V, THL ≈ 520 e⁻

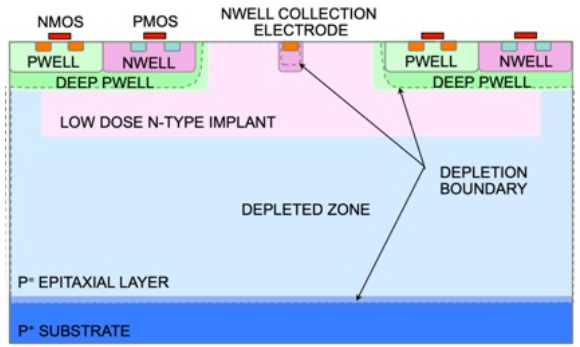


V_{bias} = - 3.6 V, THL ≈ 400 e⁻



Non-uniform in-pixel efficiency:

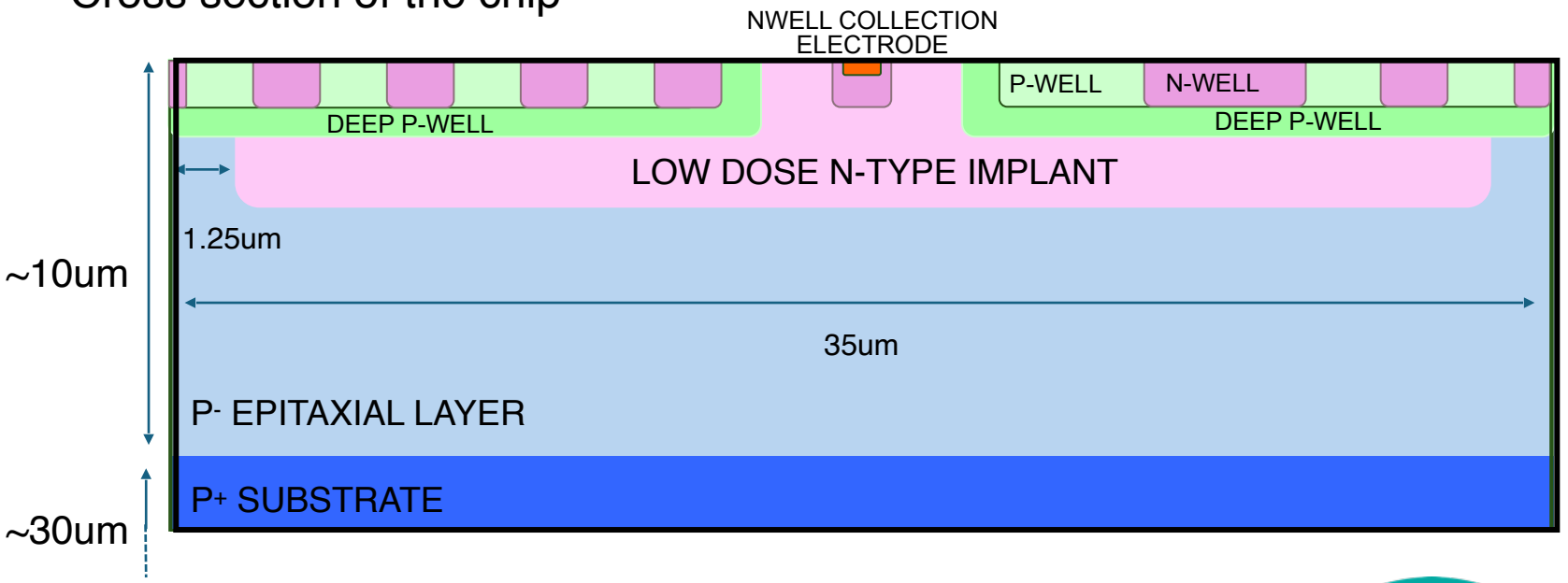
- Related to the size and location of the n-wells of the analog circuitry.
- Mitigated at larger V_{bias} and lower thresholds.
- Additionally, effects of fast front-end and large pixel size.



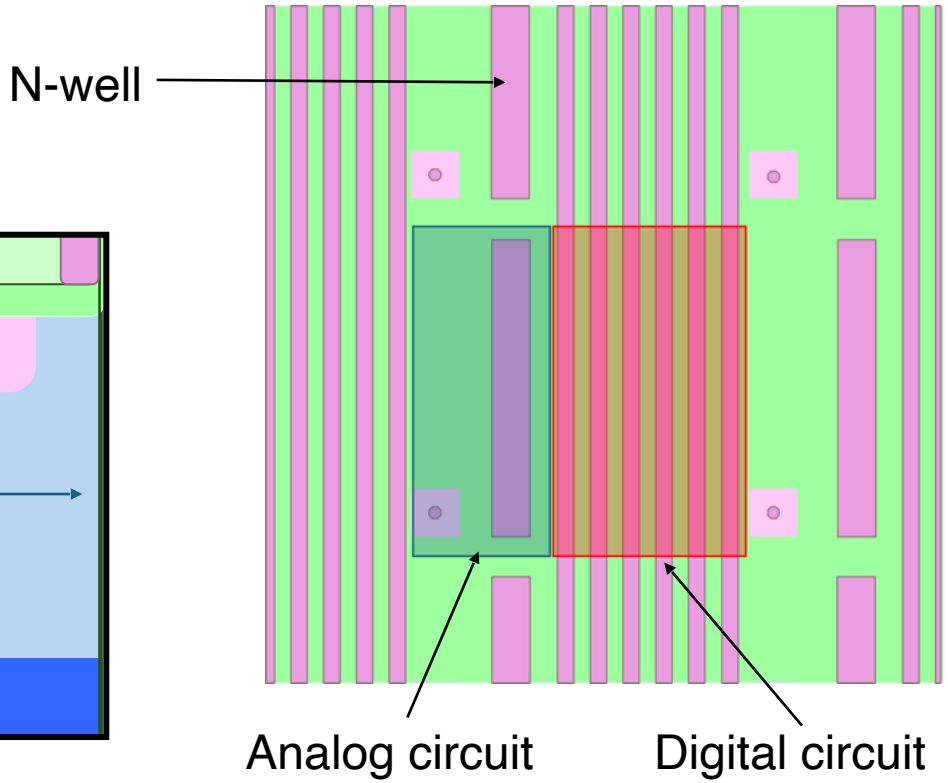
W. Snoeys, DOI:10.1016/j.nima.2017.07.046

Simulation workflow

Cross section of the chip



Layout of the H2M (top view)



Sensor structure

Sentaurus TCAD

SYNOPSYS

Electric field

ap² allpix squared

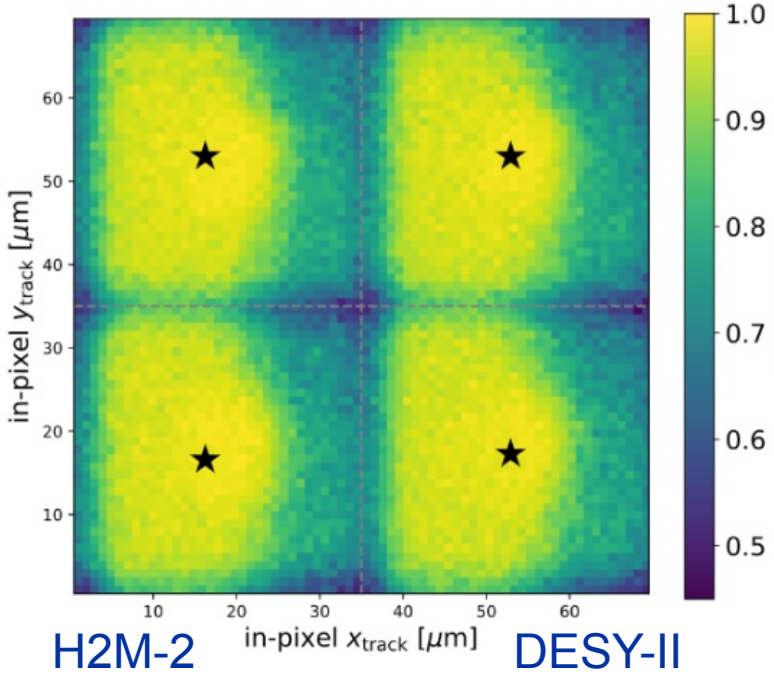
Pixel hits

Analysis

Comparison between measurements and simulation

Test beam

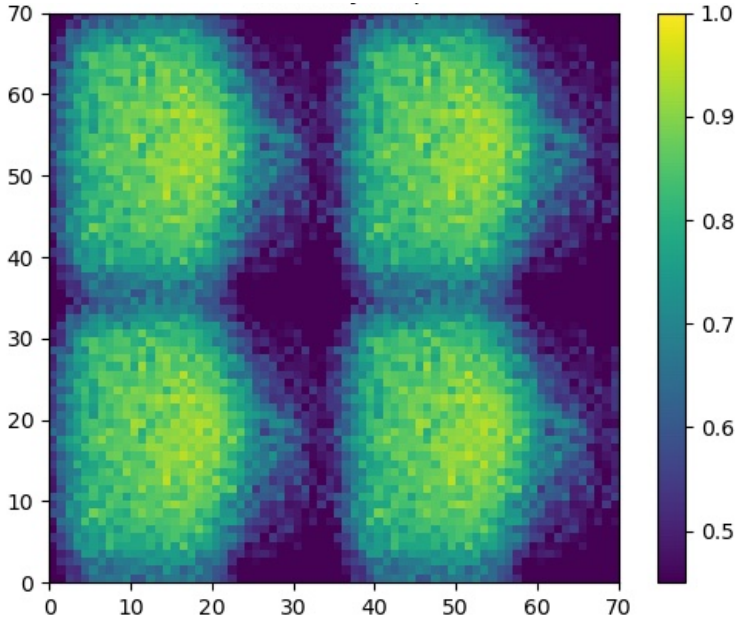
Vsub = -1.2V, THLD=520e-



H2M-2 DESY-II

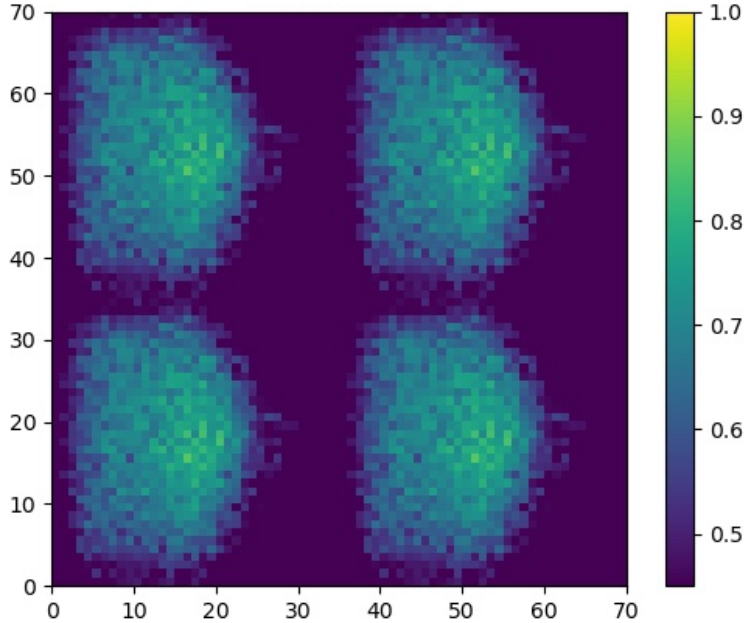
Simulations

Vsub = -1.2V, THLD=400e-



Simulation

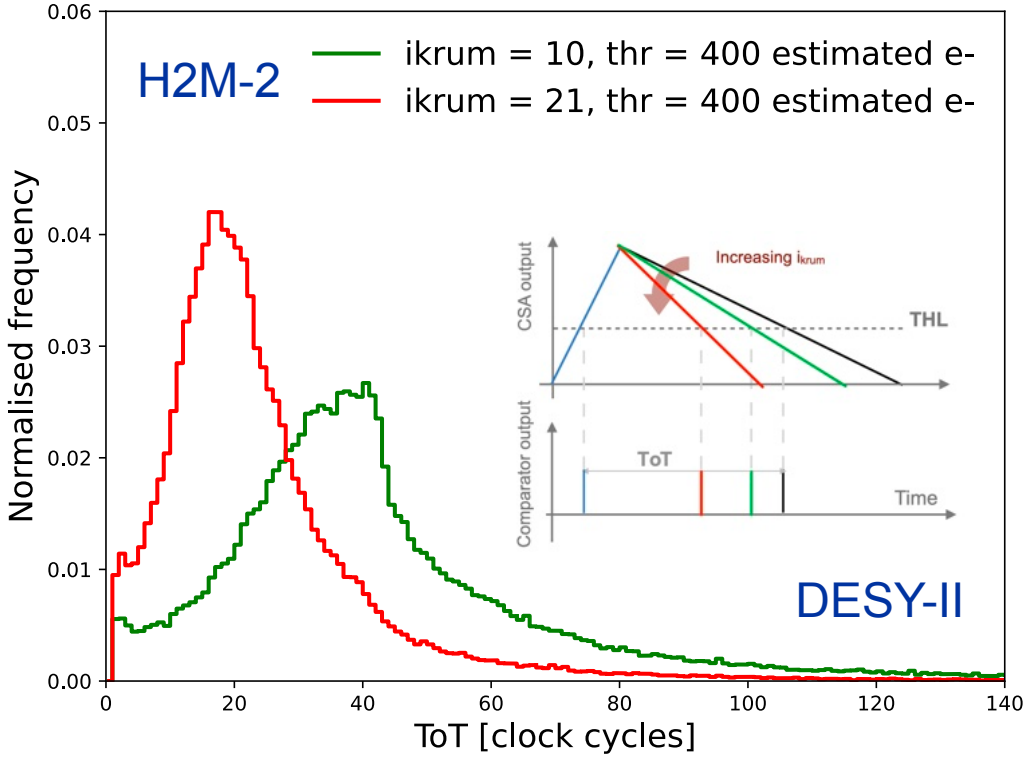
Vsub = -1.2V, THLD=520e-



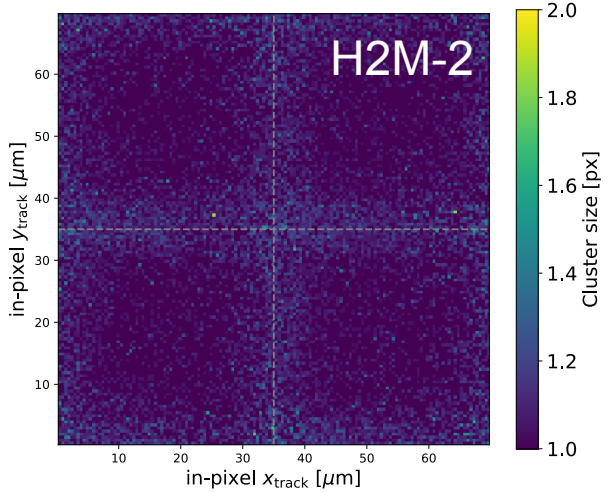
Simulation

Good qualitative matching of the pattern. Current simulation predicts too low efficiency: quantitative matching is ongoing work.

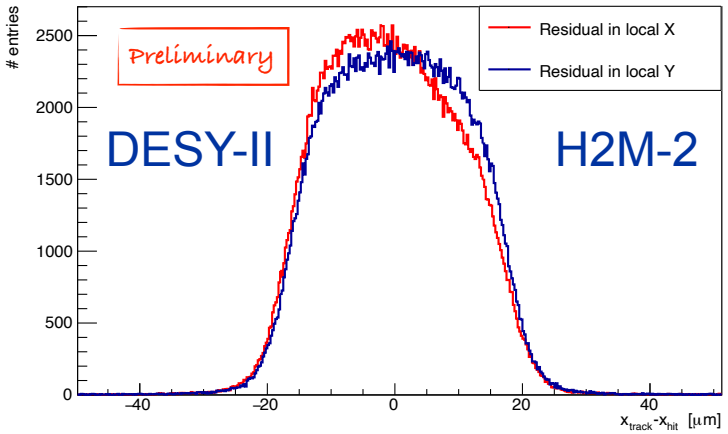
ToT, cluster size and spatial resolution distributions



Cluster size



Spatial resolution

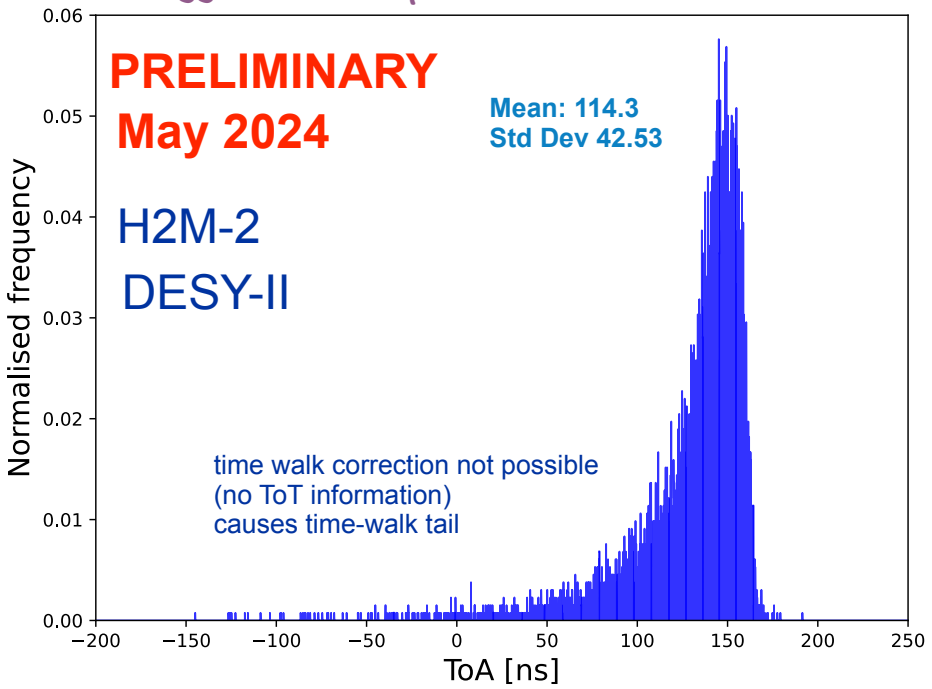


ToT measurement, threshold ~ 400 electrons

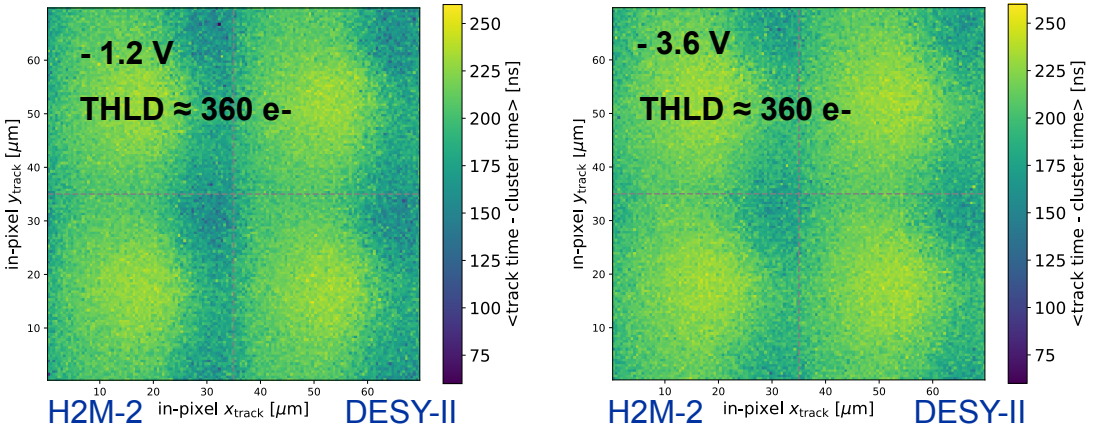
- Spatial resolution and cluster size dominated by the ~35 μm pitch and the high threshold.
- Asymmetric residuals in X due to the low-efficiency part.

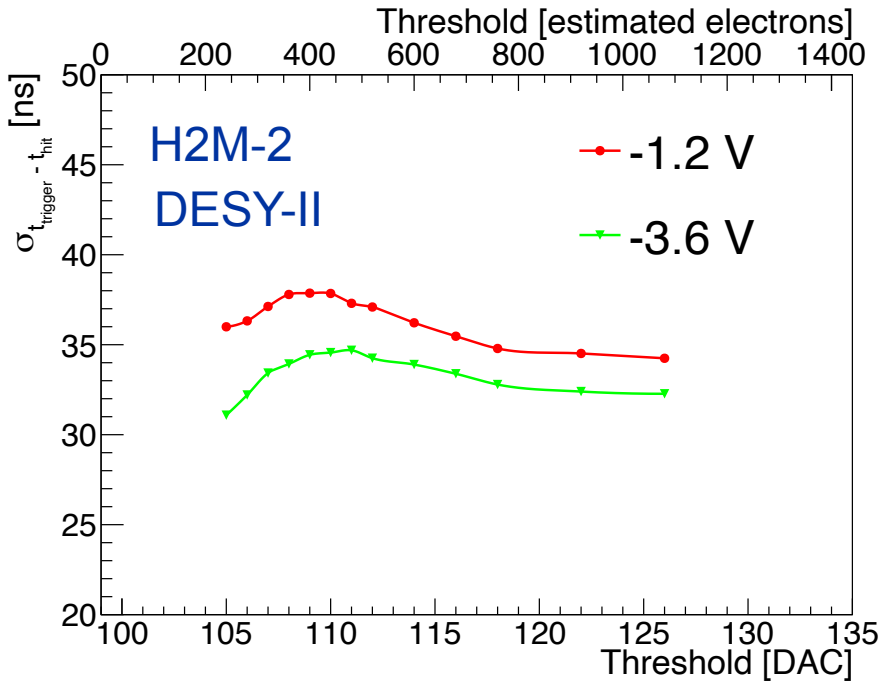
Time resolution (ToA)

Trigger time stamp with a resolution of ~ 5 ns

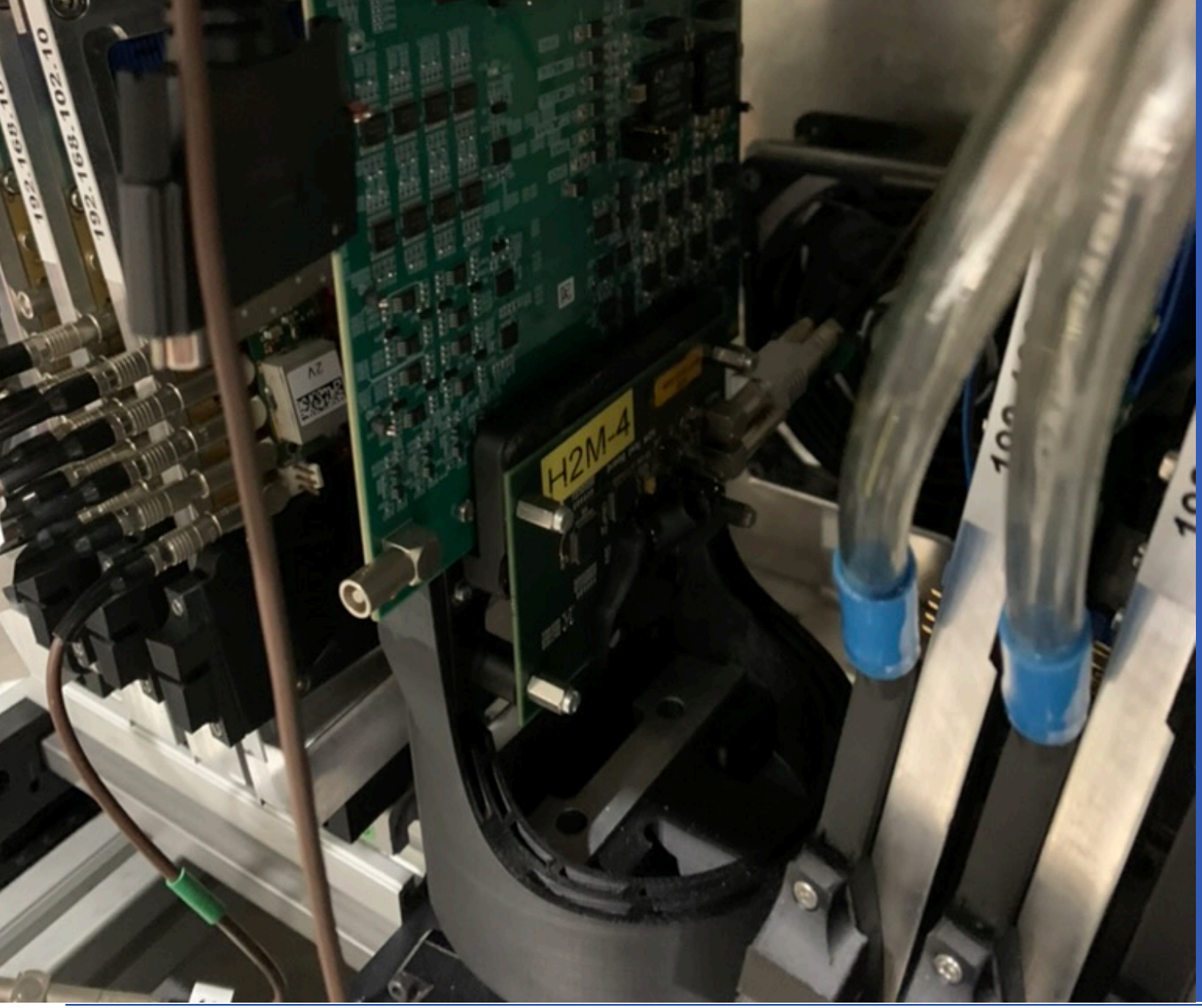


large impact of in-pixel position on mean ToA





- **Better timing resolution for -3.6 V than -1.2 V.**
  Due to more uniform charge-collection time across the pixel cell.
- **Better timing at low thresholds.**
  Above ~400 electrons, better time resolution due to the small efficiency region around the collection electrode with fast charge collection.



Conclusions

Fully functional digital-on-top sensor in a 65 nm CIS.

Calibration and characterisation of performance with laboratory and test beam measurements.

- Fully efficient operation in test beam:
  - 27 e- noise, 200 e- minimum threshold, >99.1% efficiency.
- Impact of n-wells on charge-collection efficiency observed and qualitatively confirmed by simulations.
- Timing performance dominated by sensor effects? > ~30 ns.

Outlook: investigating the possibility of backside-thinning the chips from 50 um to <~30 um, to explore impact of thickness on performance.

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