R&D of a MAPS based Inner Tracker for the STCF

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On behalf of the STCF MAPS working group

1st DRD3 week on Solid State Detectors R&D
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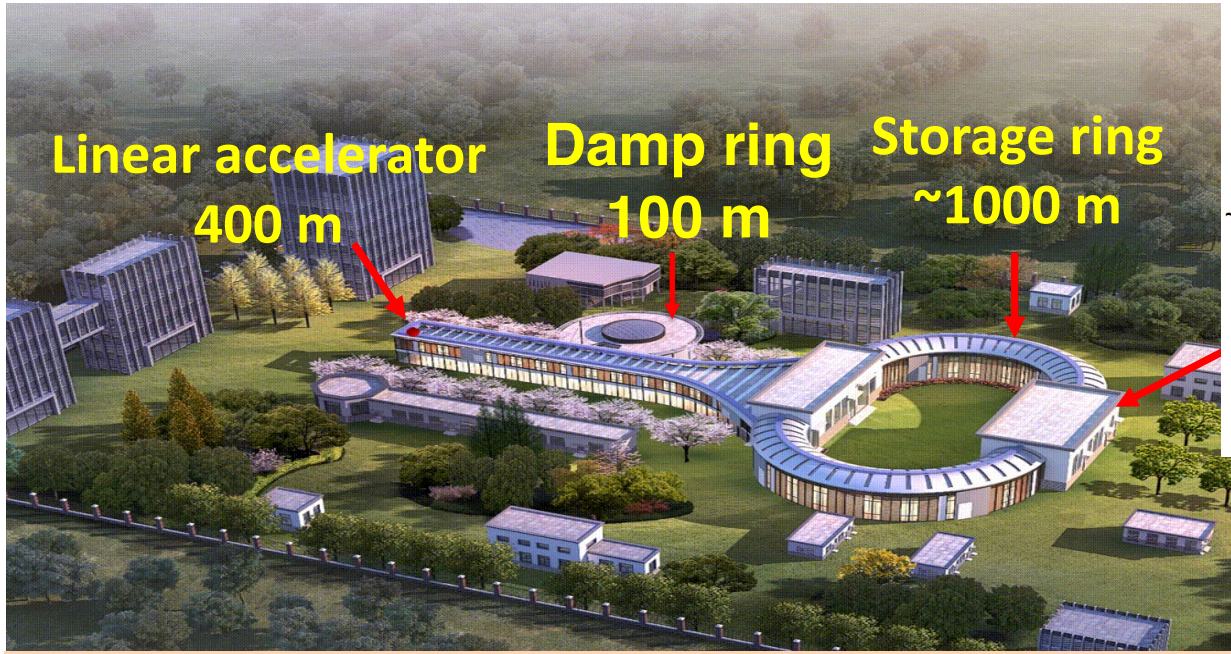
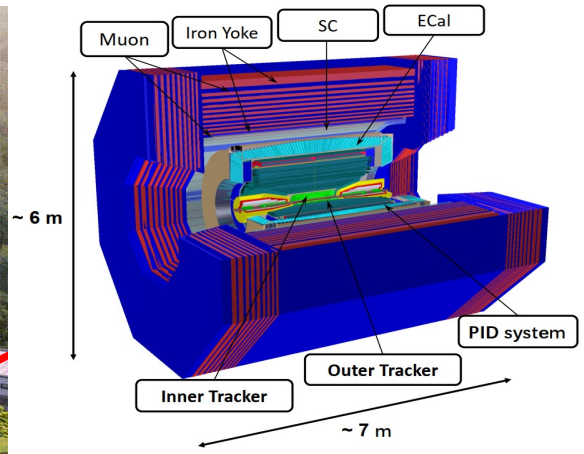
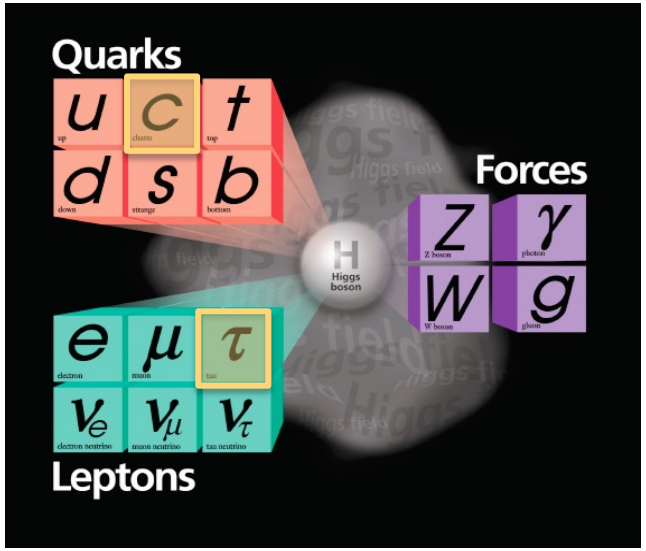
Super Tau Charm Facility (STCF)





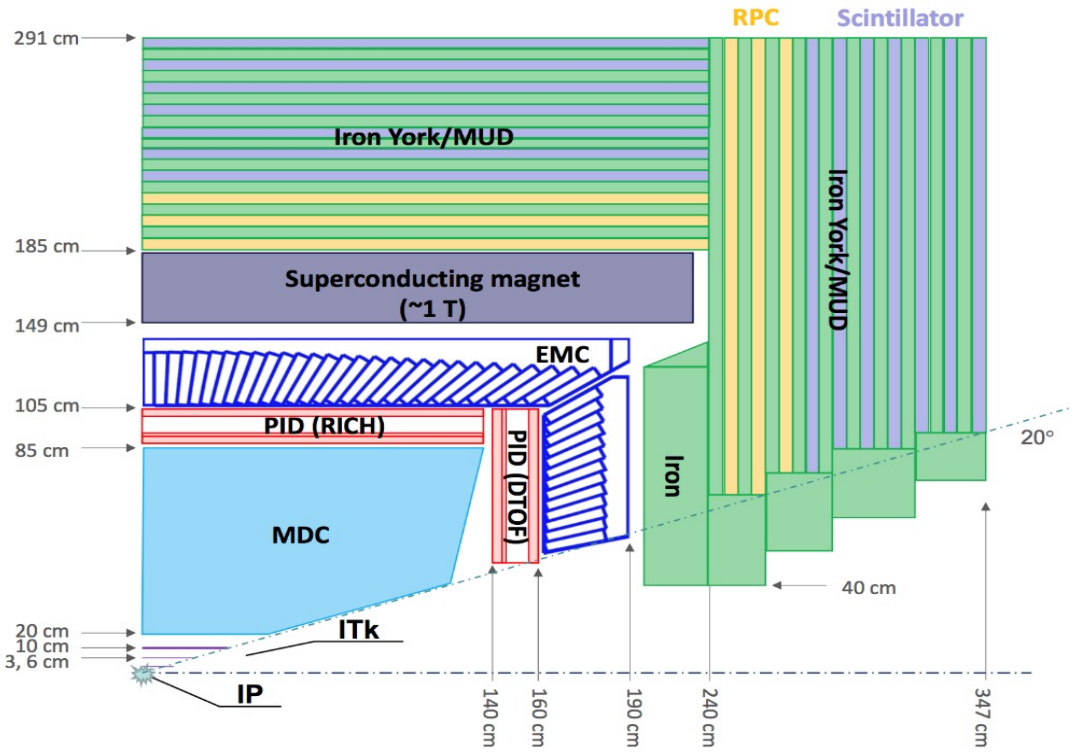
Detector



- Energy range: E_{cm}=2-7GeV
- Peak luminosity >0.5×10^{35} cm^{-2} s^{-1} at 4 GeV
- Potential for an upgrade to increase lumi. and realize polarized beam

- 1 ab^{-1} data expected per year
- Generate an unprecedentedly large number of τ leptons, particles made of c quarks
- Important playground for study of QCD, exotic hadrons, flavor and search for new physics

Conceptual design



Solid angle coverage: 93%·4π (polar angle: 20°~160°)

Inner tracker(ITK)

- <0.35%X_0/layer
- σ_{xy}<100μm

Main drift chamber(MDC)

- σ_{xy} < 130μm
- σ_p/p~ 0.5% @ 1GeV
- dE/dx ~ 6%

Particle identification(PID)

- π/K (K/p) 3~4σ sepa. up to 2 GeV/c

Electromagnetic calorimeter(EMC)

- E range : 0.025~3.5 GeV
- σ_E @ 1GeV
  - Barrel 2.5%; Endcap 4.0%
- Pos. res. : 5 mm

Muon detector(MUD)

- 0.4 ~ 2.0 GeV
- π suppression > 30

FRONTIERS OF PHYSICS

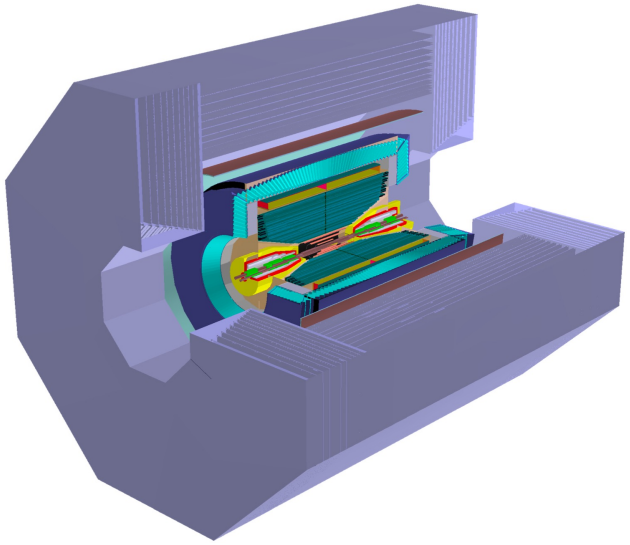
REPORT
Volume 19 / Issue 1 / 14701 / 2024

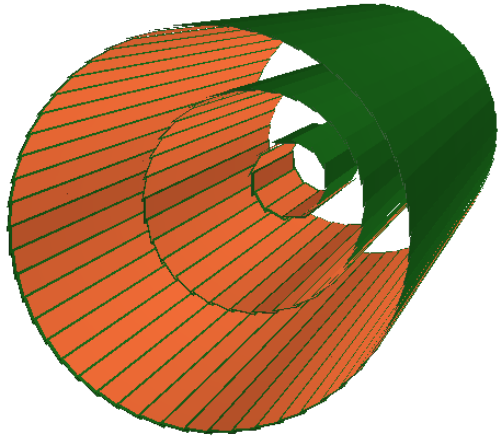
STCF conceptual design report (Volume 1): Physics & detector

Front. Phys. 19, 14701 (2024)

Conceptual design of the MAPS tracker

- Physics requirements of the Inner Tracker:
  - Tracking efficiency: >99% @ $p_T > 0.3\ GeV$; >90% @ $p_T > 0.1\ GeV$
- A preliminary design of the MAPS based Inner Tracker (ITKM)
  - Three layers of silicon pixel detectors, with radii of 36mm, 98mm, 160mm (beam pipe: 30mm)
  - Acceptance: polar angle of 20°~160°
- Total area: 1.3m^2





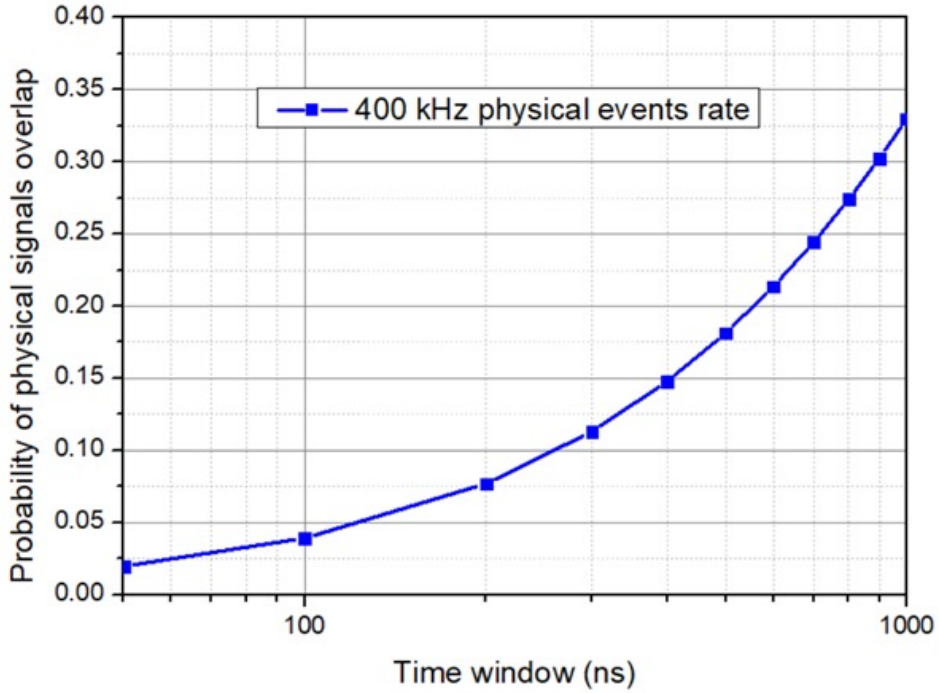
Layer	Radius (mm)	Length (cm)	Area (cm^2)
1	36	19.8	447.5
2	98	53.9	3315.9
3	160	87.9	8838.6

Geometry/layout still being optimized
Might extend to 4 or more layers

Design targets

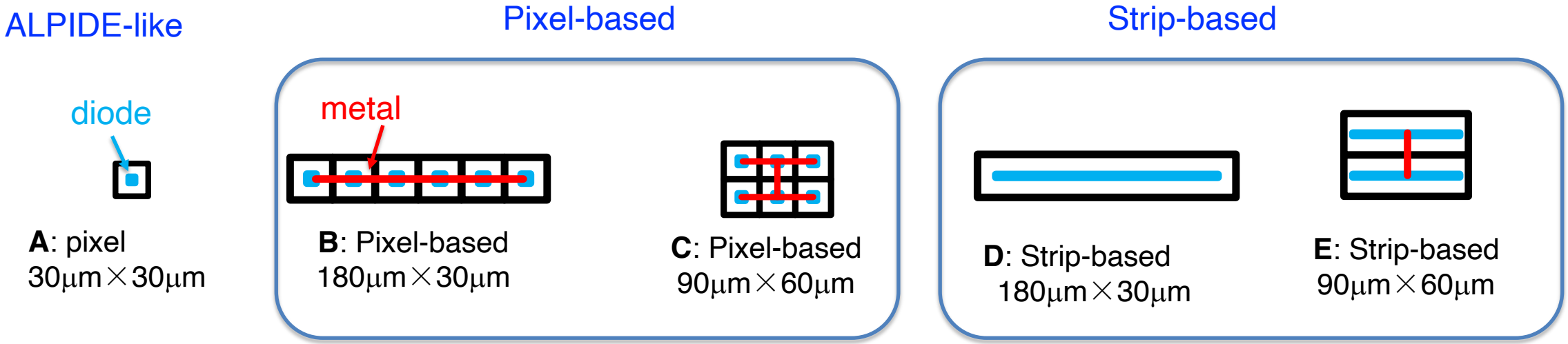
- Requirements on the STCF MAPS
  - Power consumption: $\leq 100 mW/cm^2$
  - Material budget per layer: $\leq 0.35\%\ X_0$
  - Spatial resolution: $\leq 30 \mu m$
  - Time resolution: $\leq 50 \mathrm{ns}$ (to deal with the pileup issue at high luminosity)
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding

Probability of pileup(with an event rate of 400 kHz @ J/ψ, bunch crossing of 4ns):
- 4% within 100ns
- 8% within 200ns



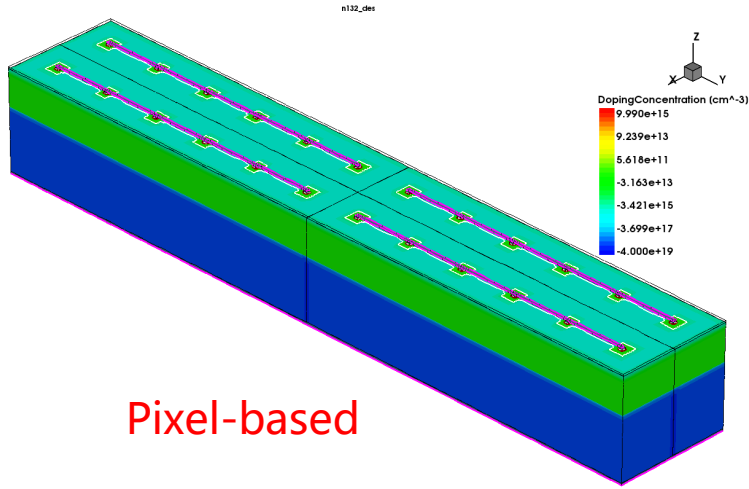
Sensor design

- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - Three different designs
    - Pixel-based: analog connected small pixels ($1\times6 \rightarrow 1, 2\times3 \rightarrow 1$) using metal lines
    - Strip-based: extended diode size in one direction
    - Superpixel based: digital connected small pixels

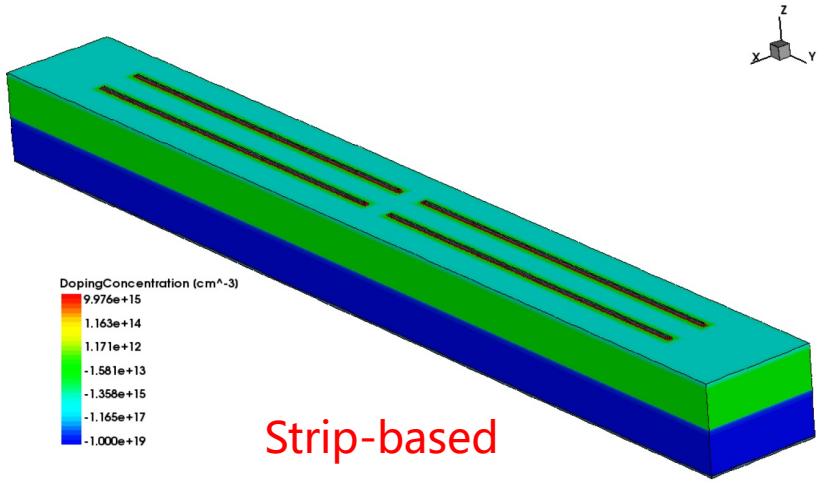


TCAD simulation

- Strip Sensor
  - Rectangular: 30μm×180μm
  - Diode : 2μm×150μm
- Sensor capacitance
  - Single pixel: 2 fF
  - Pixel-based pixel: 12 fF
    - Also need to consider the capacitance of metal lines
  - Strip-based pixel: 30 fF
    - Much larger than 2 fF ×6

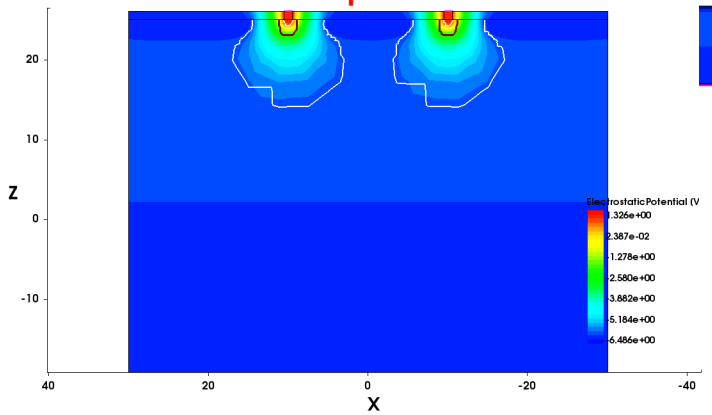


Pixel-based



Strip-based

XZ plane

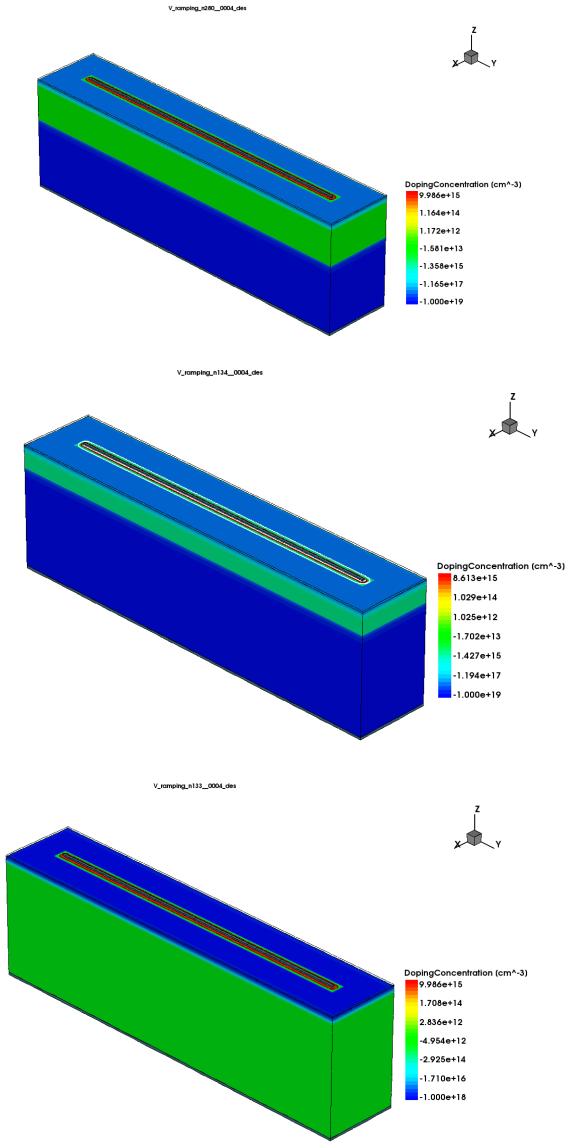


YZ plane

Uniformer depletion zone along the strip → beneficial for charge collection and timing

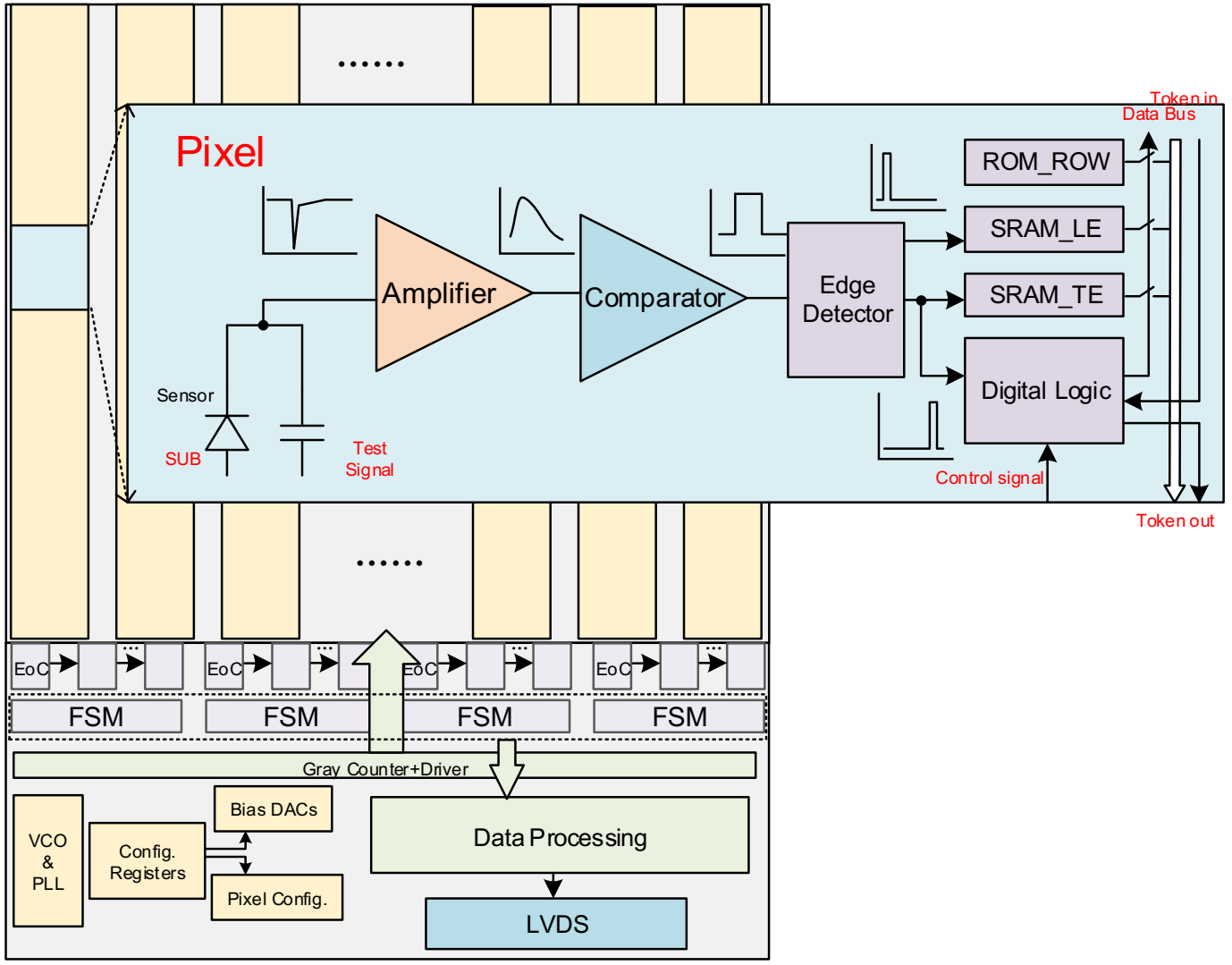
Design technologies

- Three different CIS technologies are being explored
  - Default: 180nm CIS with high-resistivity epitaxial wafers
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$; epi thickness: ~20 μm
    - Eg: Tower 180nm(ALPIDE)
  - 90nm CIS with low-resistivity epi wafers:
    - Resistivity: $\gtrsim 10\Omega \cdot cm$; epi thickness: 10~20 μm
  - 130nm CIS with high resistivity substrates:
    - Resistivity: $\gtrsim 1\mathrm{k}\Omega \cdot cm$, no epi layers



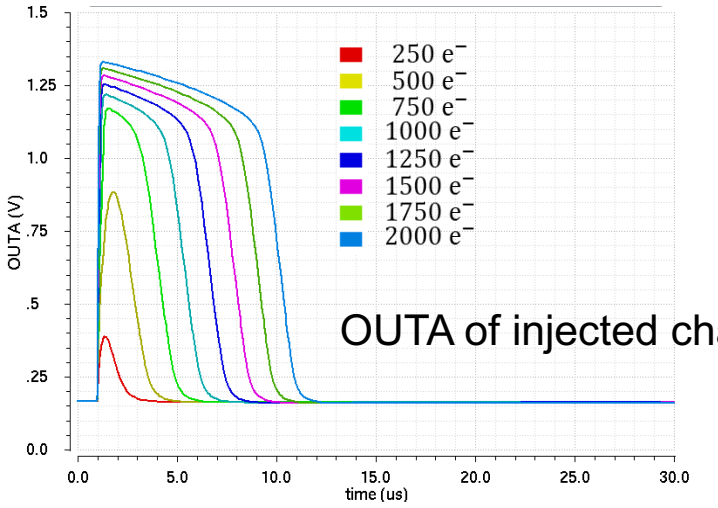
Readout architecture

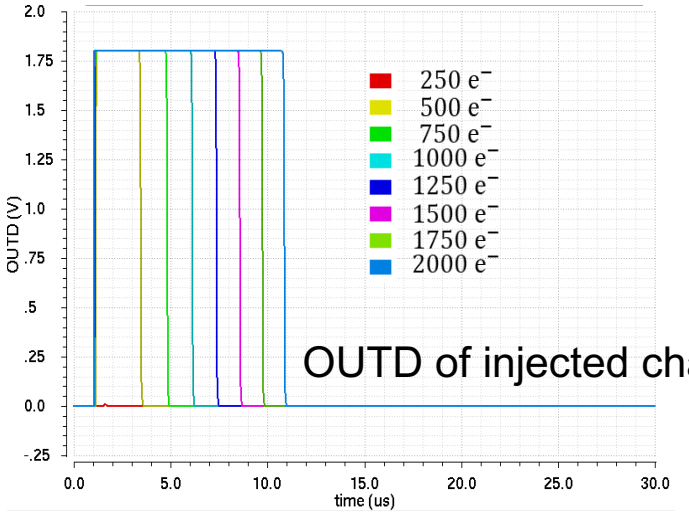
- In-pixel circuits
  - Analog amplifier, comparator
  - Priority readout
  - SRAM, ROM
  - Charge injection
- Digital readout
  - End-of-column driver
  - Column level priority logic
  - Data processing module
  - Serializer
  - PLL, LVDS
- Analog configuration
  - VDAC×2, IDAC
  - Bandgap, EoC current mirror
  - I^2C
- Test points

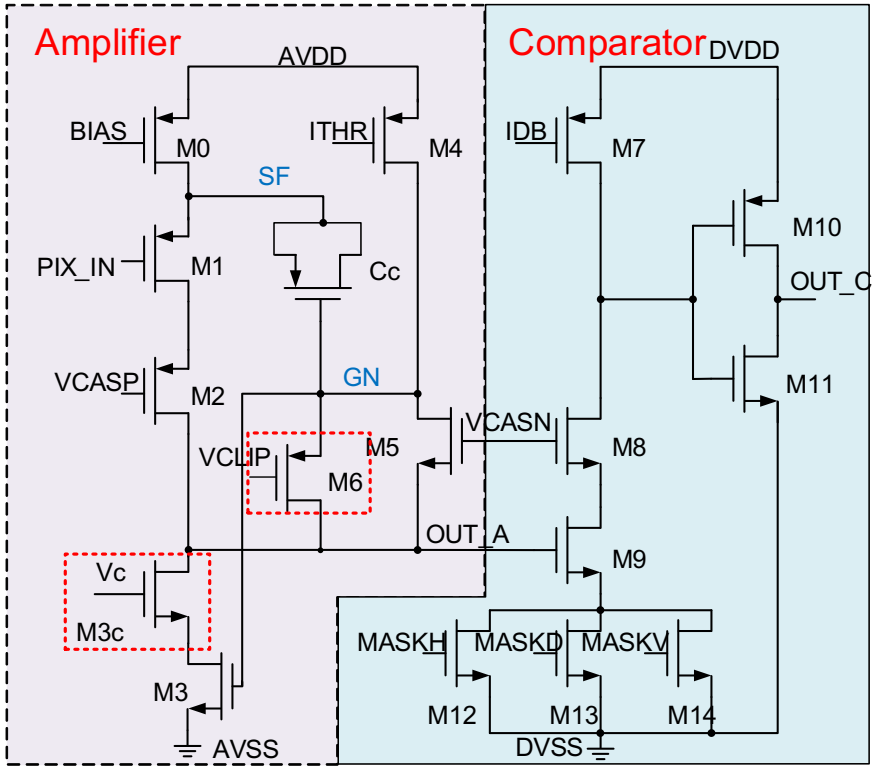


In-pixel front-end: analog

- Analog amplifier & current comparator(similar to the TJ-Monopix2 frontend)
- Simulated performance (30μm×180μm, strip-based sensor)
  - In the timing measurement mode: Threshold=309.0 e$^-$, ENC=11.4 e-, Mismatch=5.7 e$^-$
  - Power consumption: ~800 nA/pix, ~26 mW/cm^2
  - ΔToT/ ΔQ_{inj}=4.8 μs/ke$^-$

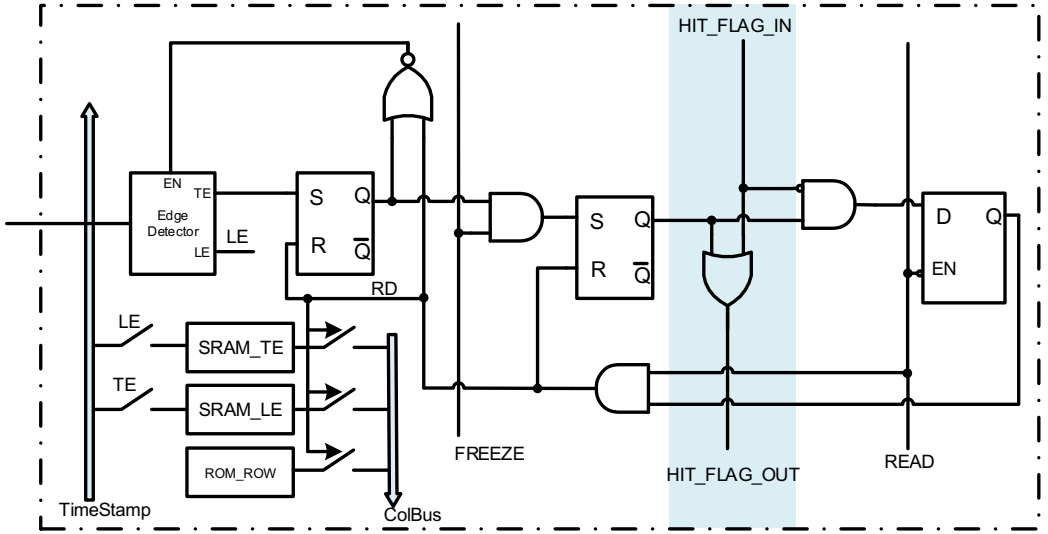


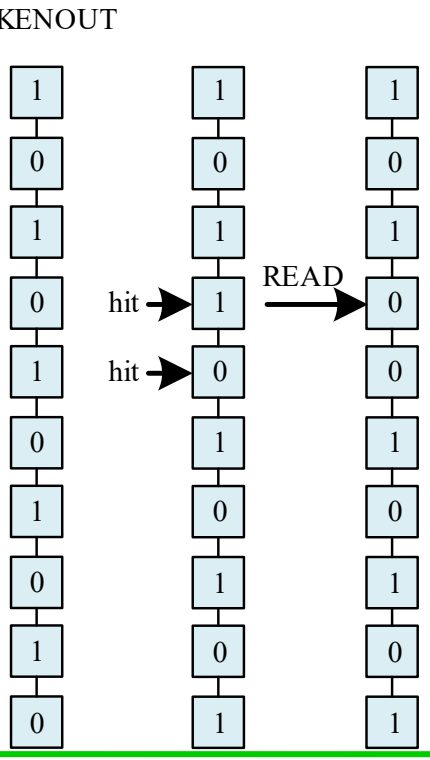


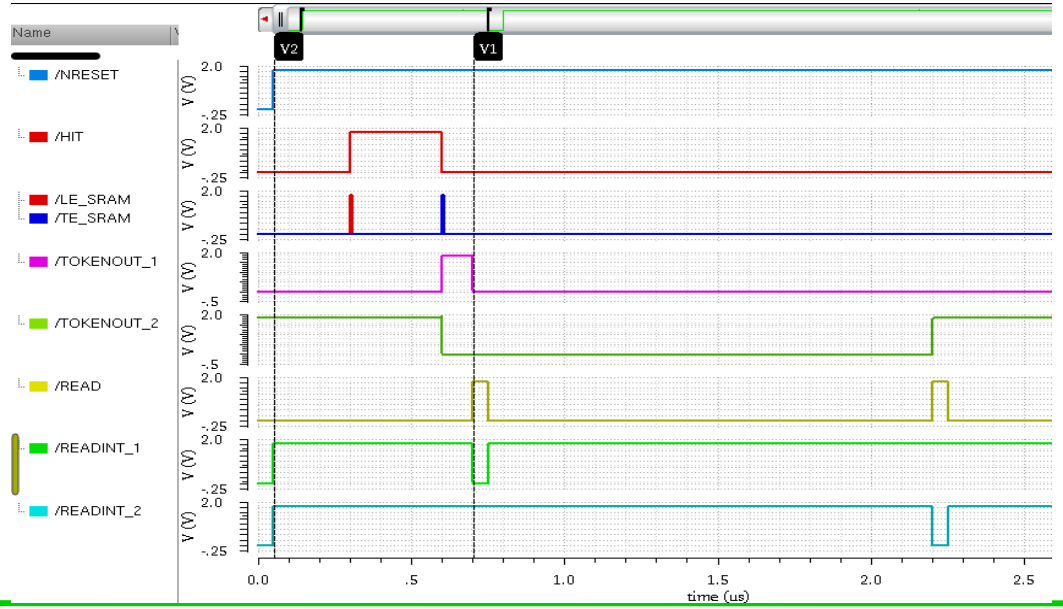


In-pixel front-end: digital

- In-pixel digital circuits
  - Priority readout based on TOKEN
  - Readout scheme similar to ATLAS FE-I3
  - Timestamp clock: 20MHz
  - 8-bit leading-/falling-edge
    - Can be optionally turned off
  - Readout clock: 10MHz

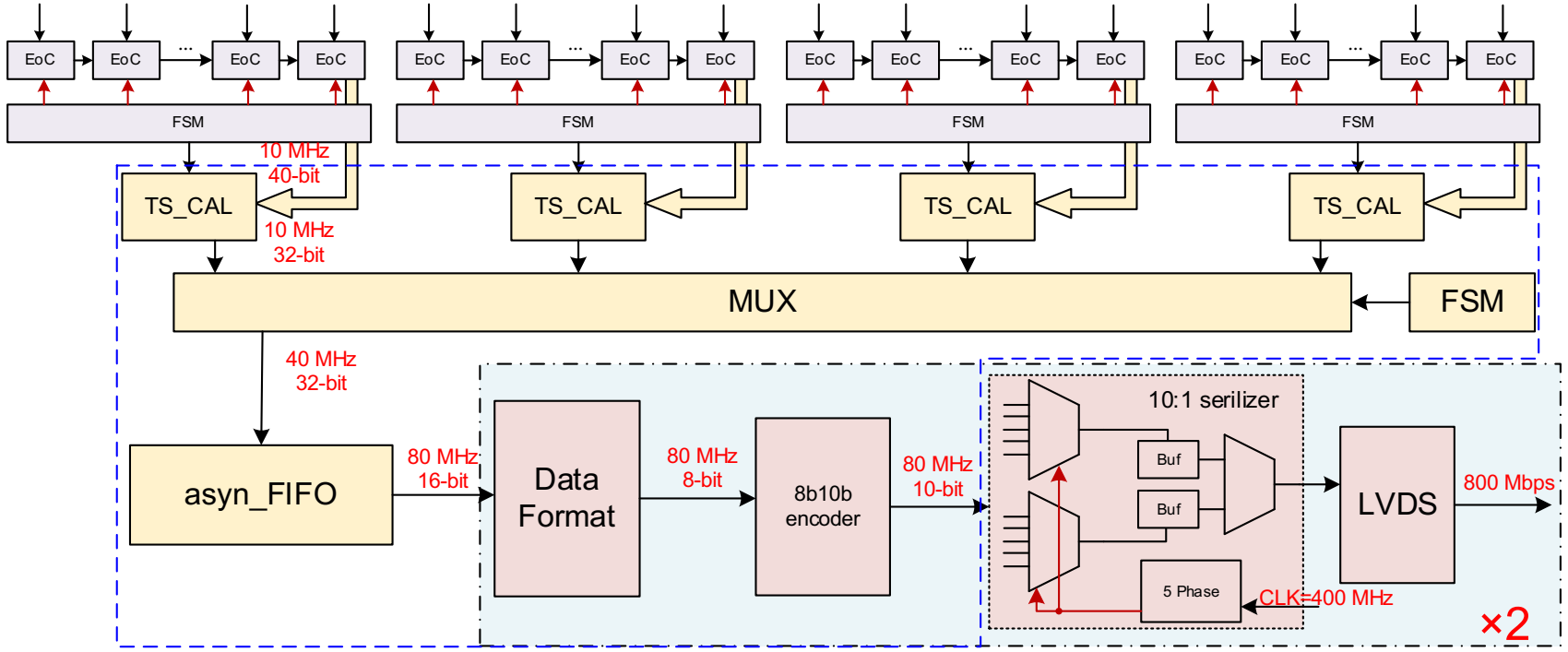






Peripheral readout

- EoC data readout circuit
  - Grouped columns with each group readout in parallel to reduce waiting time
  - Readout rate >29.6 MHz/Chip，40-bit/Hit(55-bit/Hit after frame encoding)
  - Bandwidth: 800Mbps×2

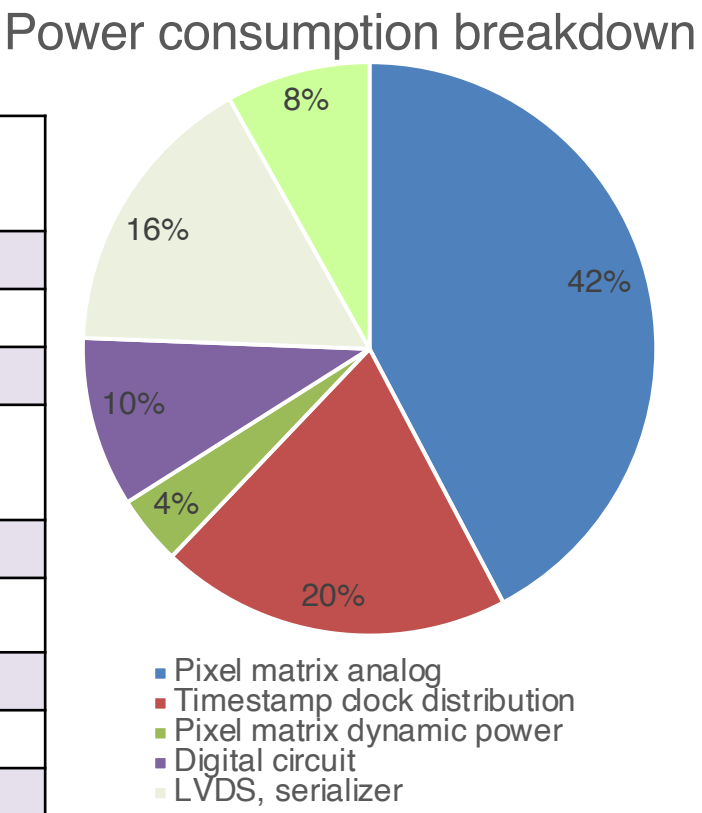


- Data processing unit
  - Timestamp calibration
  - Column group MUX
  - Async FIFO
  - Frame builder
  - 8b10b encoder
  - Serializer

Power density estimation

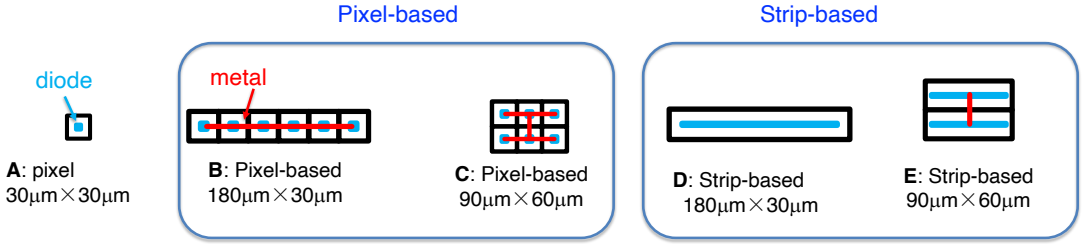
- Estimated power consumption extended to the full scale chip (~2 cm×2 cm)
  - Strip-based: 55.7 mW/cm^2
  - Pixel-based: 46.2 mW/cm^2
- Expected to reach the target of ~50 mW/cm^2
  - With the potential to use air cooling

Items	Power consumption	Notes
Analog in pixel matrix	~26 mW/cm^2	Strip-based
	~15 mW/cm^2	Pixel-based
Timestamp clock distribution	12.2 mW/cm^2	
Dynamic power consumption of the pixel matrix	2.4 mW/cm^2	with a data rate of 8.7 MHz/cm^2
Periphery	23.5 mW	32MHz event rate
PLL, serializer, LVDS	39 mW	x 2 data/clock output
Analog configuration	20 mW	
Total	222.6 mW	Strip-based
	184.6 mW	Pixel-based

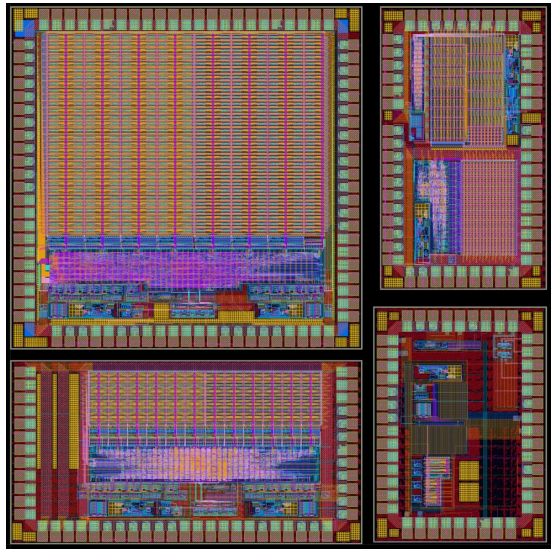


Prototype chips

- Designed 4 prototype chips based on the TJ 180nm technology
  - Chip 1: ALPIDE-like small pixels，0/1 digital readout
  - Chip 2: large pixels ($96\mu m \times 60\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 3: large pixels ($170\mu m \times 31\mu m$, Strip-based + Pixel-based) with TOA+TOT readout
  - Chip 4: 3T analog readout (5 types of sensors)



	Chip1	Chip2		Chip3		Chip4
Pixel size（μm×μm）	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	ALPIDE-like	Strip-based	Pixel-based	Strip-based	Pixel-based	Mixed
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Token	Token		Token		Analog readout
ToA & ToT	X	√		√		X



Total area: 5 mm×5 mm
Submitted in 2024 Q1

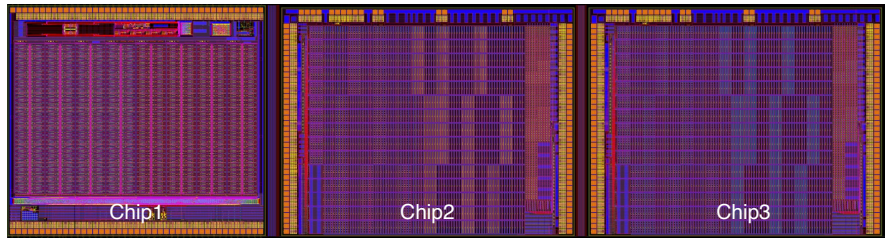
Alternative designs: 90nm CIS

- Front-side illuminated (FSI) COMS process(FCIS90)
  - Low resistivity epitaxial wafer
  - 4-metal layers
- Back-side illuminated (BSI) COMS process(BCIS90)
  - Low resistivity epitaxial wafer
  - 6-metal layers

Submitted in 2024.5

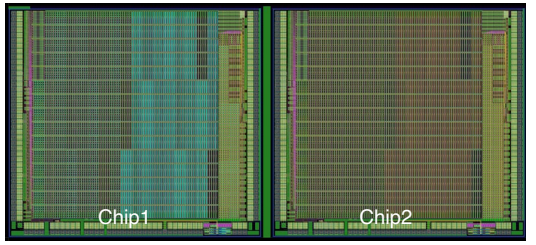
FCIS protype chips: 10.4 mm×3.0 mm

- Chip1: MAPS
- Chip2&3: 3T sensors



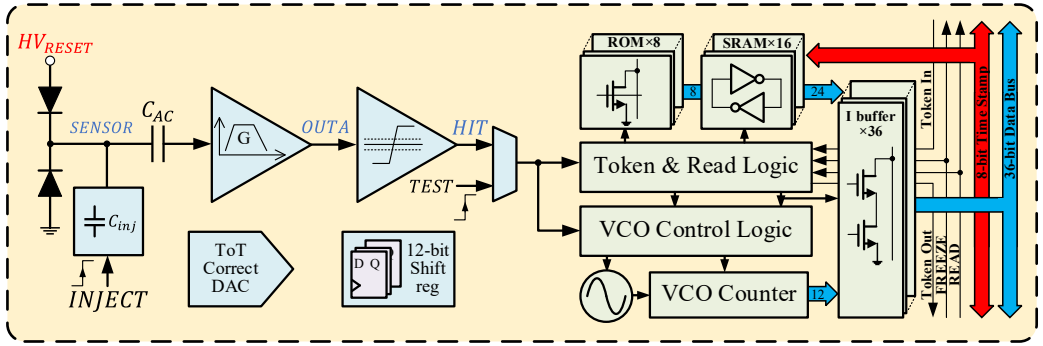
BCIS chips: 7.0 mm×3.0 mm

- Chip1&2: 3T sensors
- 6 test pixel for analog amplifier verification

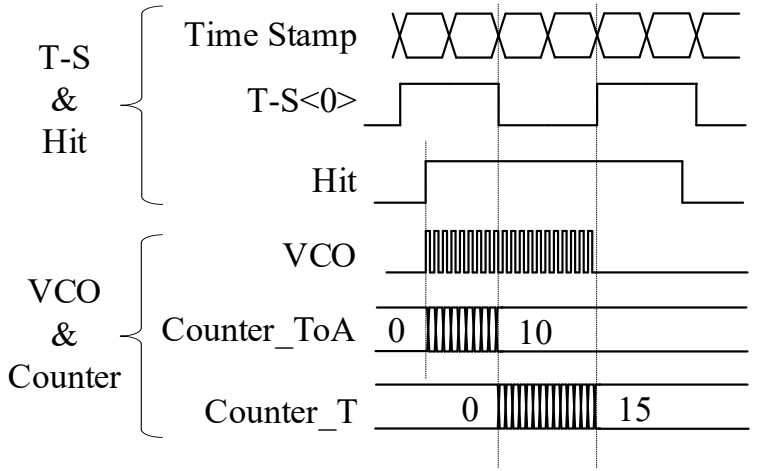


90nm design: in-pixel circuit

- In-pixel VCO
  - Benefit from the smaller process node(180nm →90nm)
  - High timing resolution with a low power consumption

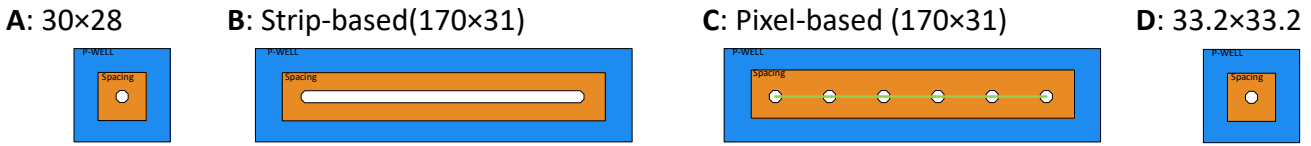


  - VCO (500MHz) starts once the leading edge of the hit signal arrives
    - TOA counting and no calibration needed
  - Timing
    - 8-bit Gray code for the leading edge
    - 8-bit Gray code for the falling edge
    - 6-bit for the leading edge VCO
    - 6-bit for the timestamp LSB interval
  - Simulation shows an expected timing resolution of about 6ns



Alternative designs: 130nm CIS

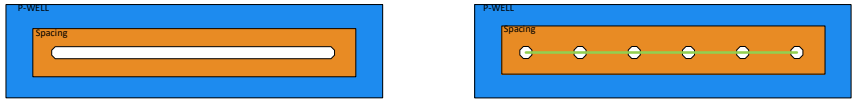
- 130nm CIS
  - Only support high resistivity substrate(no epitaxial layers)
  - 6 metal layers and support deep p-well
- Four prototype chips in total, to be submitted in 2024.7
  - Chip1: Large sensor, ToA/ToT readout
  - Chip2: Small sensor, ALPIDE-like
  - Chip3: 3T sensors with analog readout
  - Chip4: Small sensor, readout based on superpixels



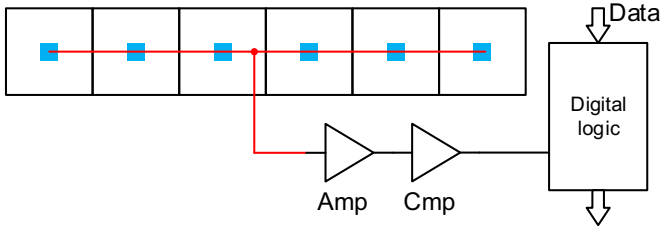
	Chip1		Chip2	Chip3	Chip4
Pixel size (μm×μm)	170 × 31		30 × 28	Mixed	33.2×33.2
Sensor	B	C	A	A+B+C (Metal、Active、Diode)	D
Pixel array	60x8	60x8	60x48	Mixed	576×144
Readout	Column-drain		Column-drain	Analog readout	Column-drain （super pixel based）
ToA & ToT	√		×	×	√

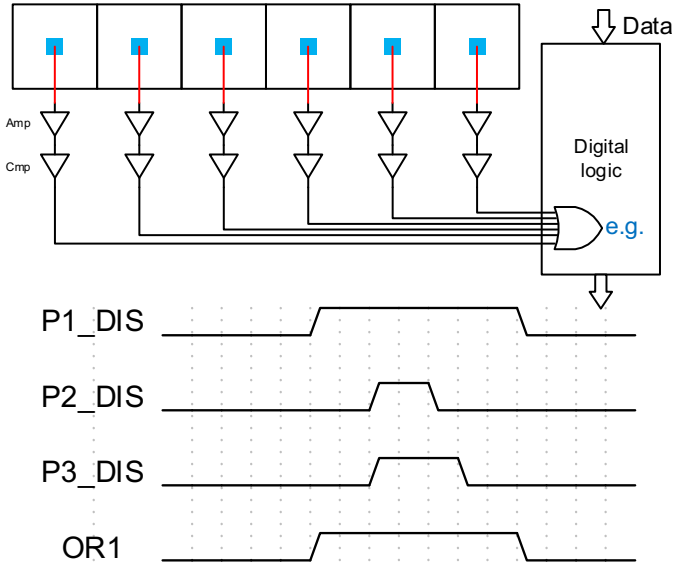
130nm MAPS design with superpixels

- Small pixels:
  - Advantages: low capacitance, good S/N, charge collection and timing
  - Disadvantages: too many readout channels, high power consumption
- Strip-based pixels or analog connected small pixels can reduce the number of readout channels, but still have larger capacitance



- How to make use of the advantages of small pixels but to keep the power consumption low? Superpixels!

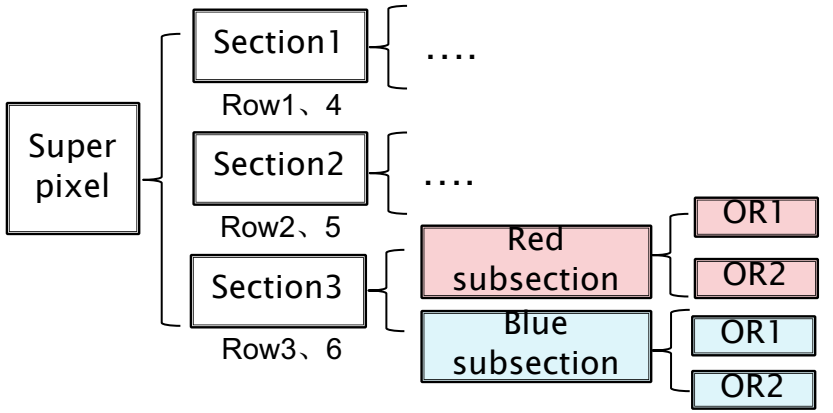


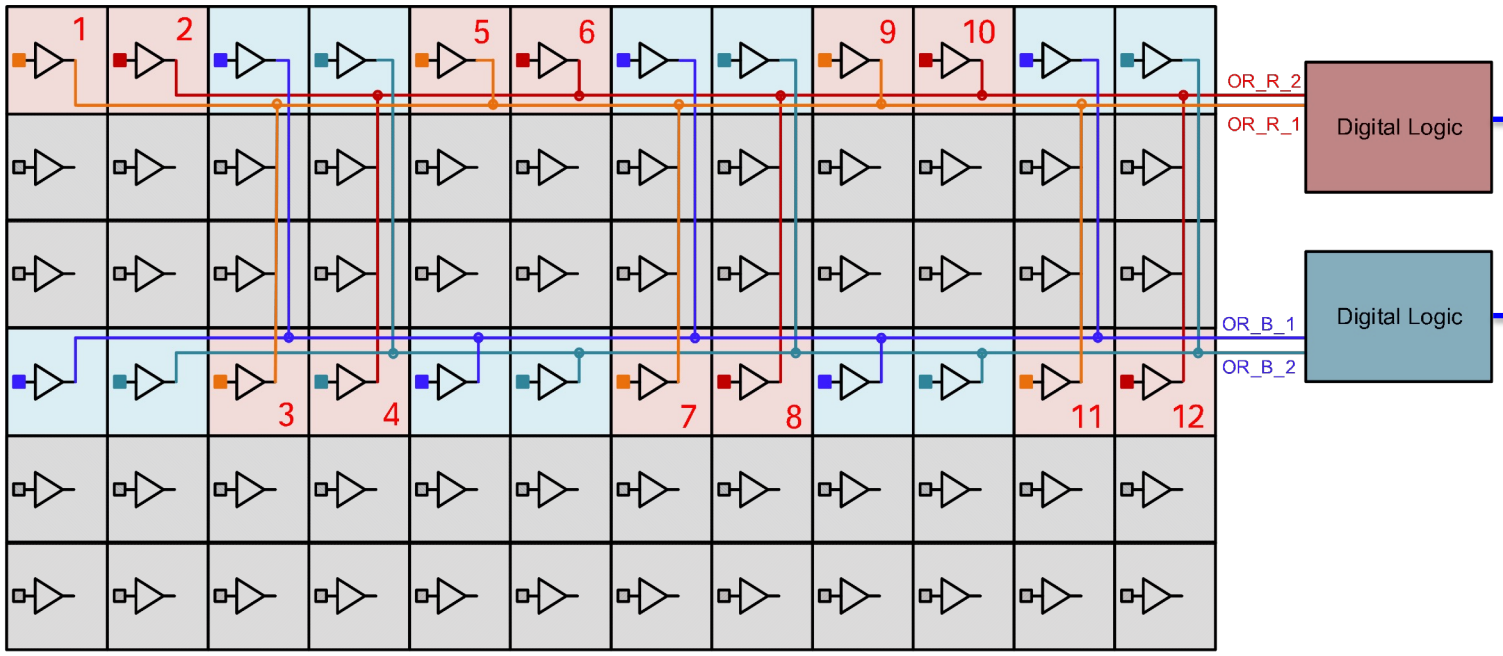


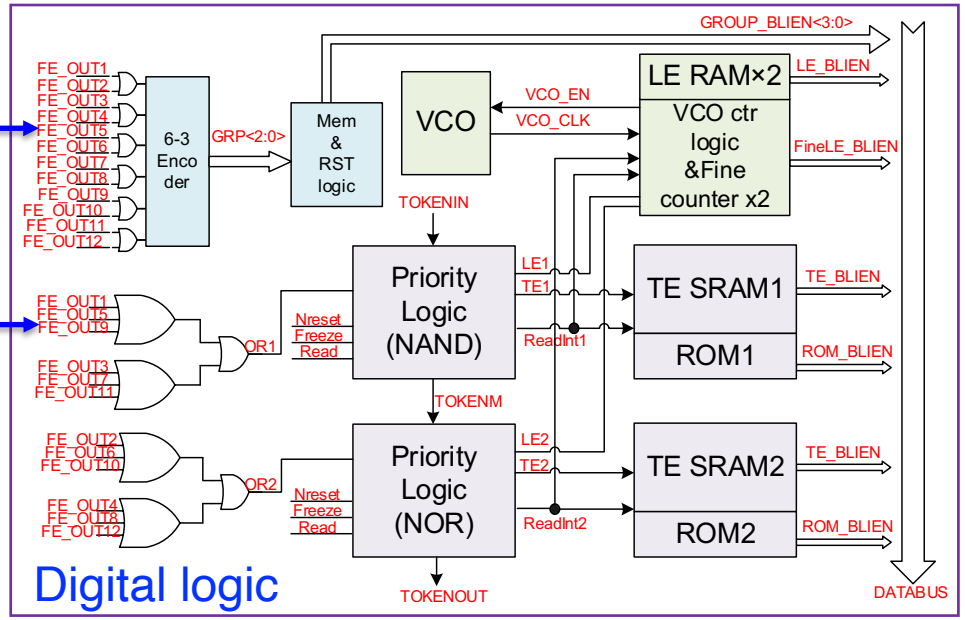
- Each pixel has its own front-end analog
- Simply combining adjacent pixels with FastOR would lead to TOT loss
- Solution: Combining non-adjacent pixels

130nm MAPS design with superpixels

- Combining non-adjacent pixels to prevent ToT loss
- Superpixels with a 6×12 pixel array
  - 6 sets of identical digital readout logic(6 superpixels)
    - OR of pixels with odd and even indices separately
  - When cluster size < 3×4, no ToT loss occurs
    - with an equivalent spatial resolution of 1×1







Summary

- MAPS-based inner tracker is a promising option for the STCF
  - Power consumption: $\leq 100 mW/cm^2$
  - Low material budget per layer: $\leq 0.35\%\ X_0$
  - Spatial resolution: $\leq 30 \mu m$
  - Time resolution: $\leq 50 \mathrm{ns}$

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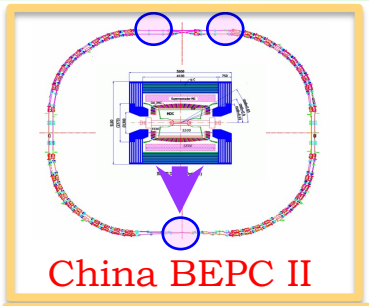
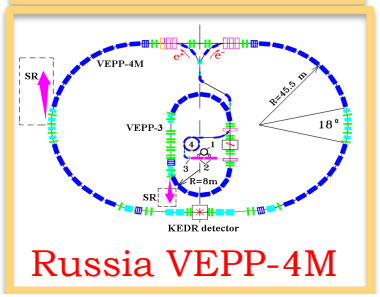
- Prototype chips design finished and submitted to the foundry in 2024.3
  - Based on the 180nm HR epi technology
- Also exploring alternative CIS technologies
  - 90nm CIS with LR epi
  - 130nm CIS with HR substrate

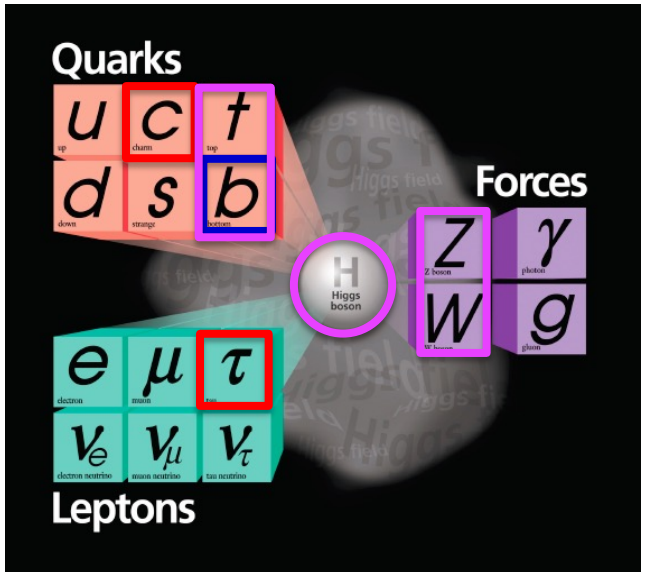
Backup

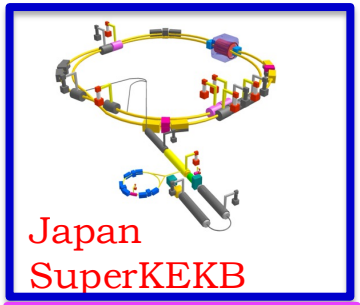
Collider experiments


China BEPC II



Russia VEPP-4M




Japan SuperKEKB


Europe LHC

Increase luminosity ~50-100

China BEPCII Japan KEKB, US PEPII

China STCF Japan SKEKB，

CERN LEP → LHC US Tevatron

CERN FCC, China CEPC

Increase energy ~10

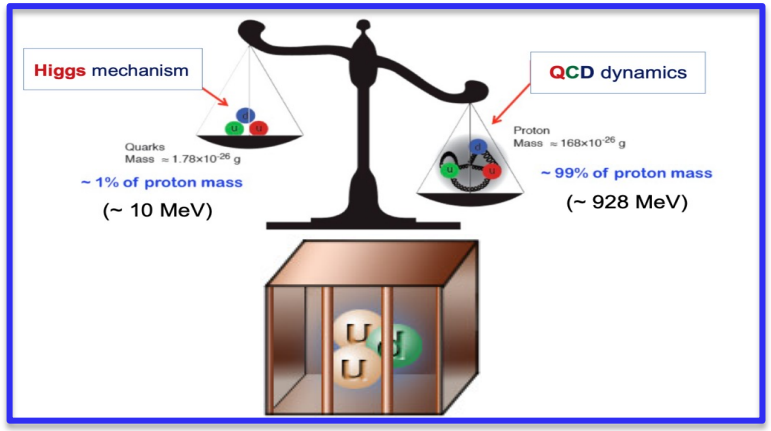
High luminosity/precision frontier:
- Hadron structure
- Exotic matter
- Nature of strong interaction
- Search for new physics

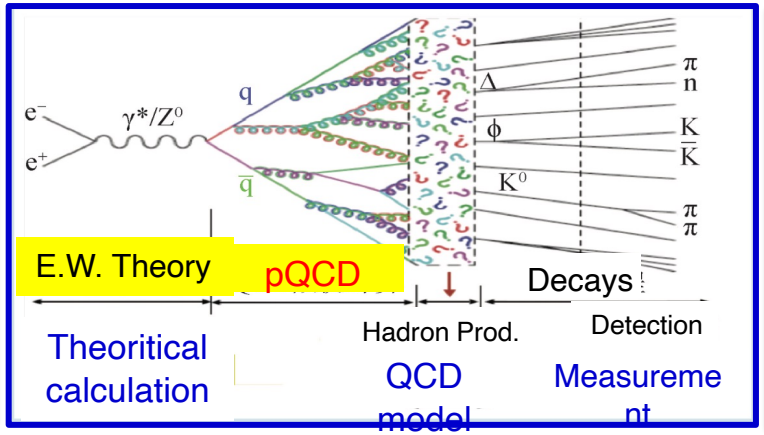
High energy frontier:
- Origin of mass
- Nature of electroweak interaction
- Search for new physics
- Precise study of third generation quarks.

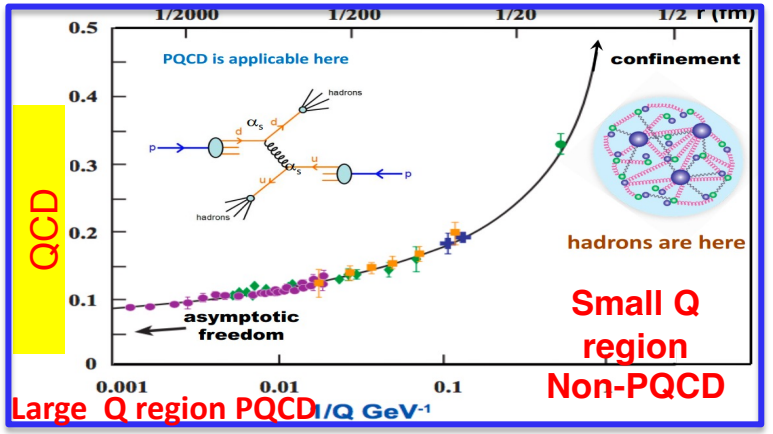
Key Questions To The Strong Interaction

The key questions to the strong interaction

- What is the origin of observable mass (mass of hadrons)?
- How are hadrons formed, and what is the hadron structure?
- What is the essence of asymptotic freedom and color confinement?







The primary task of particle physics:develop understanding of the laws of nature at a more fundamental level.

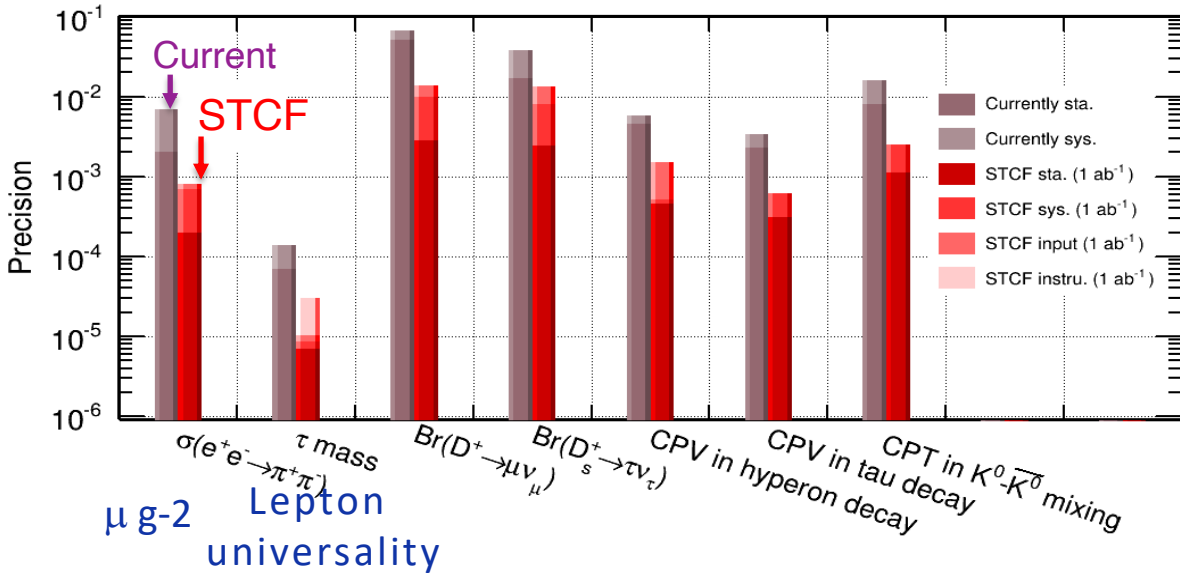
→ Requires a coordinated multi-dimensional program: precise theoretical predictions for observation, experimental measurements with state-of-the-art sensitivities and well-controlled systematic errors.

→ STCF can play unique role to this primary task!

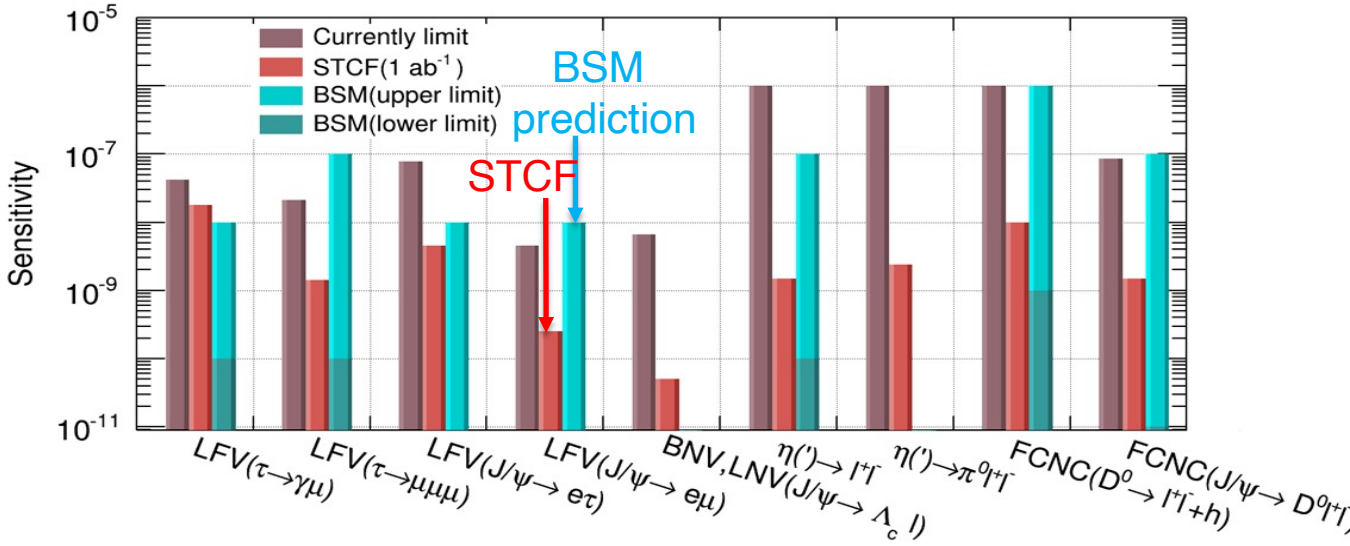
Physics opportunities with STCF

STCF can improve the current precisions of many important measurements, and sensitivities of many new physics searches by 1-2 orders of magnitude.

Some have exceeded theoretical expectations→ Great potential to discover new physics!



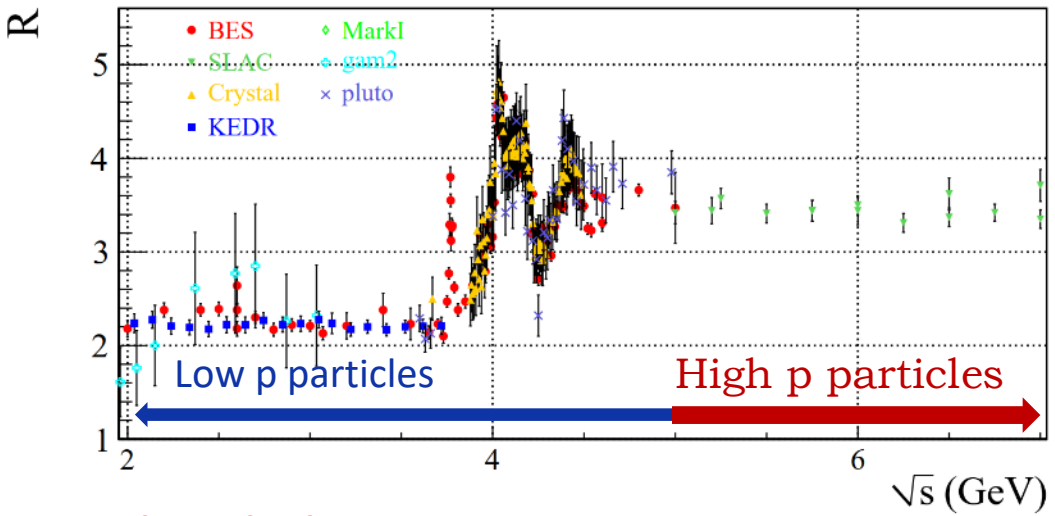
Violation of symmetries(CP, CPT)



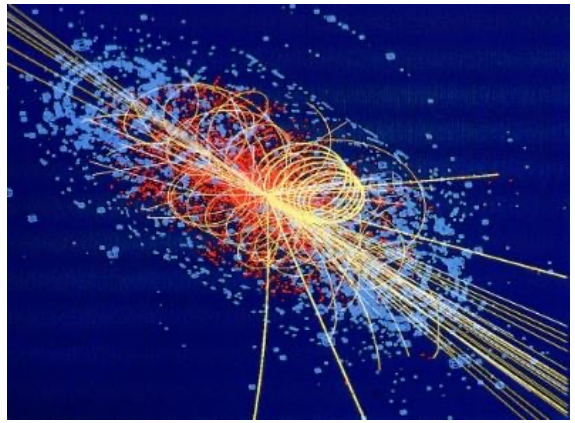
Violation of lepton flavor, baryon number, flavor-changing neutral current processes (LFV, BNV, FCNC)

Spectrometer Design Requirements and Challenges

Wide energy region E_{cm} : 2-7 GeV



Super high luminosity 5 × 10^{34} $cm^{-2}s^{-1}$



- High events ~400 kHz
- High counting rate ~1 MHz/cm^2
- High data flow ~300 GB/s
- High radiation and bkg
  ~4 kGy/y,~2 × 10^{11} $n_{eq}/cm^2/y$

Benchmark physics requirements

Process	Physics interest	Optimized subdetector	Requirements
$\tau \to K_s\pi\nu_\tau$, $J/\psi \to \Lambda\bar{\Lambda}$, $D_{(s)}$ tag	*CPV* in the τ sector, *CPV* in the hyperon sector, Charm physics	ITK+MDC	Acceptance: 93% of 4π; Trk. Effi.: $> 99\%$ at $p_T > 0.3$ GeV/c; $> 90\%$ at $p_T = 0.1$ GeV/c, $\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130$ μm at 1 GeV/c
$e^+e^- \to KK + X$, $D_{(s)}$ decays	Fragmentation function, CKM matrix, LQCD, etc.	PID	π/K and K/π misidentification rate $< 2\%$, PID efficiency of hadrons $> 97\%$ at $p < 2$ GeV/c
$\tau \to \mu\mu\mu$, $\tau \to \gamma\mu$, $D_s \to \mu\nu$	cLFV decay of τ, CKM matrix, LQCD, etc.	PID+MUD	μ/π suppression power over 30 at $p < 2$ GeV/c, μ efficiency over 95% at $p = 1$ GeV/c
$\tau \to \gamma\mu$, $\psi(3686) \to \gamma\eta(2S)$	cLFV decay of τ, Charmonium transition	EMC	$\sigma_E/E \approx 2.5\%$ at $E = 1$ GeV, $\sigma_{\rm pos} \approx 5$ mm at $E = 1$ GeV
$e^+e^- \to n\bar{n}$, $D_0 \to K_L\pi^+\pi^-$	Nucleon structure Unity of CKM triangle	EMC+MUD	$\sigma_T = \frac{300}{\sqrt{p^3\,(\mathrm{GeV}^3)}}$ ps

FRONTIERS OF PHYSICS

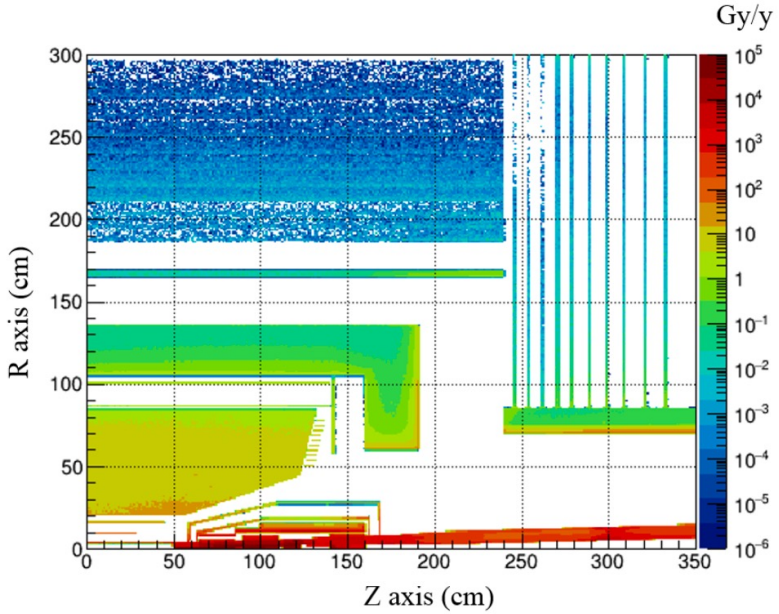
REPORT
Volume 19 / Issue 1 / 14701 / 2024

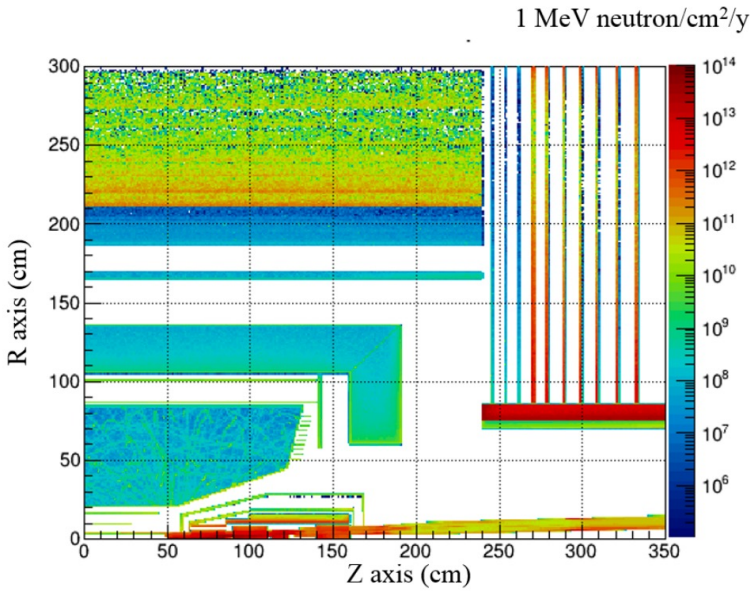
STCF conceptual design report (Volume 1): Physics & detector

Front. Phys. 19, 14701 (2024)

Radiation level

- Simulated radiation level



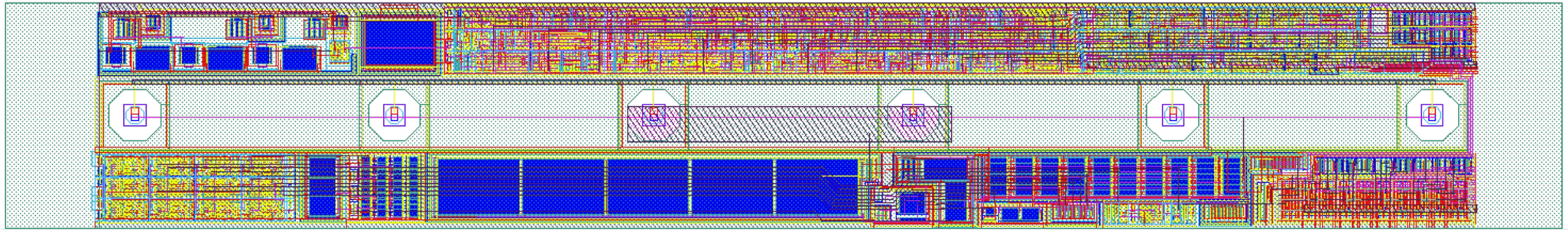


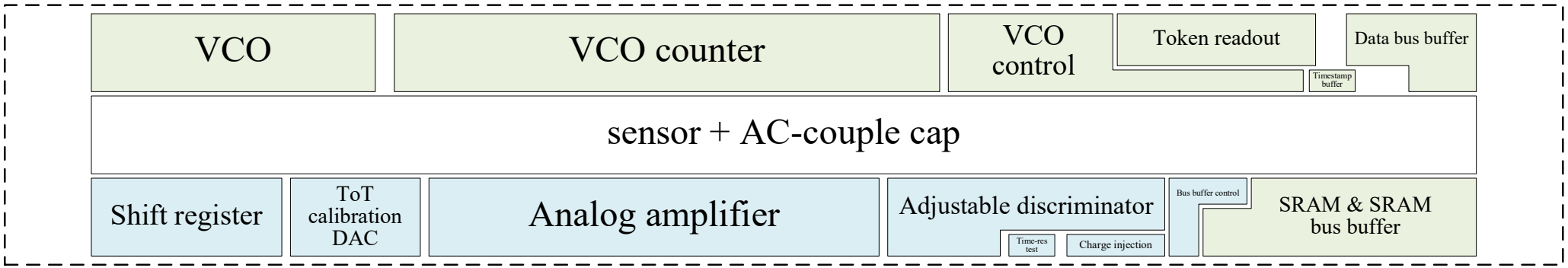
Detector	Highest TID value per pixel (Gy/y)	Highest NIEL damage per pixel (1 MeV neutron/cm^2/y)	Highest count rate per channel (Hz/channel)
Silicon-inner-1	3490	1.75×10^{11}	2.61×10^{2}
Silicon-inner-2	320	3.72×10^{10}	2.74×10^{1}
Silicon-inner-3	150	2.68×10^{10}	8.51×10^{0}

NIEL: ~ 10^{11} n_{eq}/cm^2/y
TID: ~0.35MRad/year

FCIS90: In-pixel circuit

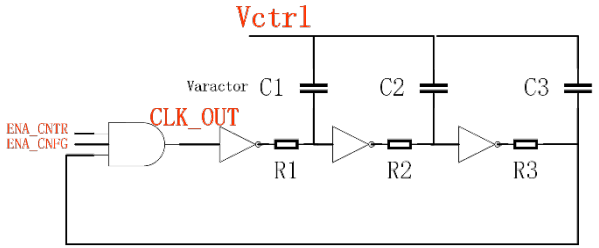
- Layout of one pixel
  - 180 μm × 30 μm
  - Analog and digital part separately placed on two sides of the sensor

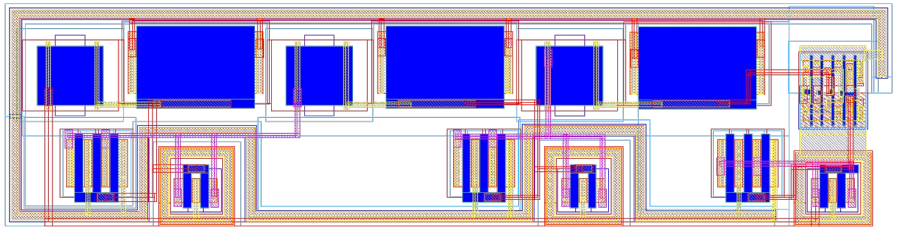




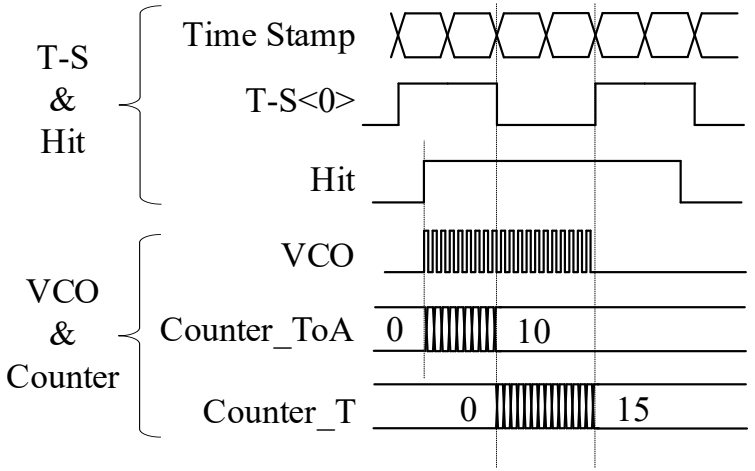
FCIS90: In-pixel circuit

- In-pixel VCO
  - High timing resolution with low power consumption





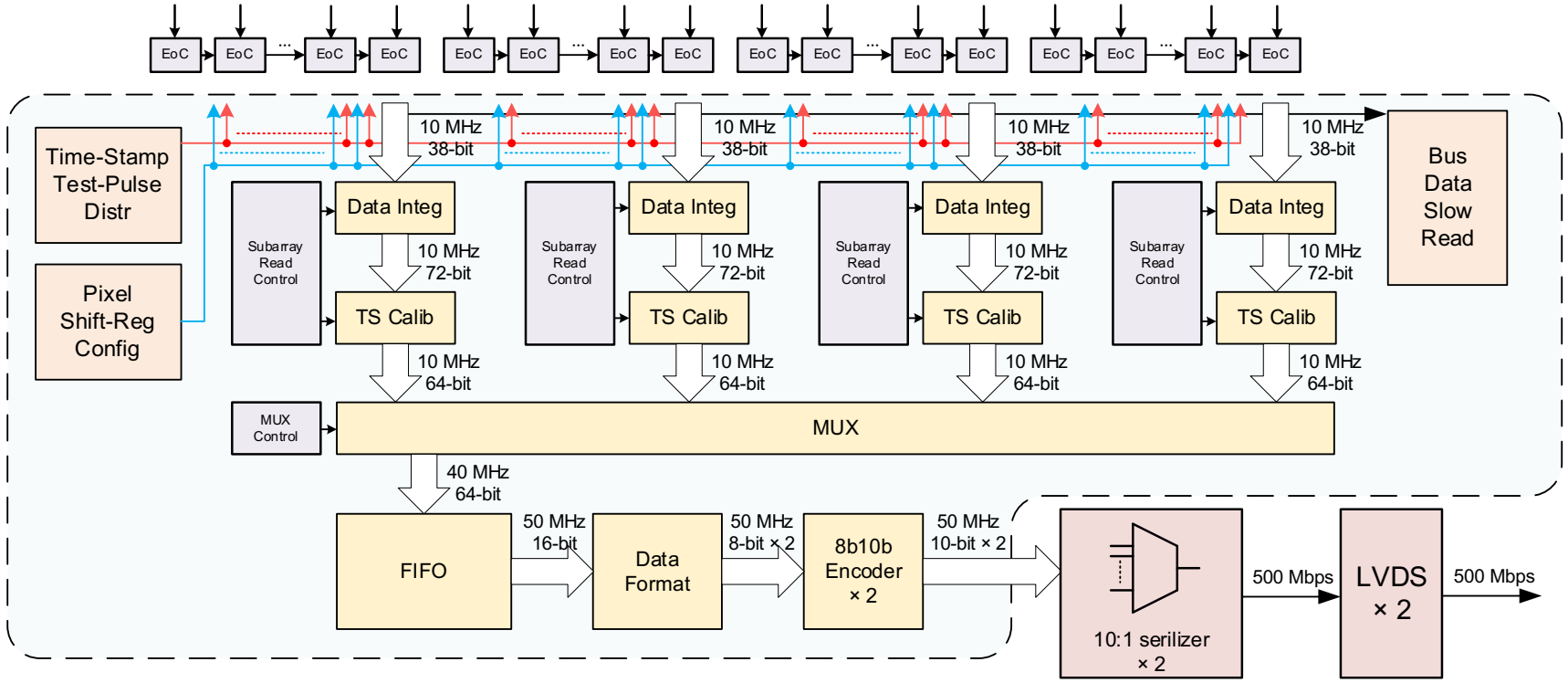
  - VCO starts once the leading edge of the hit signal arrives
    - TOA counting and
    - No calibration needed
  - Timing
    - 8-bit Gray code for the leading edge
    - 8-bit Gray code for the falling edge
    - 6-bit for the leading edge VCO
    - 6-bit for the timestamp LSB interval



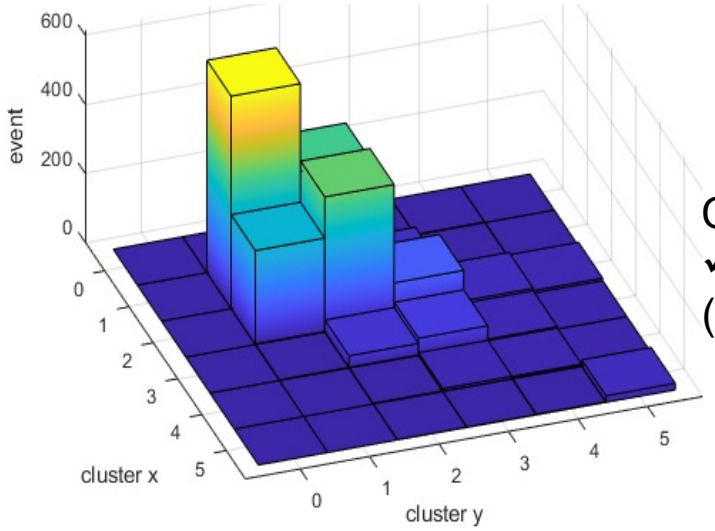
  - Simulation shows an expected timing resolution of about 6ns

FCIS90: Periphery

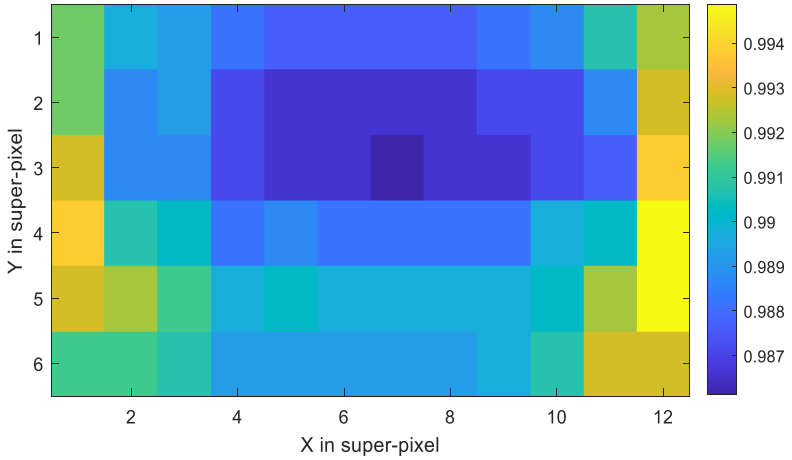
- Provide timestamp and control for the pixel matrix
- Read out hit position and timing of the pixel matrix
  - 32-bit global timestamp
  - Readout rate: 500 Mbps×2



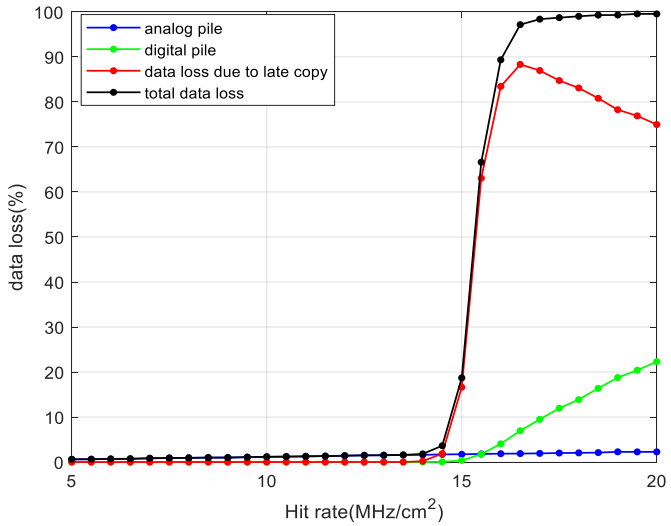
GSMC MAPS design—Chip4



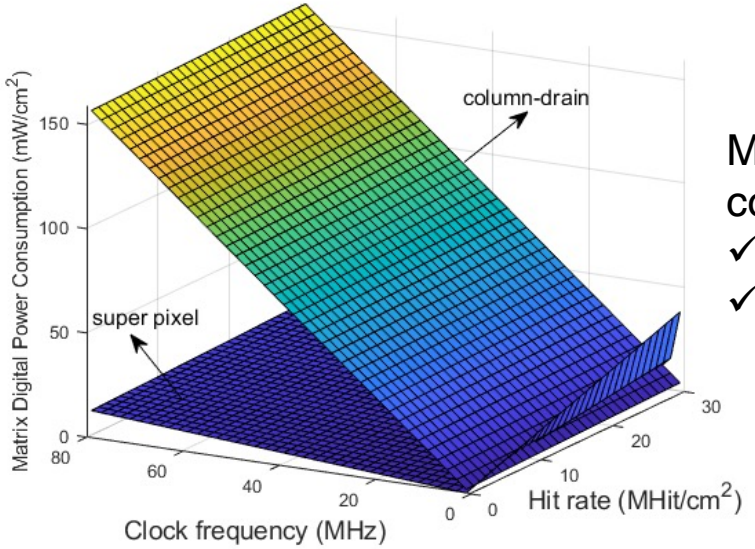
Cluster size distribution:
✓ Mean cluster size=2.3 (Threshold=150 e^-)



The probability of no ToT loss at different positions
✓ No ToT loss >99%



Hit loss simulation
✓ Readout efficiency>99% (hit rate < 8.5 MHz/cm^2)

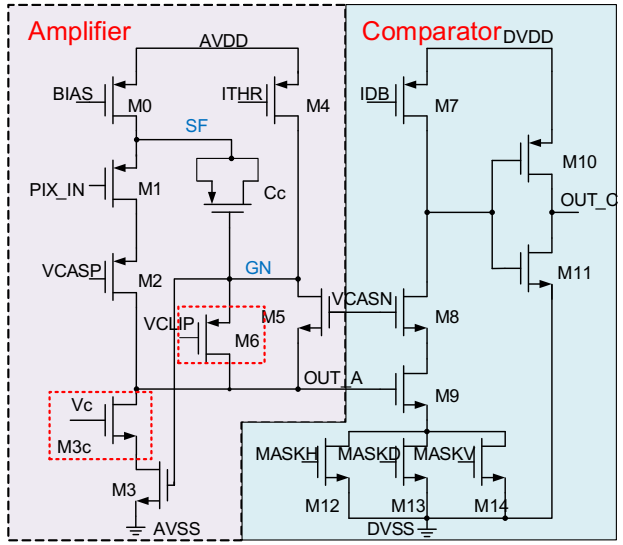


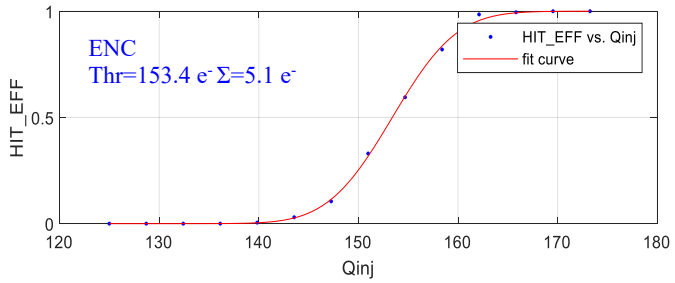
Matrix digital power consumption
✓ Column-drain
✓ Based on super pixel

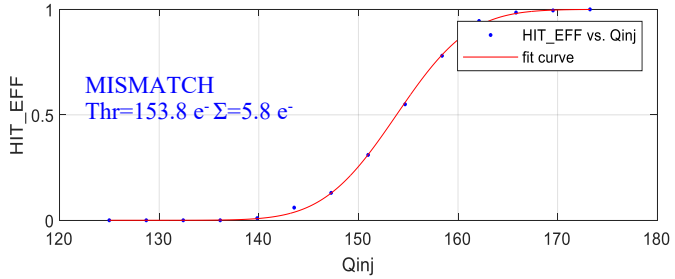
timestamp distribution power ~11.0 mW/cm².

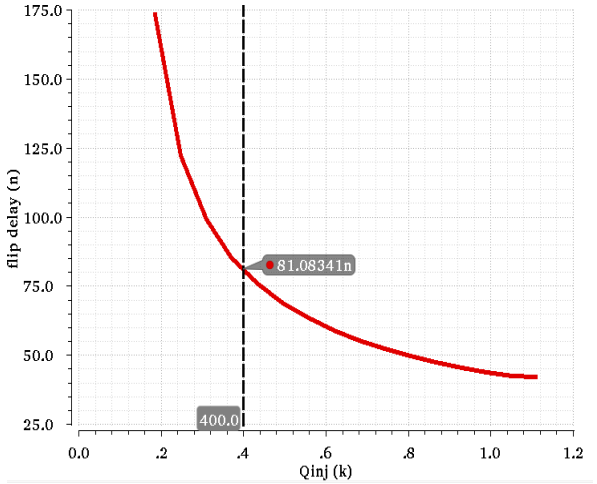
GSMC MAPS design—Chip4 frontend

- Frontend circuit
  - Analog amplifier & current comparator
  - Similar to the Monopix2 frontend
- Simulation results
  - Threshold~153 e^-
  - ENC~5.1 e^-
  - MISMATCH~5.8 e^-
  - Analog power consumption~120 nA/pix
  - Timing response<81 ns(Qinj=400 e^-)
  - ΔToT/ΔQin=189 ns /100 e^-

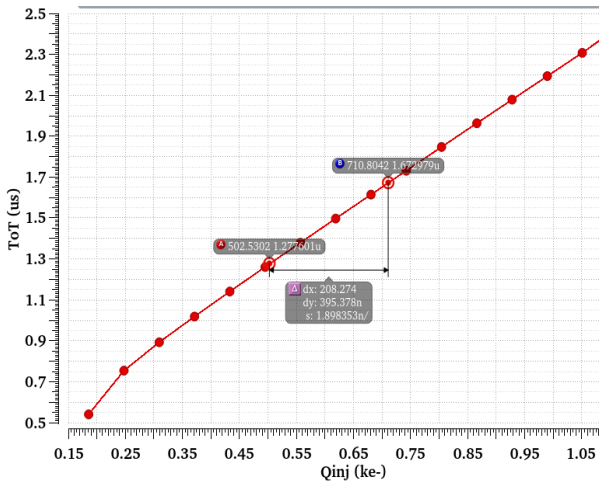








Time walk curve



ToT-Qinj curve

GSMC MAPS design—Chip4 digital readout

- Multiple pixels share readout logic → adequate circuit area
  - Start-stop VCO in super pixels
    - Record fine ToA @500 MHz
    - Almost no static power consumption
    - 5-bit fine ToA, 8-bit coarse ToA, 8-bit ToT