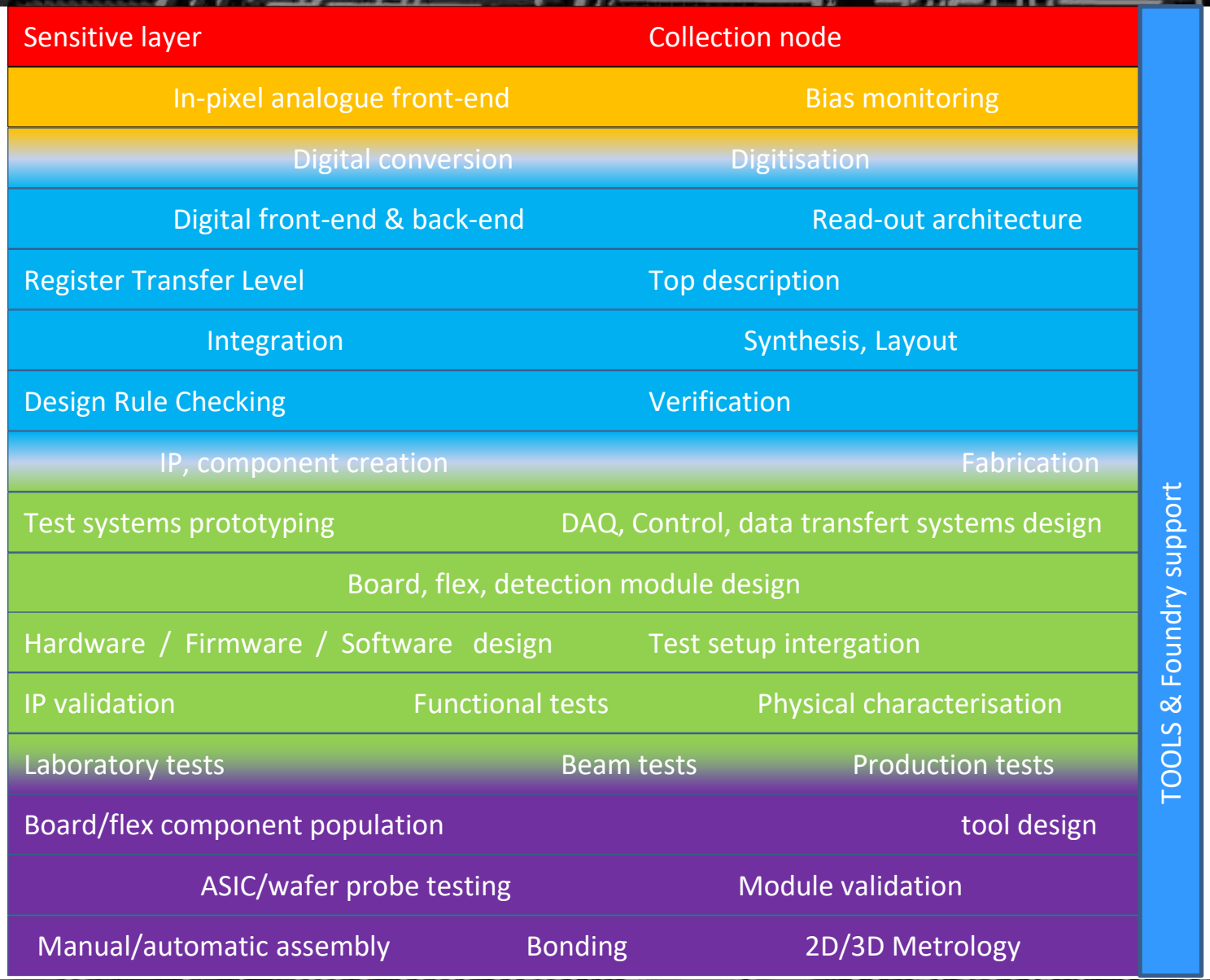
Innovations in CMOS Pixel Sensor Technology at IPHC: Projects and Future Prospects

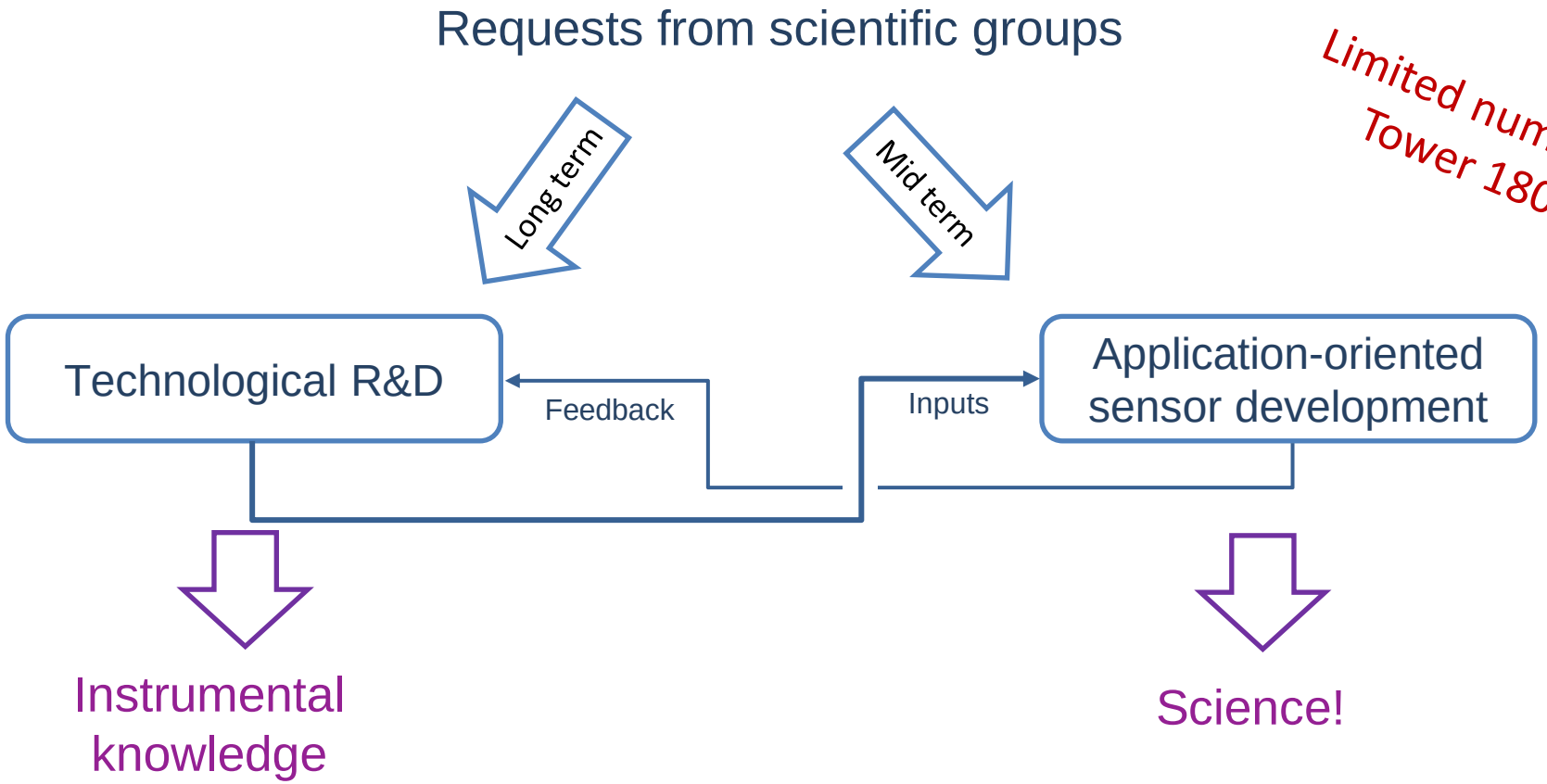
Frédéric Morel on behalf of IPHC teams

IPHC has a full range of MAPS expertise



- Based on the expertise of:
  - C4PI: MAPS facility
  - Physics groups: PICSEL (FCC), ALICE, Belle II
- C4PI a board team of engineers and technicians:
  - 6 in analogue design and process
  - 7 in digital design and verification
  - 6 in test and characterisation
  - 3 in microtechnics and integration
  - 5 to 10 students
    - PhD, internships and apprentices
- Physics groups are essential:
  - Scientific drivers
  - Analysis expertise

C4PI missions



Limited number of technologies
Tower 180 nm and 65 nm

Next generation detectors need new concepts:

- Fast development cycle
- Low risk project

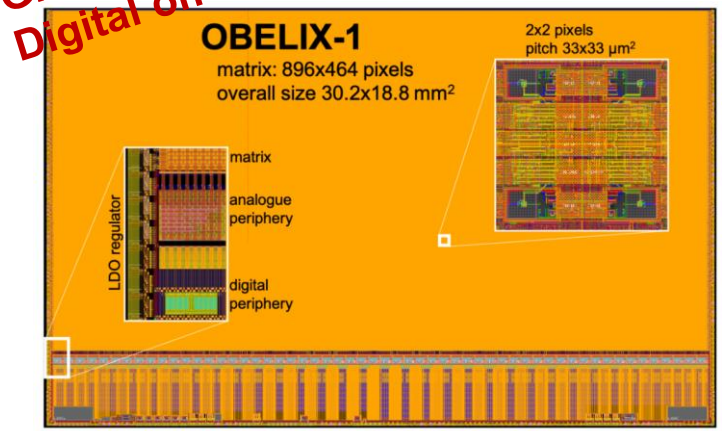
Need expertise on large scale sensors:

- Size vs performances
- Tools and Methodology (DoT, UVM, …)

Application-oriented sensor in Tower 180 nm

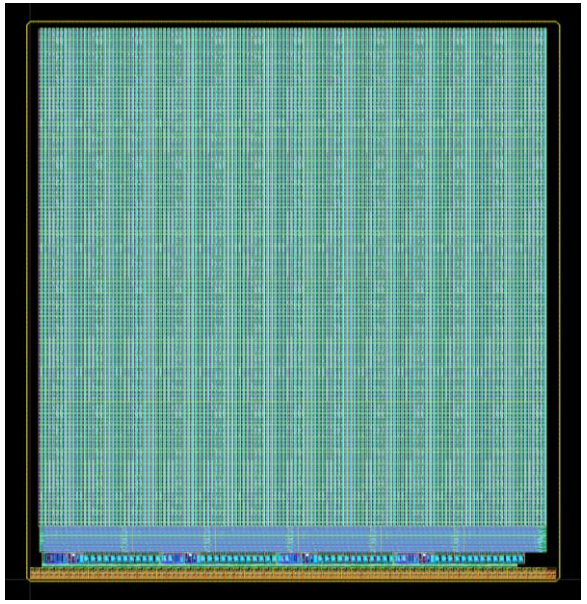
- MIMOSIS — CBM-MVD
  - Fully designed at C4Pi
    - Collaboration with IKFrankfurt & GSI
  - 5 µm — 5 µs — 20 (70) MHz/cm² continuous read-out
    - Modified process & AC-diode (full or partial depletion)
  - Series of submission: 2017 ⟶ 2025
  - More in M. Deveaux's talk
- OBELIX — Belle II-VTX
  - Design within a wide collaboration:
    - Uni.Bergamo, Uni.Bonn, CPPMarseille, Tech.Uni.Dortmund, HEPHY-Vienna , IFIC-Valencia, INFN-Pavia, KEK-Tsukuba
  - 10 µm — 50 ns — 120 MHz/cm² triggered read-out
    - Modified process & DC or AC-diode (full depletion)
  - Started 2022: 1st version in 2024
  - More in M. Babeluk's talk

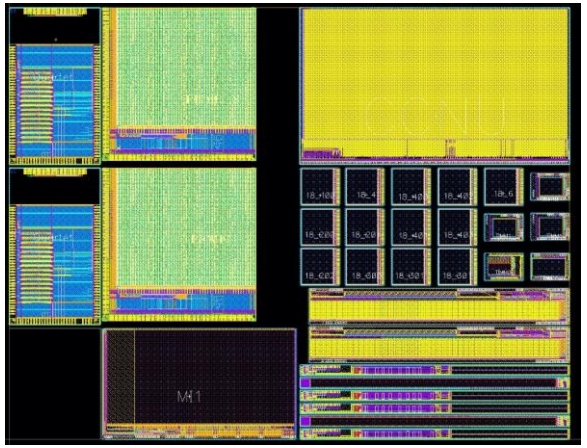
Growing experience in Digital on Top methodology



Technological R&D in Tower 180 nm

- TIIX
  - Small size prototype (5x7 mm^2) for ion tracking & identification
  - Design with: IP2I-Lyon
  - 12 µm / 10 ns / 100 kHz/cm^2 continuous read-out
    - linear dynamic up to ~800 ke-
      for energy measurement over a wide range
    - Modified process (full depletion)
  - Series of submissions: 2020 ⟶ 2024
- QUARTPIC submissions
  - Multi-project engineer runs organised by C4Pi
    - Include internal R&D with small chips
    - Mostly focus on DRD7 activities
  - 1st run 2021 (French projects + China)
  - 2nd run 2024 (French projects + CERN + China)
  - 3rd run under discussion for 2025





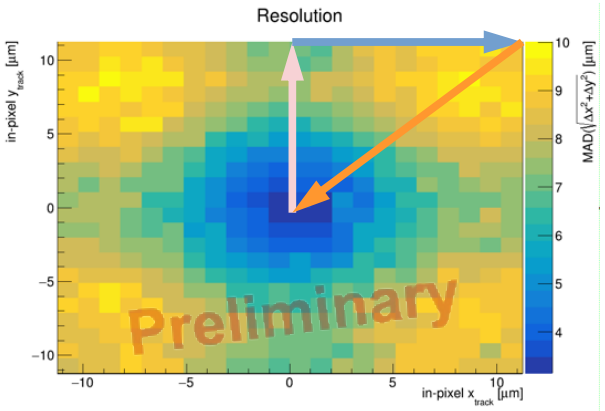
Technological R&D in Tower 65 nm: Charge collection study

- CE65 chips
  - Small matrix (2x2 mm^2) exploring new process
  - Simple architecture:
    - **Analog output**
    - Rolling shutter readout
  - Variations on:
    - Process Standard—Modified—Modified with gaps
    - Diode arrangement (squared or staggered)
    - Pitchs 15—18—22.5 µm
  - Series of 2 submission 2021 and 2023
  - Partners share analysis and measurements
    - IPHC — CTU Prague – UZH Zurich

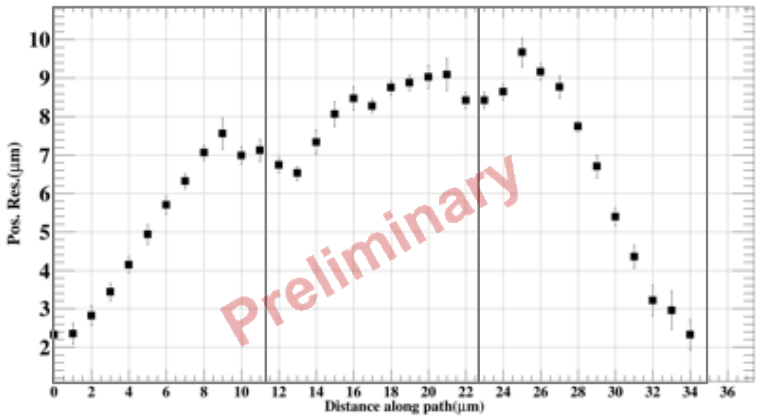
Process	Pitch (µm)	Spatial Res. (µm) Tel. res. Subtracted (2.1 µm)
GAP	22.5	~5.1
GAP	18	~4.1
GAP	15	~3.2
STD	22.5	~2.4
STD	18	~1.8
STD	15	~1.3

Preliminary

Only square diode arrangement

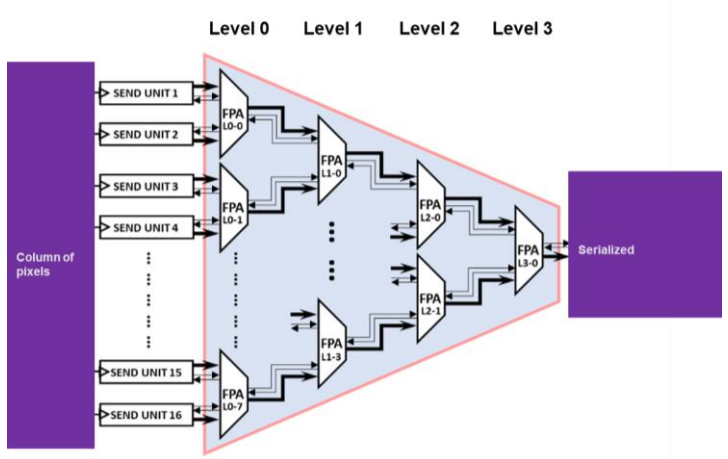


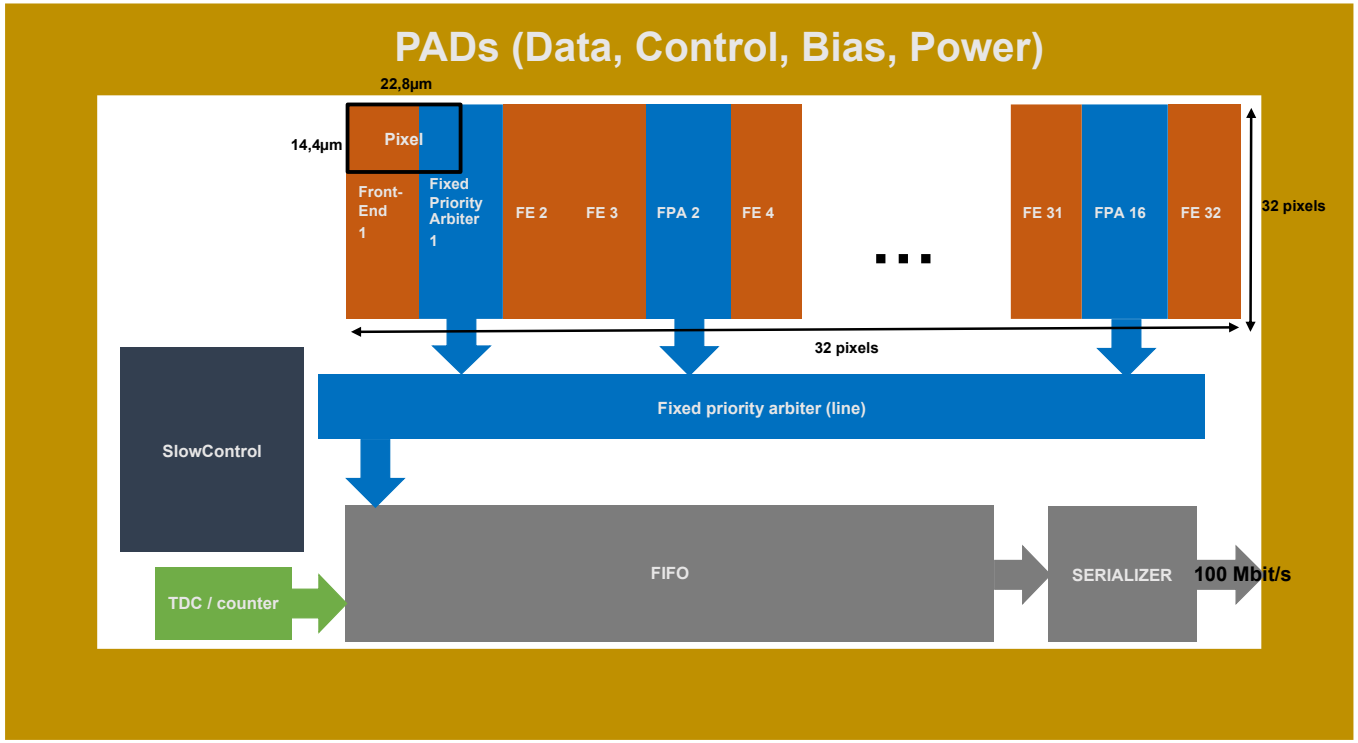
Process — GAP
Pitch — 22.6 µm



Technological R&D in Tower 65 nm: Readout study

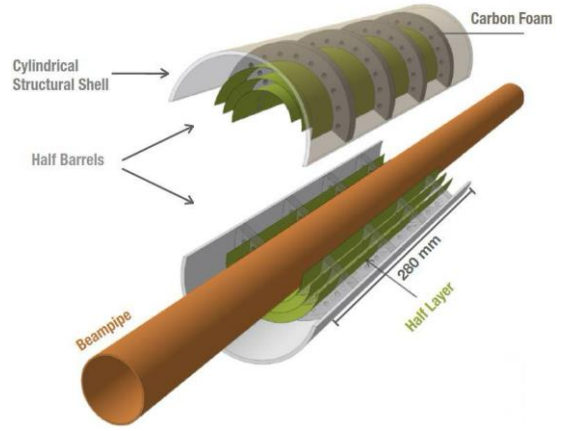
- SPARC
  - Small prototype (2x2 mm^2) for new matrix read-out
  - Design with: IRFU-Saclay
    - Contribution from CERN-EP R&D & ALICE-ITS3 (DPTS pixel front-end)
  - Full asynchronous read-out logic
    - Clockless 20 ns time-stamping
    - ~10 mW/cm^2 in matrix
  - 1st submission 2024



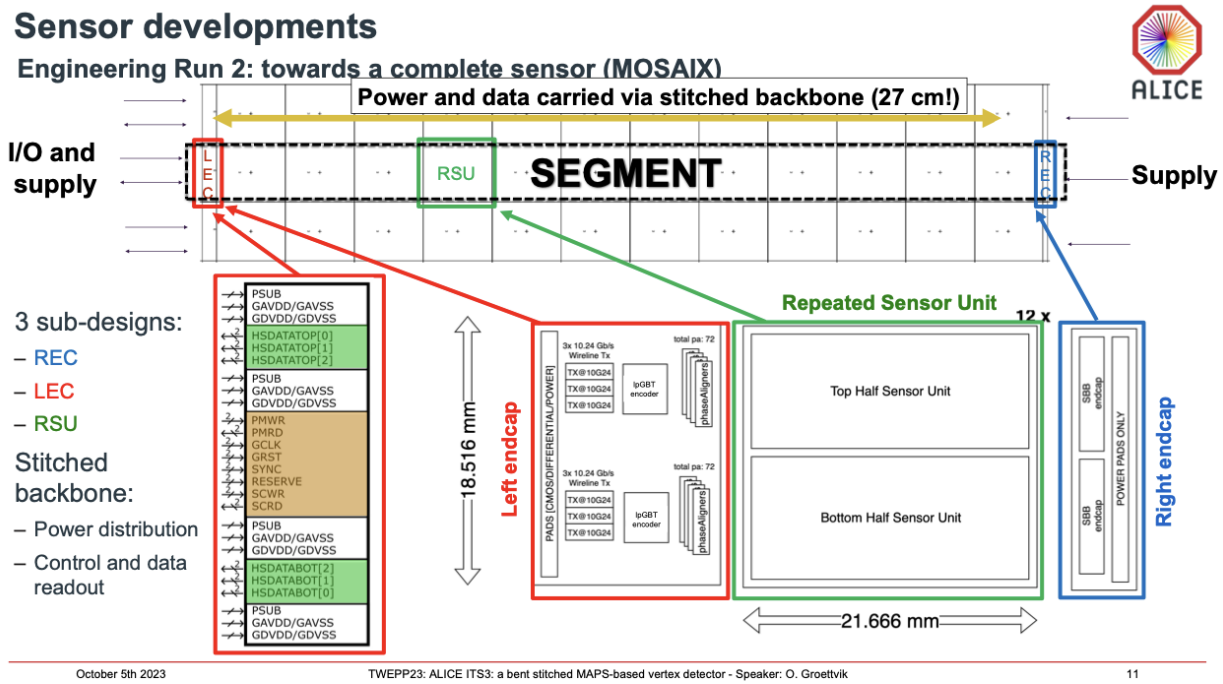


Application-oriented sensor in Tower 65 nm: ITS3

- MOSAIX — ALICE-ITS3
  - Wafer scale sensor ASICs with stitiching
    - Ultra-thin and bendable: 50 µm
    - Tower 65 nm
  - 5 µm — 2 µs — ~6 MHz/cm² continuous read-out
  - Series of submission: 2021 ⟶ 2025
    - Large design team
  - IPHC design effort:
    - Responsibility of matrix integration (DoT)
    - Contribution in analogue biasing



TWEPP23 — O. Groettvik



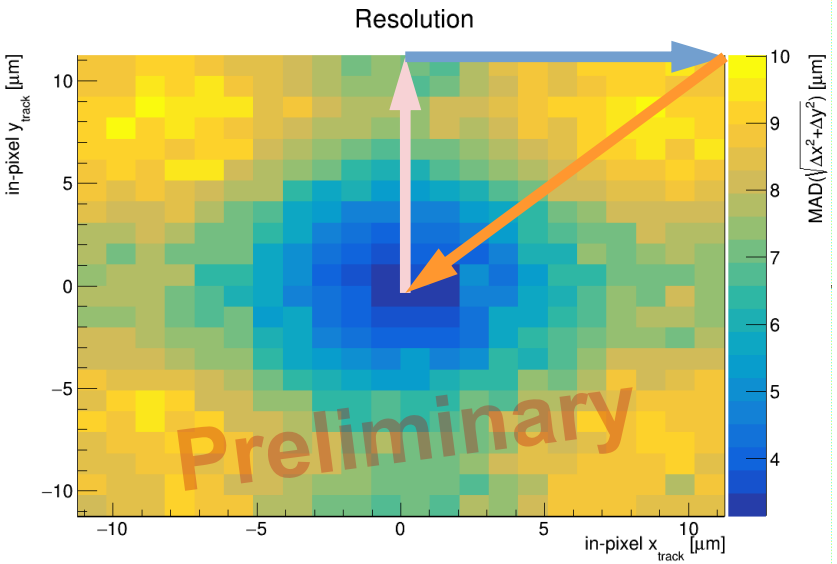
Conclusion

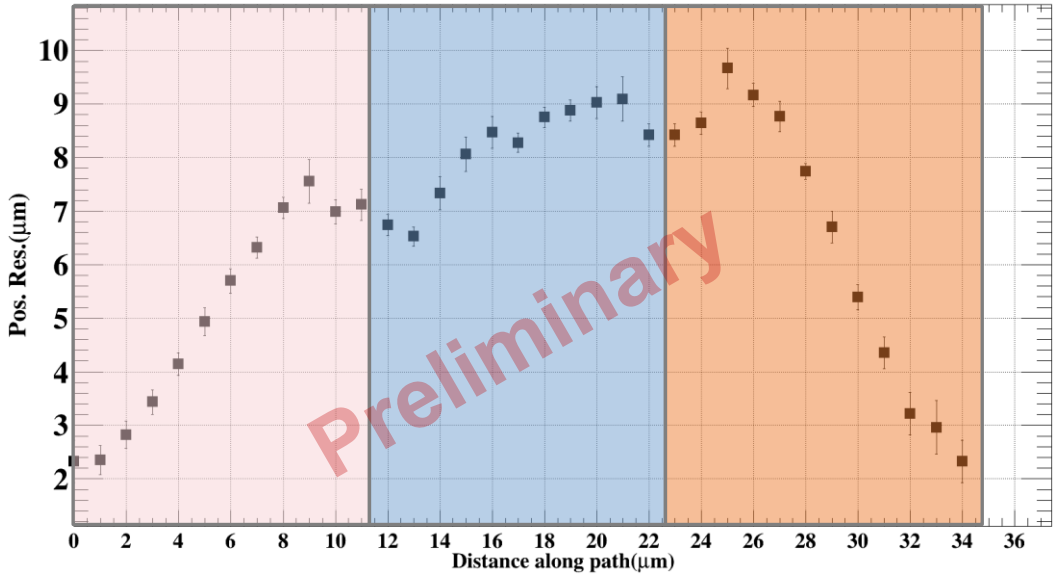
- IPHC has been involved in MAPS R&D since 25 years
  - Strong expertise on several aspects
- Interest in vertexing and tracking development
- Focus on two technologies
  - Tower 180 nm is a well-established technology
  - Tower 65 nm is where future cutting-edge developments are made
- Involvement in
  - DRD3 for RG1 (position resolution) RG3 (readout for large tracking area)
  - DRD7 WG6 for imager technology access

Backup

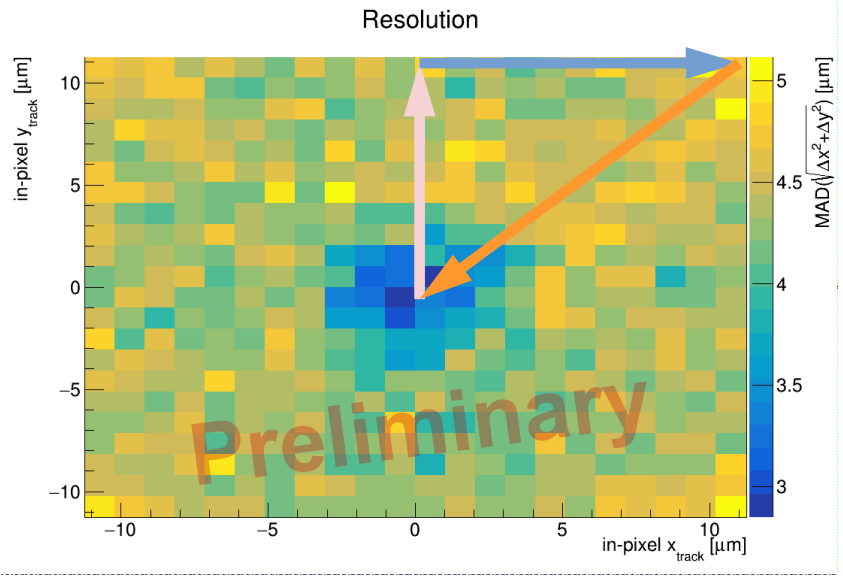
Technological R&D in Tower 65 nm: Charge collection study

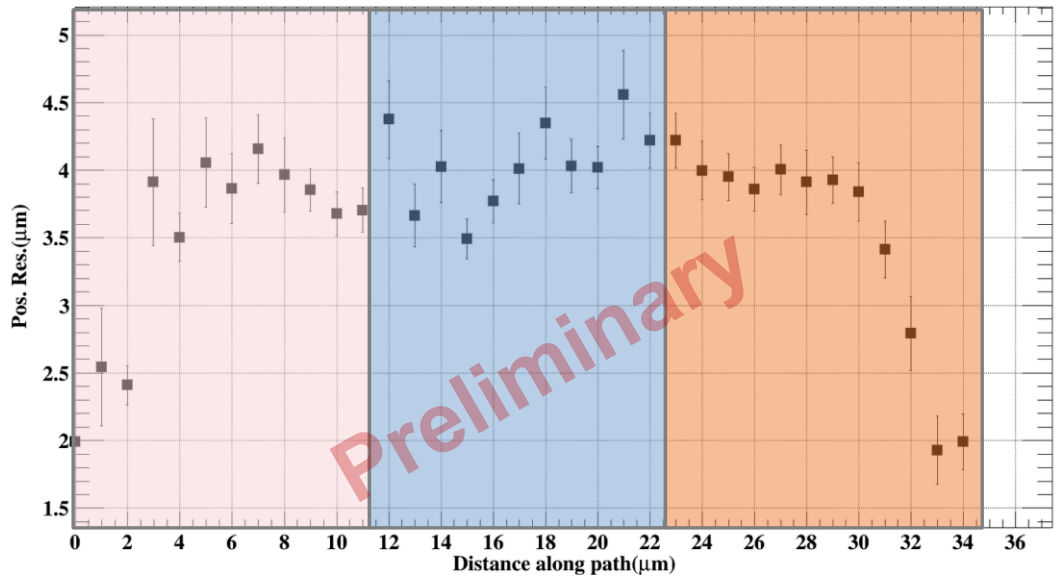
Process — GAP
Pitch — 22.6 µm





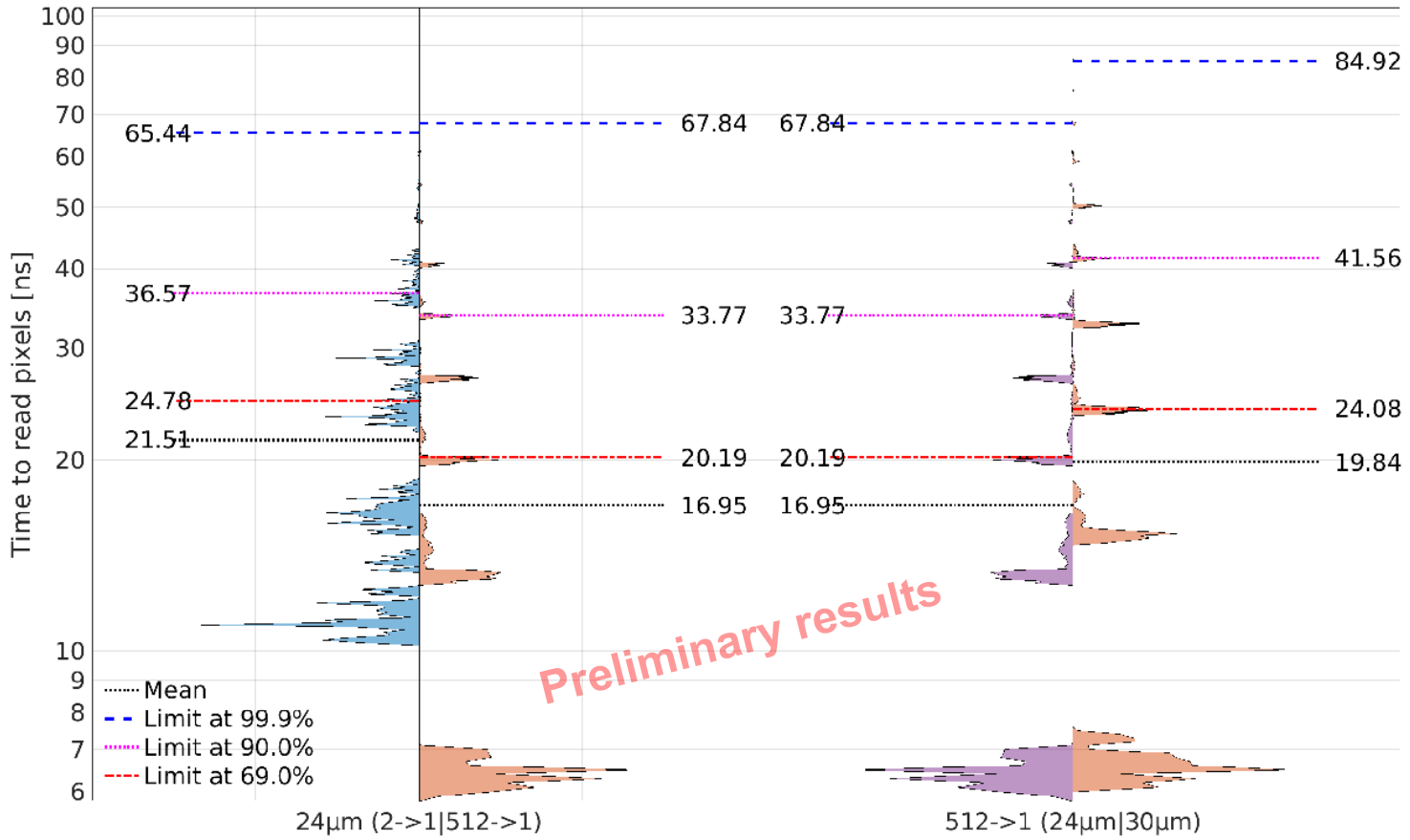
Process — STD
Pitch — 22.6 µm





Technological R&D in Tower 65 nm: Readout study

- Read the event as soon as is available
- Time to read an event for different physical events
  - 2 different topologies
    - 2->1 and 512->1
  - Large number of events are read in less than 7 ns
- Tens of ns time stamping at column level is achievable



J. Soudier PhD