



# Innovations in CMOS Pixel Sensor Technology at IPHC: Projects and Future Prospects

Frédéric Morel on behalf of IPHC teams

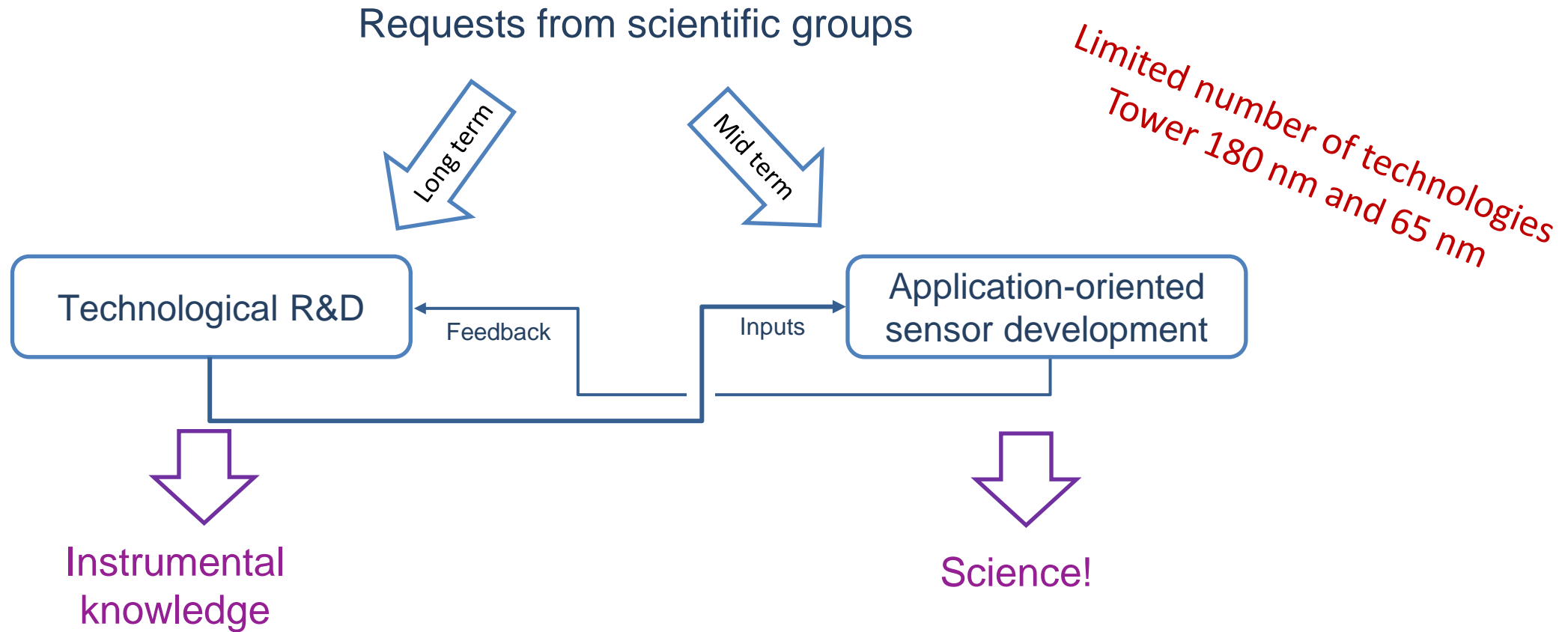
# IPHC has a full range of MAPS expertise

Sensitive layer		Collection node	
In-pixel analogue front-end		Bias monitoring	
Digital conversion		Digitisation	
Digital front-end & back-end		Read-out architecture	
Register Transfer Level		Top description	
Integration		Synthesis, Layout	
Design Rule Checking		Verification	
IP, component creation		Fabrication	
Test systems prototyping		DAQ, Control, data transfert systems design	
Board, flex, detection module design			
Hardware / Firmware / Software design		Test setup intergration	
IP validation		Functional tests	Physical characterisation
Laboratory tests	Beam tests	Production tests	
Board/flex component population		tool design	
ASIC/wafer probe testing		Module validation	
Manual/automatic assembly	Bonding	2D/3D Metrology	

TOOLS & Foundry support

- Based on the expertise of:
  - C4PI: MAPS facility
  - Physics groups: PICSEL (FCC), ALICE, Belle II
- C4PI a board team of engineers and technicians:
  - 6 in analogue design and process
  - 7 in digital design and verification
  - 6 in test and characterisation
  - 3 in microtechnics and integration
  - 5 to 10 students
    - PhD, internships and apprentices
- Physics groups are essential:
  - Scientific drivers
  - Analysis expertise

# C4PI missions



Next generation detectors need new concepts:

- Fast development cycle
- Low risk project

Need expertise on large scale sensors:

- Size vs performances
- Tools and Methodology (DoT, UVM, ...)

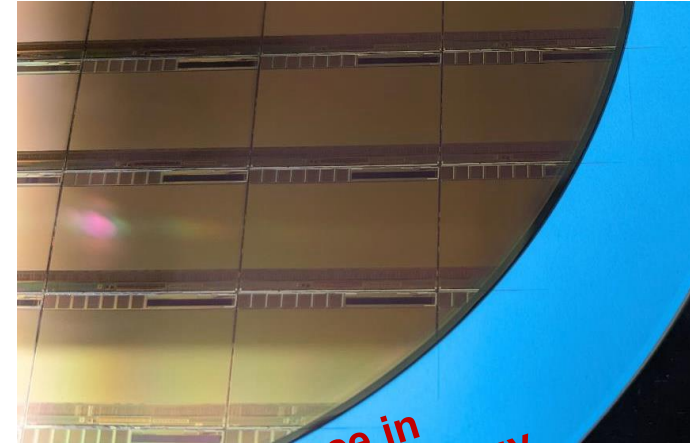
# Application-oriented sensor in Tower 180 nm

## ■ MIMOSIS — CBM-MVD

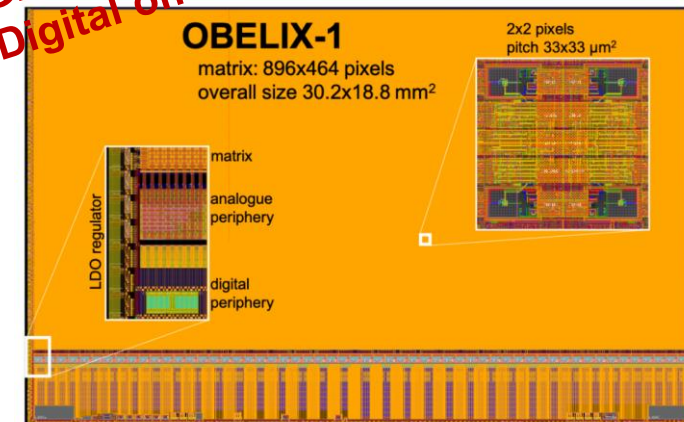
- Fully designed at C4Pi
  - Collaboration with IKFrankfurt & GSI
- $5\ \mu\text{m} - 5\ \mu\text{s} - 20\ (70)\ \text{MHz}/\text{cm}^2$  continuous read-out
  - Modified process & AC-diode (full or partial depletion)
- Series of submission: 2017 → 2025
- More in M. Deveaux's talk

## ■ OBELIX — Belle II-VTX

- Design within a wide collaboration:
  - Uni.Bergamo, Uni.Bonn, CPPMarseille, Tech.Uni.Dortmund, HEPHY-Vienna, IFIC-Valencia, INFN-Pavia, KEK-Tsukuba
- $10\ \mu\text{m} - 50\ \text{ns} - 120\ \text{MHz}/\text{cm}^2$  triggered read-out
  - Modified process & DC or AC-diode (full depletion)
- Started 2022: 1<sup>st</sup> version in 2024
- More in M. Babeluk's talk



*Growing experience in  
Digital on Top methodology*



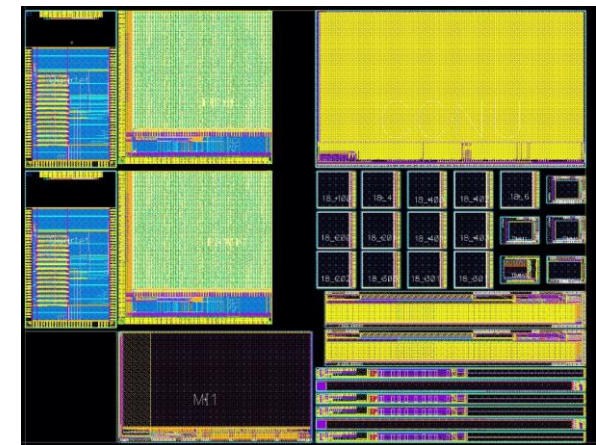
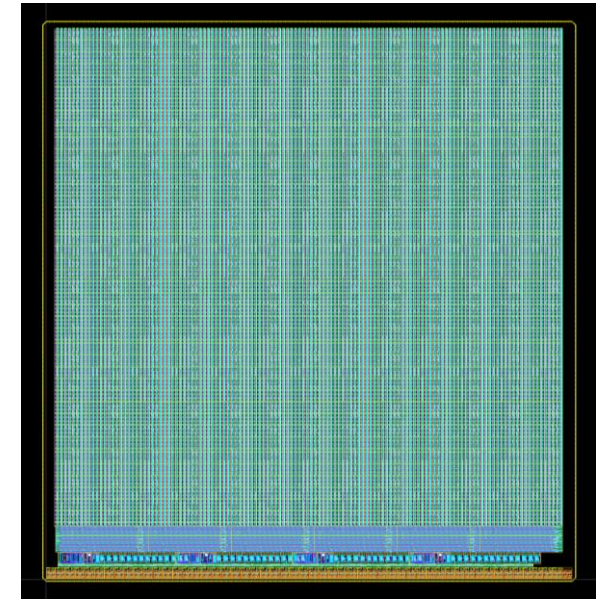
# Technological R&D in Tower 180 nm

## ■ TIIX

- ❑ Small size prototype (5x7 mm<sup>2</sup>) for ion tracking & identification
- ❑ Design with: IP2I-Lyon
- ❑ 12 μm / 10 ns / 100 kHz/cm<sup>2</sup> continuous read-out
  - linear dynamic up to ~800 ke-  
for energy measurement over a wide range
  - Modified process (full depletion)
- ❑ Series of submissions: 2020 → 2024

## ■ QUARTPIC submissions

- ❑ Multi-project engineer runs organised by C4Pi
  - Include internal R&D with small chips
  - Mostly focus on DRD7 activities
- ❑ 1<sup>st</sup> run 2021 (French projects + China)
- ❑ 2<sup>nd</sup> run 2024 (French projects + CERN + China)
- ❑ 3<sup>rd</sup> run under discussion for 2025



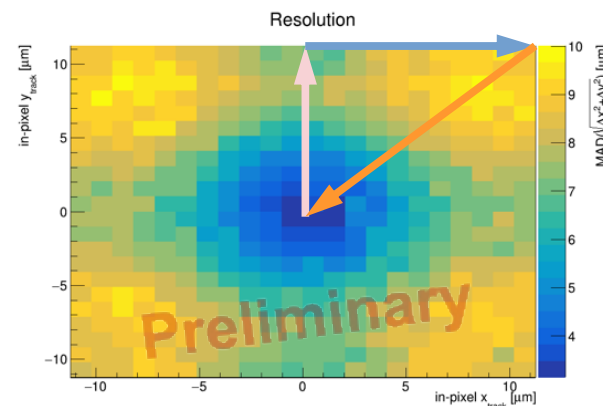
# Technological R&D in Tower 65 nm: Charge collection study

## ■ CE65 chips

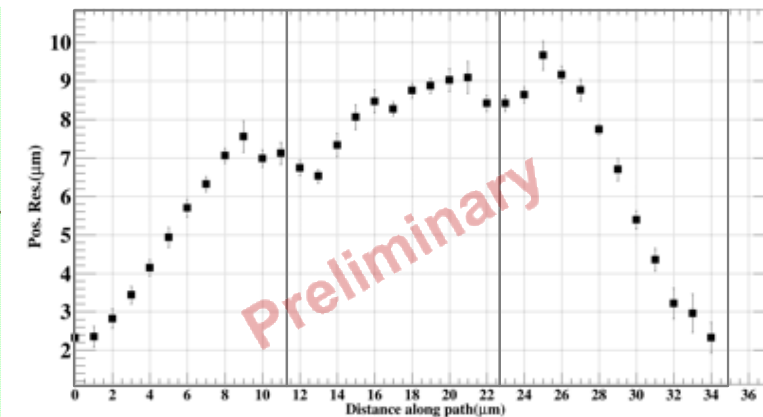
- ❑ Small matrix (2x2 mm<sup>2</sup>) exploring new process
- ❑ Simple architecture:
  - **Analog output**
  - Rolling shutter readout
- ❑ Variations on:
  - Process Standard—Modified—Modified with gaps
  - Diode arrangement (squared or staggered)
  - Pitches 15—18—22.5 μm
- ❑ Series of 2 submission 2021 and 2023
- ❑ Partners share analysis and measurements
  - IPHC — CTU Prague – UZH Zurich

Process	Pitch (μm)	Spatial Res. (μm) Tel. res. Subtracted (2.1 μm)
GAP	22.5	~5.1
GAP	18	~4.1
GAP	15	~3.2
STD	22.5	~2.4
STD	18	~1.8
STD	15	~1.3

**Only square diode arrangement**



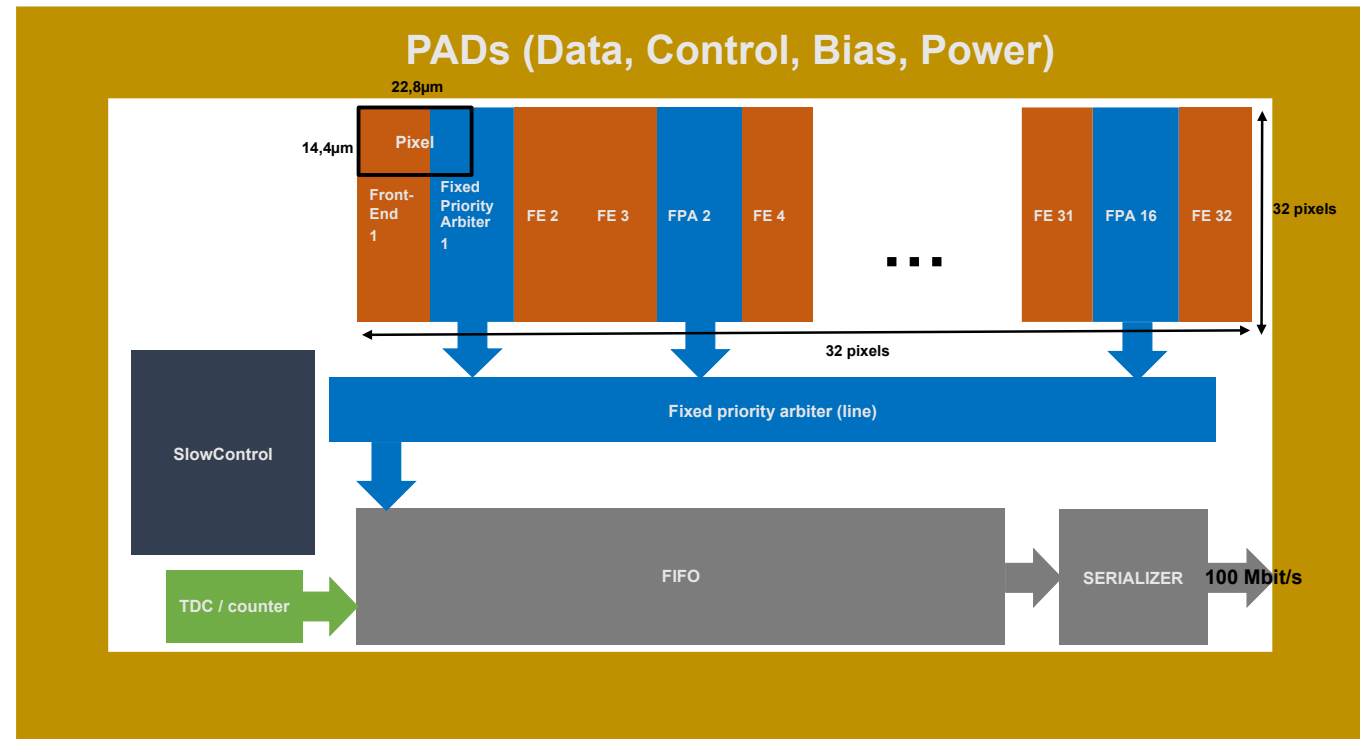
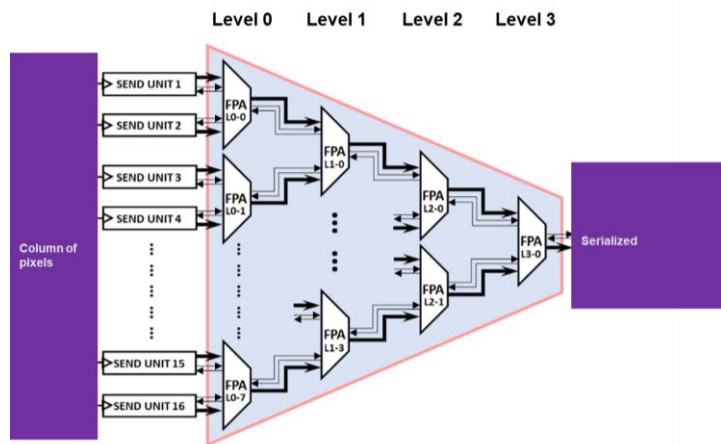
Process — GAP  
Pitch — 22.6 μm



# Technological R&D in Tower 65 nm: Readout study

## ■ SPARC

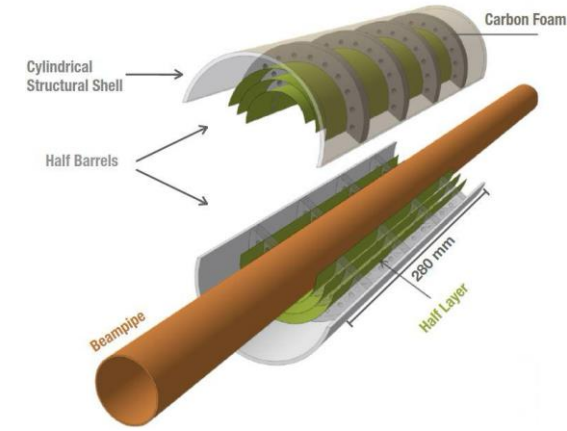
- ❑ Small prototype (2x2 mm<sup>2</sup>) for new matrix read-out
- ❑ Design with: IRFU-Saclay
  - Contribution from CERN-EP R&D & ALICE-ITS3 (DPTS pixel front-end)
- ❑ Full asynchronous read-out logic
  - Clockless 20 ns time-stamping
  - ~10 mW/cm<sup>2</sup> in matrix
- ❑ 1st submission 2024



# Application-oriented sensor in Tower 65 nm: ITS3

## ■ MOSAIX — ALICE-ITS3

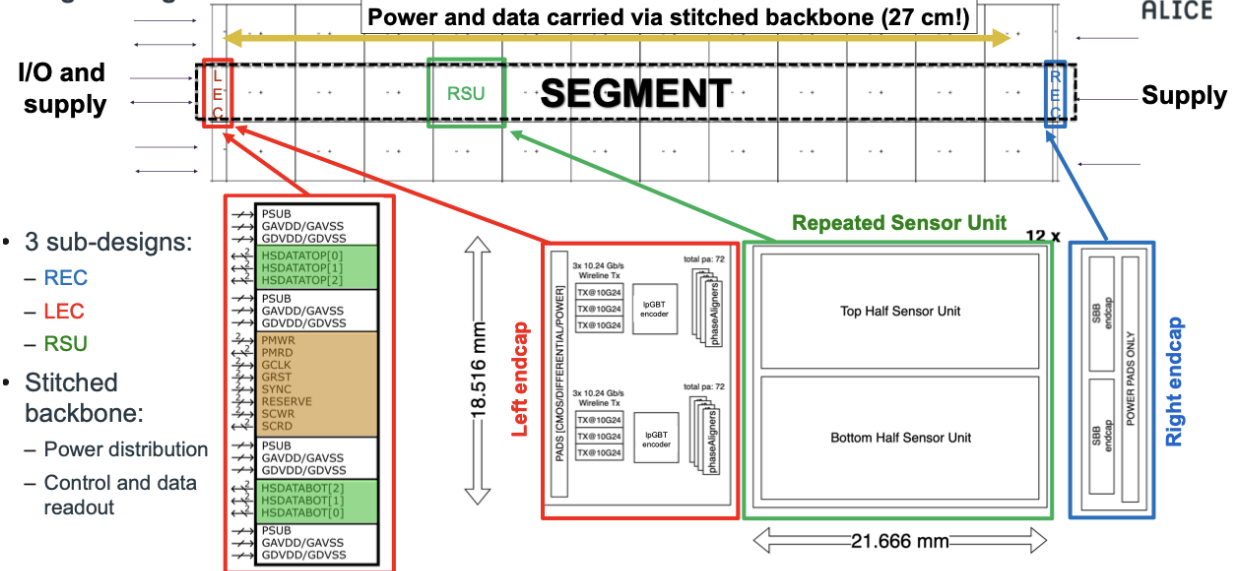
- Wafer scale sensor ASICs with stitching
  - Ultra-thin and bendable: 50  $\mu\text{m}$
  - Tower 65 nm
- 5  $\mu\text{m}$  — 2  $\mu\text{s}$  —  $\sim 6 \text{ MHz/cm}^2$  continuous read-out
- Series of submission: 2021  $\rightarrow$  2025
  - Large design team
- IPHC design effort:
  - Responsibility of matrix integration (DoT)
  - Contribution in analogue biasing



TWEPP23 — O. Groettvik

## Sensor developments

Engineering Run 2: towards a complete sensor (MOSAIX)



- 3 sub-designs:
  - REC
  - LEC
  - RSU
- Stitched backbone:
  - Power distribution
  - Control and data readout

October 5th 2023

TWEPP23: ALICE ITS3: a bent stitched MAPS-based vertex detector - Speaker: O. Groettvik

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# Conclusion

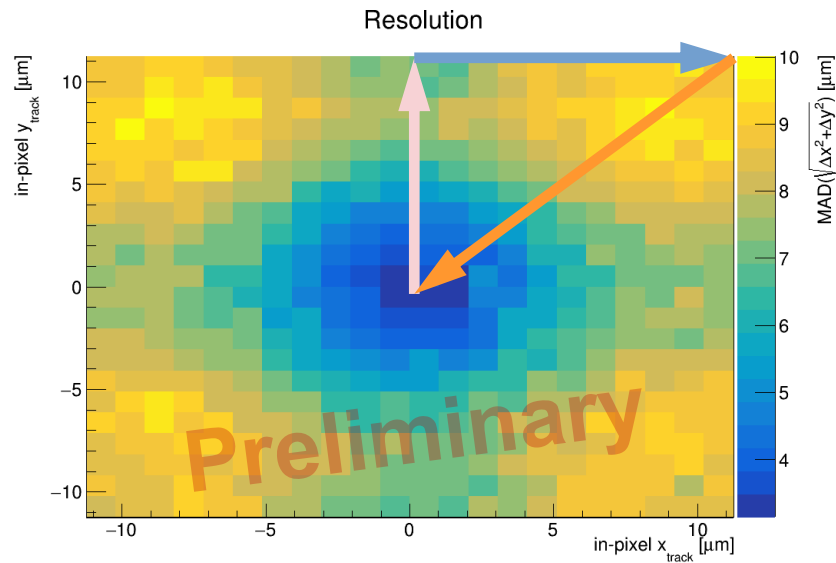
- IPHC has been involved in MAPS R&D since 25 years
  - Strong expertise on several aspects
- Interest in vertexing and tracking development
- Focus on two technologies
  - Tower 180 nm is a well-established technology
  - Tower 65 nm is where future cutting-edge developments are made
- Involvement in
  - DRD3 for RG1 (position resolution) RG3 (readout for large tracking area)
  - DRD7 WG6 for imager technology access



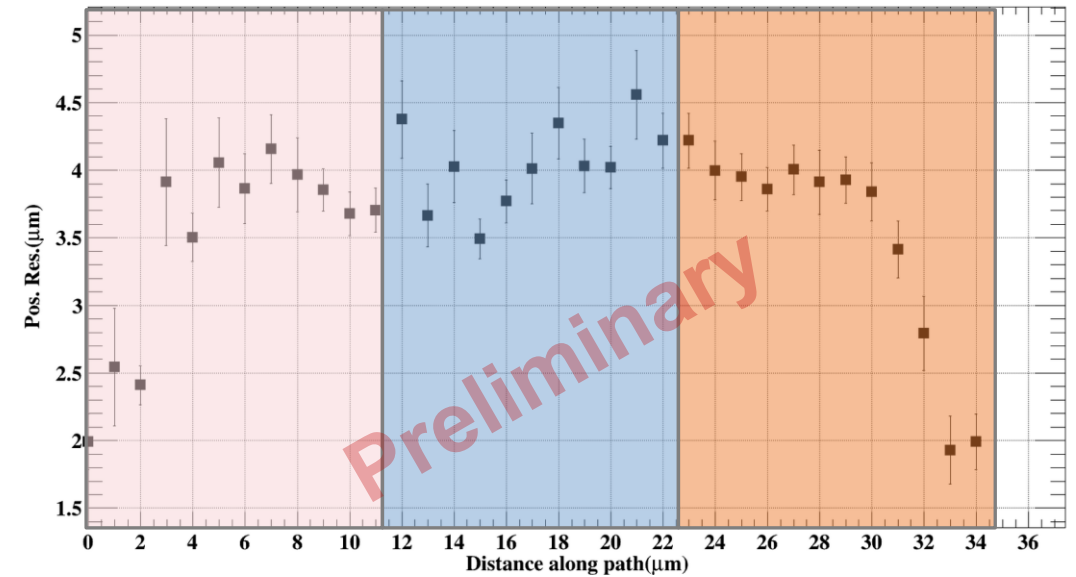
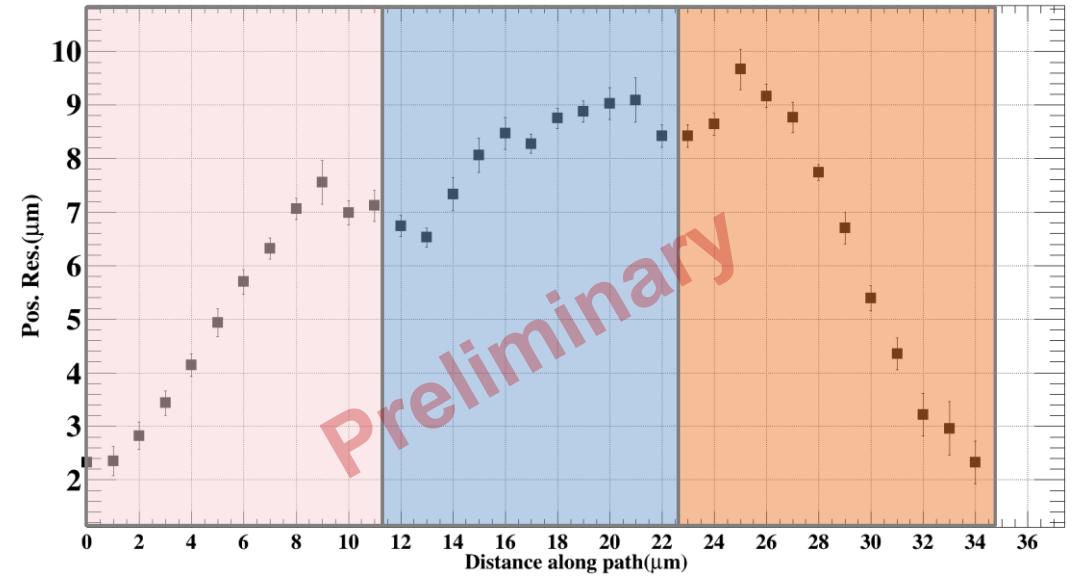
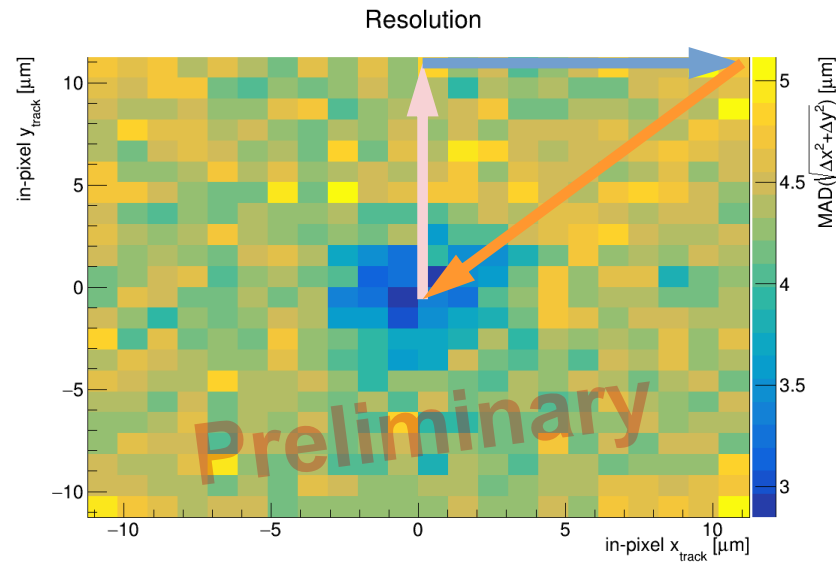
# Backup

# Technological R&D in Tower 65 nm: Charge collection study

Process — GAP  
Pitch — 22.6  $\mu\text{m}$

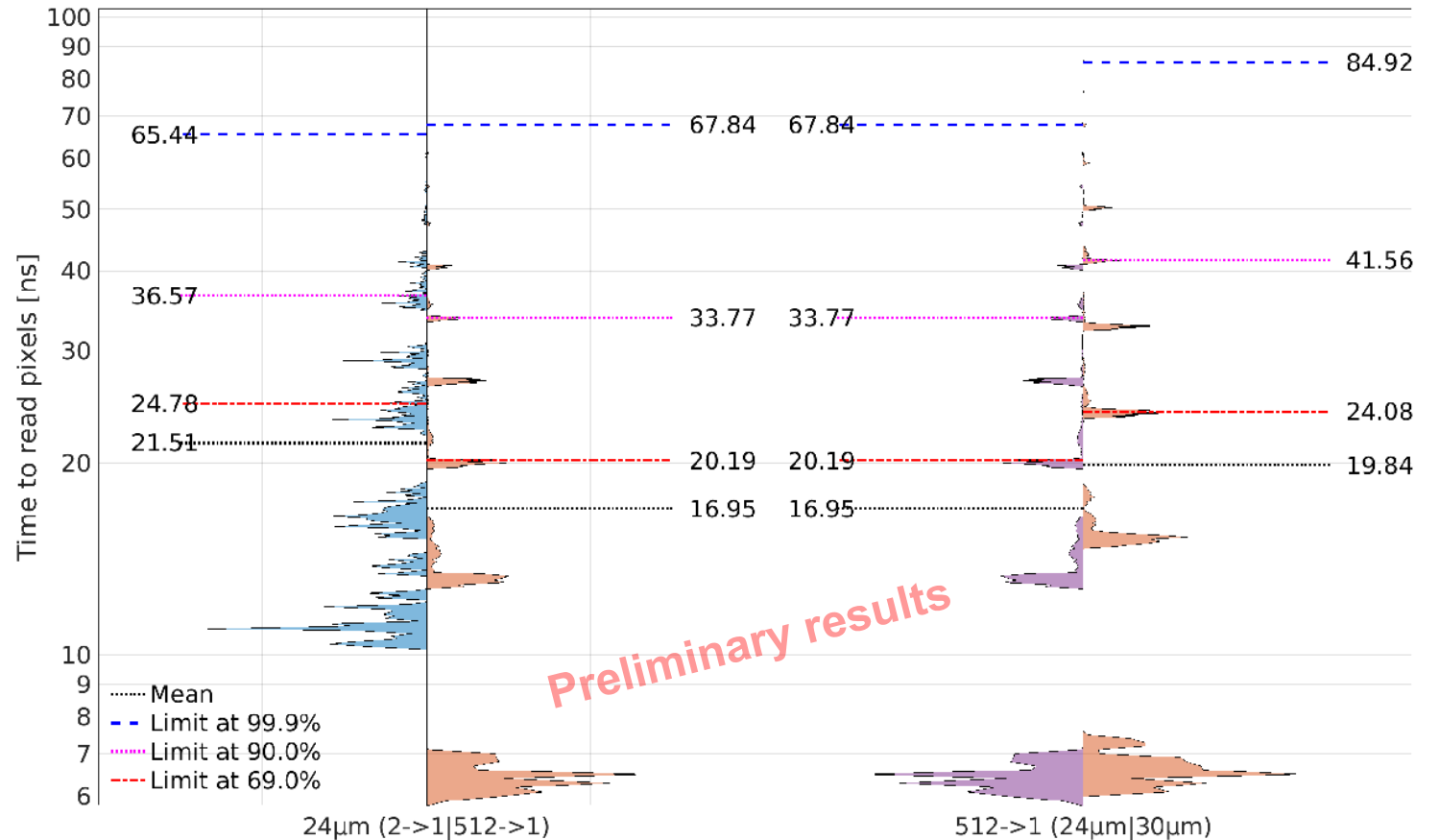


Process — STD  
Pitch — 22.6  $\mu\text{m}$



# Technological R&D in Tower 65 nm: Readout study

- Read the event as soon as is available
- Time to read an event for different physical events
  - 2 different topologies
    - 2->1 and 512->1
  - Large number of events are read in less than 7 ns
- Tens of ns time stamping at column level is achievable



J. Soudier PhD