Large fill factor DMAPS development at PSI

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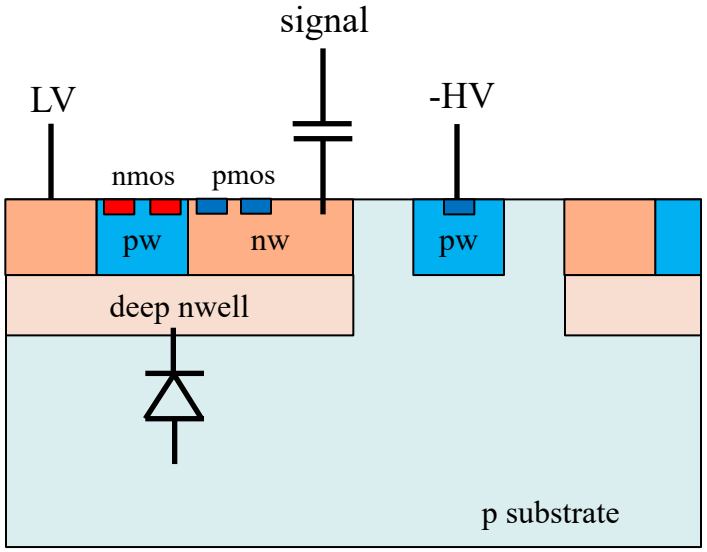
1st DRD3 week on Solid State Detectors R&D

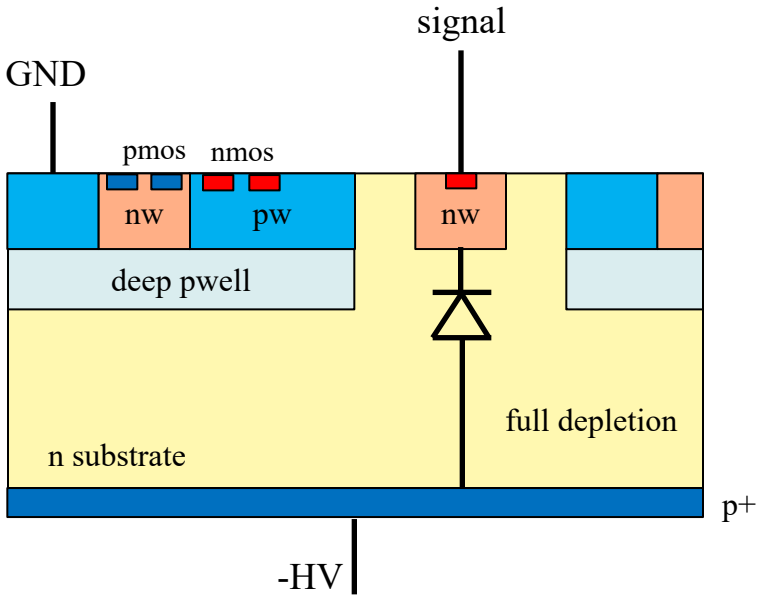
17. June 2024

Motivation

- PSI high energy physics group has developed the readout chip, the sensor and a bump bonding process for the CMS pixel detector phase 0 and phase I
  - Gained large experience in mixed signal chip design and systems design
  - No chip development for phase II upgrade
- Started general R&D on DMAPS for future applications in smaller experiments
  - A few potential applications for inhouse experiments at PSI
  - Targeting also applications outside the field of particle physics (solid state physics and environmental research)
  - Main motivation is low material budget, simpler detector design without bump bonding
  - Typical specifications are: relatively low data rates, low radiation environment, low power (operated in vacuum) and timing information of O(100-200ps)

Reminder: DMAPS Types





Large fill factor (area of collection electrode)
Large sensor capacitance

- higher noise, power needs
- Shorter drift paths, higher and more uniform drift field → +for timing, + rad hardness
- X-talk issues from electronics into collection node

TSI, AMS, LFoundry 150

Small fill factor
Small sensor capacitance

- less noise, power needs
- Fast and larger signals → + for timing
- Longer drift paths and low field regions → -for timing, - rad hardness

LFoundry 110, ESPROS, TowerJazz

History

- Started with general R&D in 2019
  - Gain experience with DMAPS
  - Gain experience with ToA measurements (time of arrival)
  - Combine the two above

- Prototype test chips in two technologies
  - Small fill factor design → LF 110 (MoTiC)
    - Modified CMOS process in collaboration with INFN
    - Ph. D. thesis Stephan Burkhlater: https://doi.org/10.3929/ethz-b-000648047
    - Vertex2023 A. Ebrahimi: https://agenda.infn.it/event/35597/sessions/27384/#20231018
    - Not covered in this talk. Currently no work ongoing
  - Large fill factor → TSI 180 (TSI-R4S), later switched to LF15A
    - Subject of this talk

Large fill factor design

- TSI 180nm HV CMOS process
- Received first chip with sensor (high res wafer) in 3/2023
- Desy beam test in 6/2023
- Learned a lot about the first prototype
  - X-talk issue(s) identified (as other groups working with large fill factor designs reported)
  - With some operational tricks reached threshold as low as 1200e- (would not be possible with full scale chip and high data rate)
  - Data quality nevertheless not very good. Spatial resolution not better than binary. Analysis ongoing.
- Wanted to address these issues in 2nd iteration
- During design phase TSI went out of business 11/23

Translation to LF15A

- Alternatively AMS (fully compatible to TSI) could produce it
  - No PDK available yet. Will not submit a design without full simulation in original PDK
  - Unclear how the availability is in the future

- Looked into LF15A
  - Very similar process
  - Used in HEP detector community
  - Only one MPW this year (May).
  - Needed fast decision and translation of TSI design
  - Redesign turned out to be straight foreward and rather quick. But again first time submission from us in this technology.

    → Some question marks.

    →No large area chip, need some experience first in MPW.

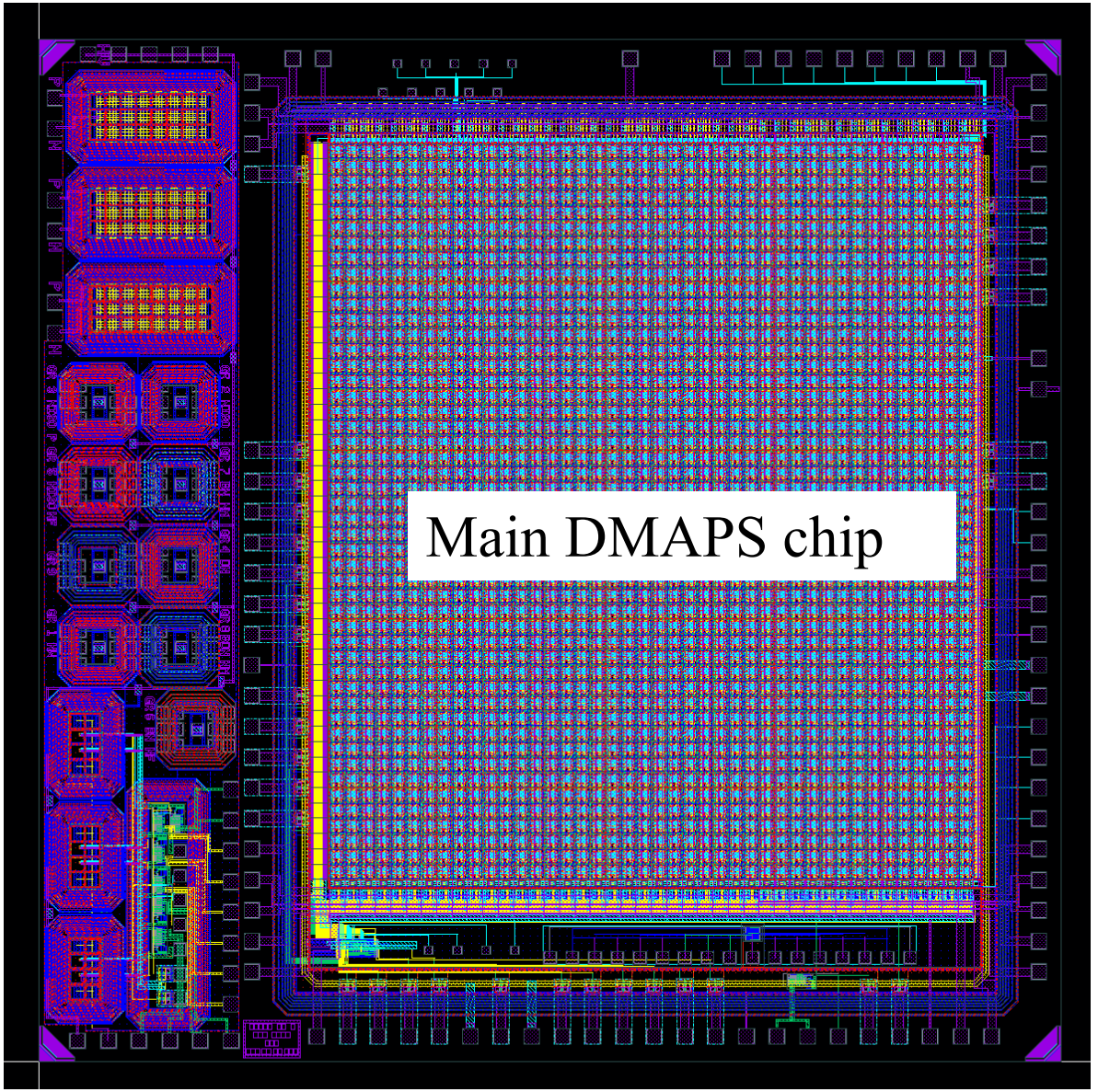
May MPW Submission

- Tape out date was May 6 2024
- MPW with 5x5mm^2 area
- 4x5 mm^2 DMAPS chip
- 1x5mm^2 sensor test structures
- 6 metals, deep N-well for charge collection and isolation, deep P-well for isolation
- High res wafers (~3 kOhm cm) supplied by LFoundry
- Post processing:
  - Thinning to 150 um:~12ke- signal (thinner sensors possible, but risk of breaking wafer increases)
  - backside p+ implant (much more uniform drift field, overdepletion possible→velocity saturation. Good for timing)
  - backside metalisation (protection from very sensitive back side)

Sensor variations

Guard ring variations

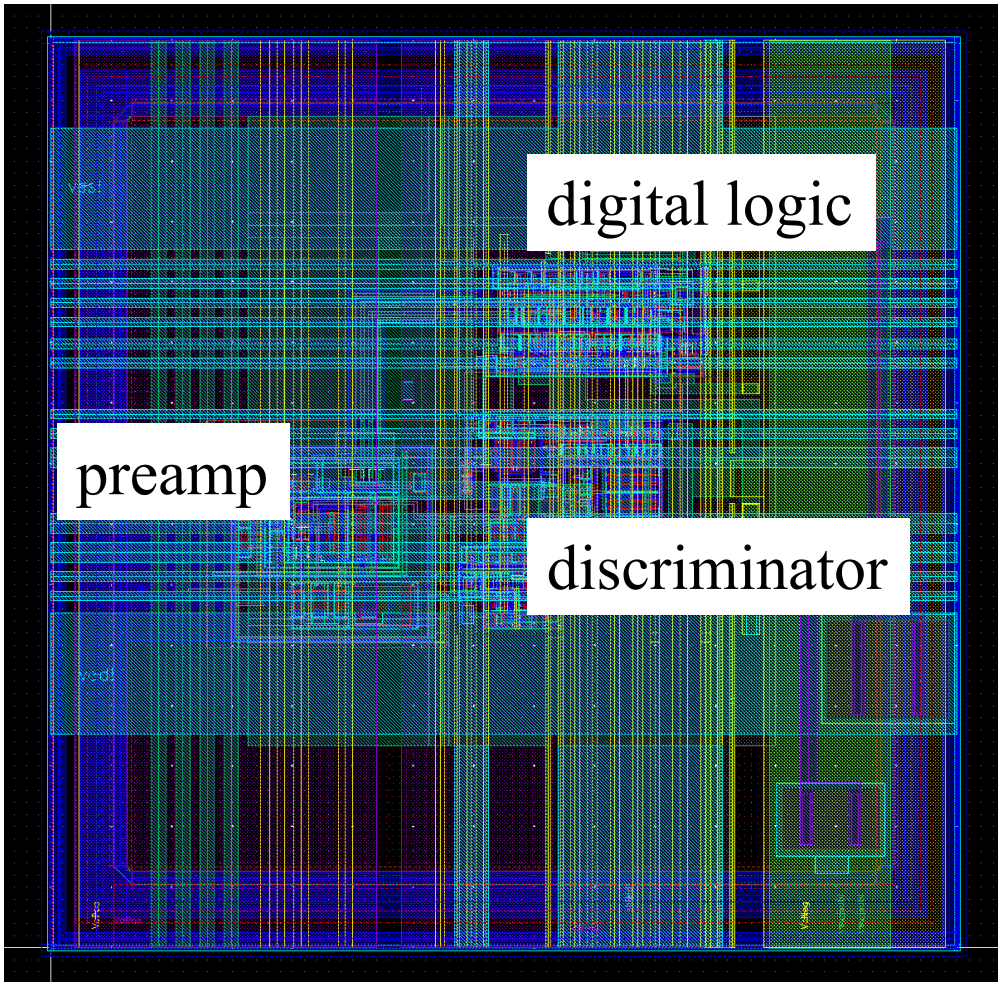
Edge TCT



DMAPS chip Panther

- 75µm x 75µm pixel.
- 48 rows, 3x14 columns:
  - 3 flavors of preamps, optimized for best timing, lowest power and highest S/N
  - No universally best preamp possible. Need to choose/optimize for each specific application
- Pixel has preamp, tunable discriminator, digital logic (kept minimal) and S&H circuit with analog PH readout
- TDC per column
- Triggered sequential, zero-suppressed readout
- Trigger output
- Most digital activity moved to col/row periphery. X-talk is a major issue in this technology!
- Enormous effort made to shield/decouple signals from extremely sensitive input node → my main concern

LF15A pixel cell



- 75µm x 75µm pixel
- 3 flavours of preamps
- Discriminator with global threshold and 3 local trim bits, mask bit
- Sample & hold circuit for analog PH readout
- Injection circuit, analog and digital (for timing calibration)
- Column length: 48 pixel, ~0.36mm

Simulated timing performance

- Rely on post layout simulation. Have to learn how good this models reality (our first submission).
- Best case with high power setting (~640mW/cm^2)
- Timewalk >3ke- at threshold of 1.5ke-: 5ns
  - With 6 bit PH measurement a time resolution of <100ps is possible
- Jitter: estimated as risetime/(S/N)
  - For 6ke- signal (50% charge sharing): risetime=2.2ns, S/N=16.5
  - Jitter <140ps
- Signal distortion from fluctuation of charge deposition/ drift field distortion: not known yet. Needs to be measured.
- Signal delay difference in column <1ns, can be calibrated
- Overall hope for time resolution O(200ps)

Outlook

- I expect the chips back by the end of the year (no dates known so far)
- Hopefully it works as expected. X-talk could be a major issue.
- If we reach a threshold <2ke-, X-talk is under control, simulation models and parasitics describe reality well we will continue developing a large area chip for real applications
- In the meantime we are studying specifications of potential applications and develop a strategy how to cover this. Potential applications at PSI are:
  - MuEDM, MuSR, PIONEER, Muography, many small scale experiments and instrumentation
- I am carefully optimistic that with this chip we can leave the steepest part of the learning curve behind us and can start to develop real detector devices.
- We would love to contribute to this community in the future and are open for any kind of collaboration