The ATLASPIX3 CMOS pixel sensor and module performance

DRD3 Week

CERN, 17 June 2024

Attilio Andreazza - Università di Milano and INFN

For the ATLASPIX3 Silicon Tracker community

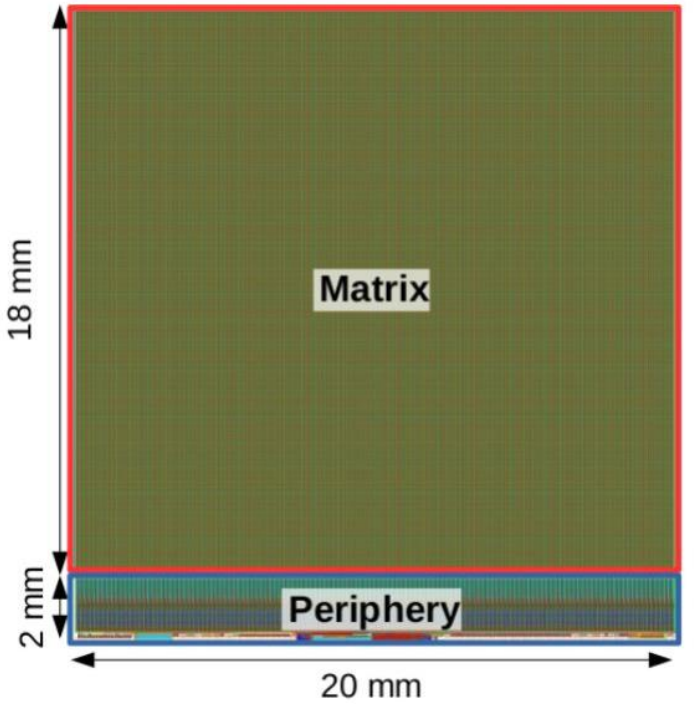
UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

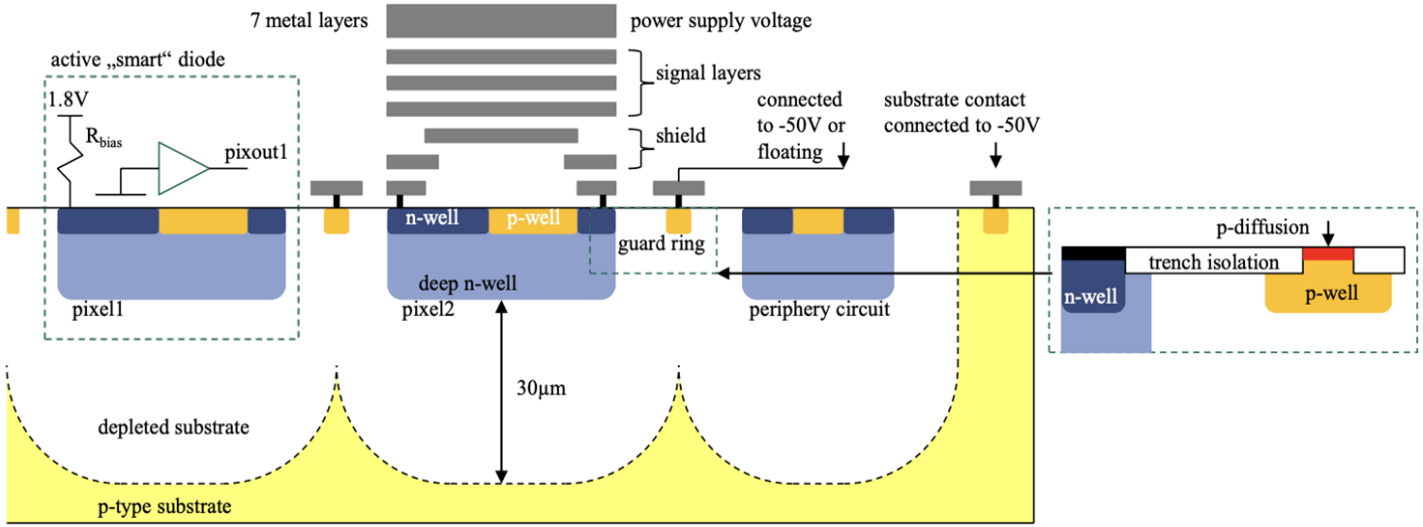
Silicon Tracker Community

- China, INFN, KIT, UK Collaboration
- Groups interested in large area tracking systems for future Higgs Factories:
  - Silicon layers in front of central gas chambers
  - Silicon wrapper outside the central gas chamber (50-100 m^2)
  - Full Silicon tracker
- Large area of Depleted CMOS Pixel Sensors
- Demonstrate the detector concept using existing sensor ATLASPIX3
  - aggregate sensors in larger area modules
  - assemble the detector in stavelets for system tests (DAQ and services)
- In parallel improving the sensor technology to the e^+e^- collider environment
  - **see this afternoon proposal**

ATLASPIX3

- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout





Laboratory readout systems

GEneric Configuration and COntrol System

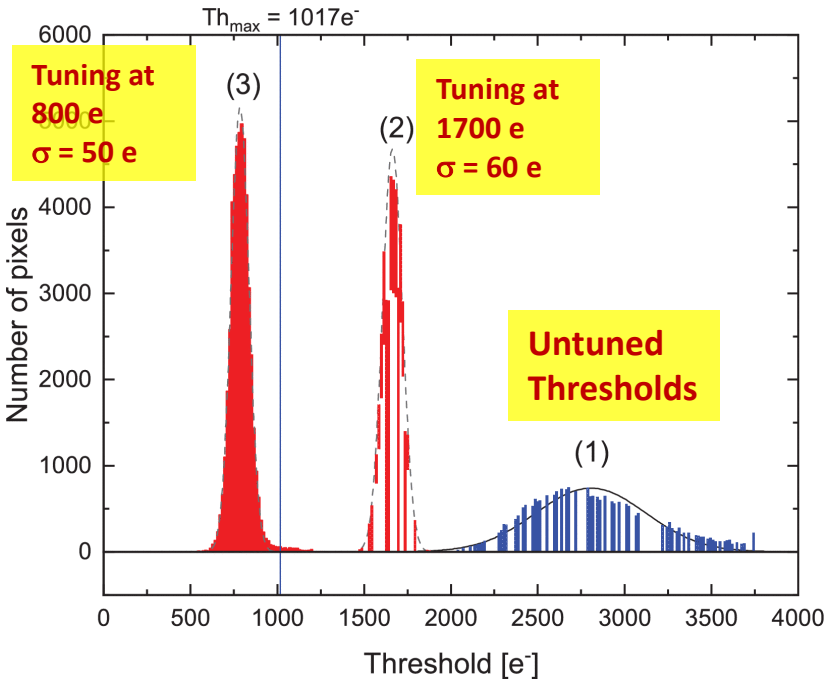
- Versatile system for application with different chips
- Developed by KIT for their sensor development
- GECCO board:
  - **LPC-FMC** connector (160 pins) **to FPGA** readout board (Nexys Video with Xilinx Artix-7)
  - **PCIe x16** connector (164 pins) **to DUT**
  - 10 power connection + HV
  - Expensive components (DACs, injection circuit) on reusable board
  - Test points for all pins
- Controlling up to 4 ATLASPIX3 powered in parallel
  - managing 4-layer single-chip telescope
  - or a 4-chips module

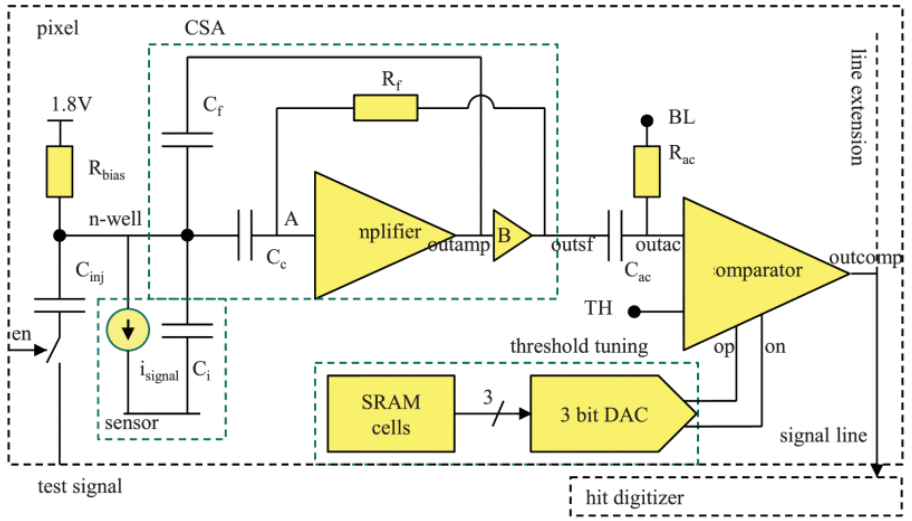
GECCO

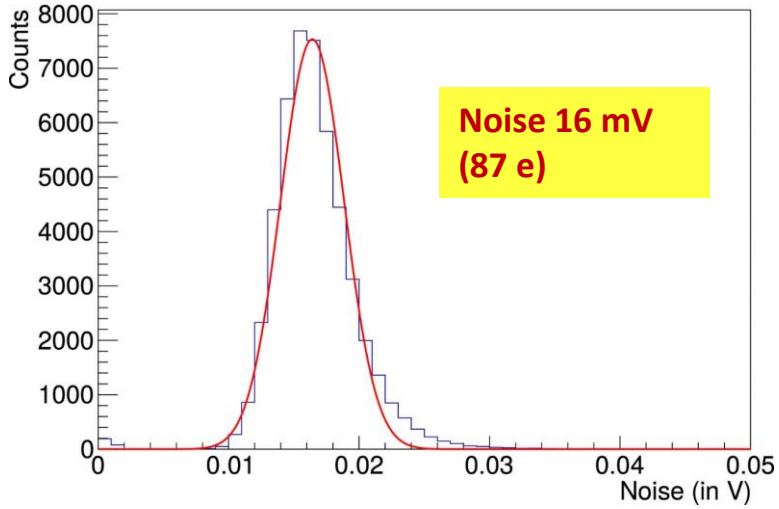
ATLASPIX3 Performance

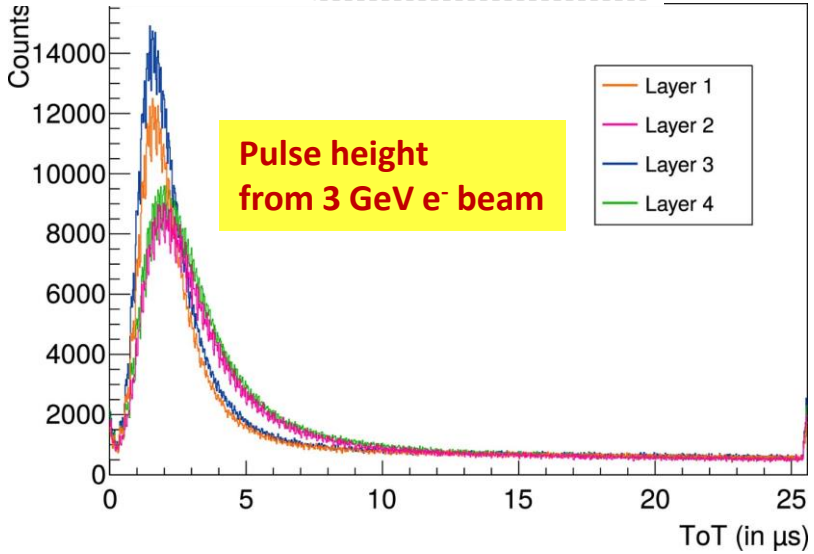
Pixel layout:

- Charge amplifier followed by a comparator
- Threshold tunable by a 3-bit DAC
- Pulse height measurement via 8-bit Time-over-Threshold





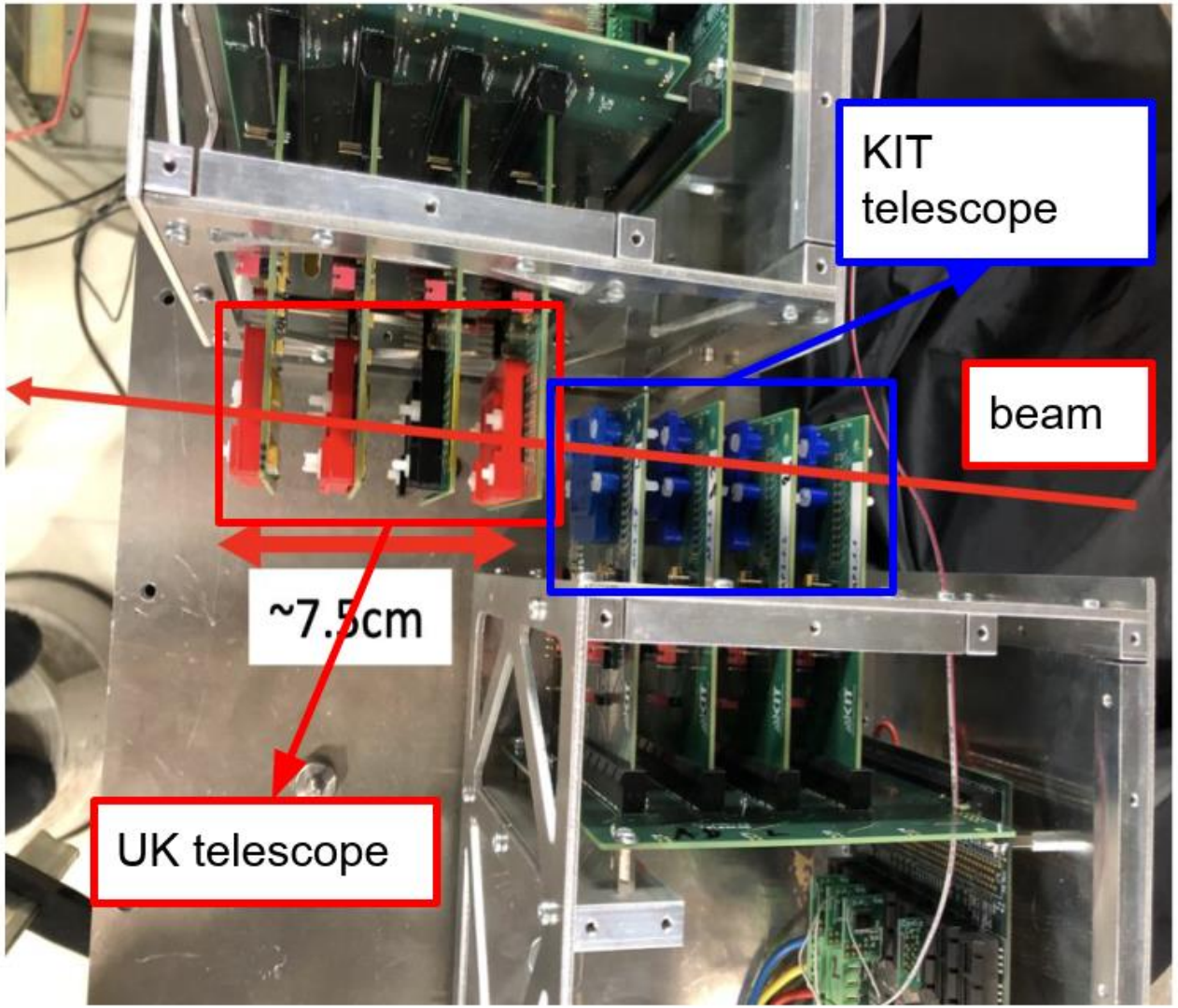




I. Peric et al., IEEE Journal of Solid-State Circuits, vol. 56, no. 8, pp. 2488-2502

R. Schimassek et al., NIM A 986 (2021) 164812

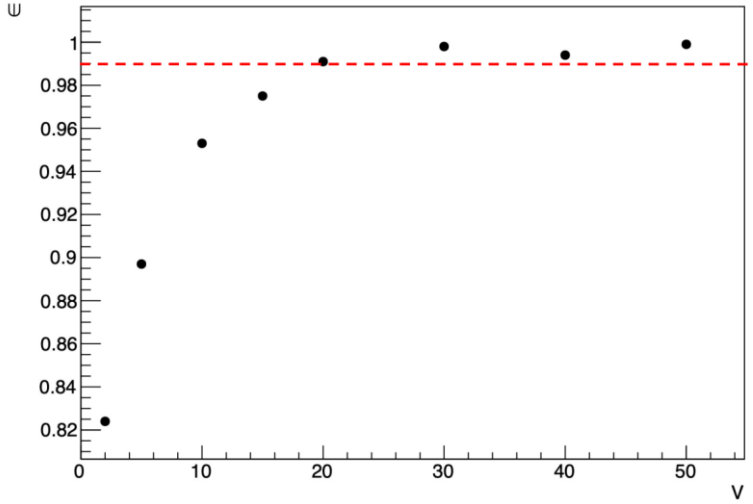
ATLASPIX3: DESY testbeam

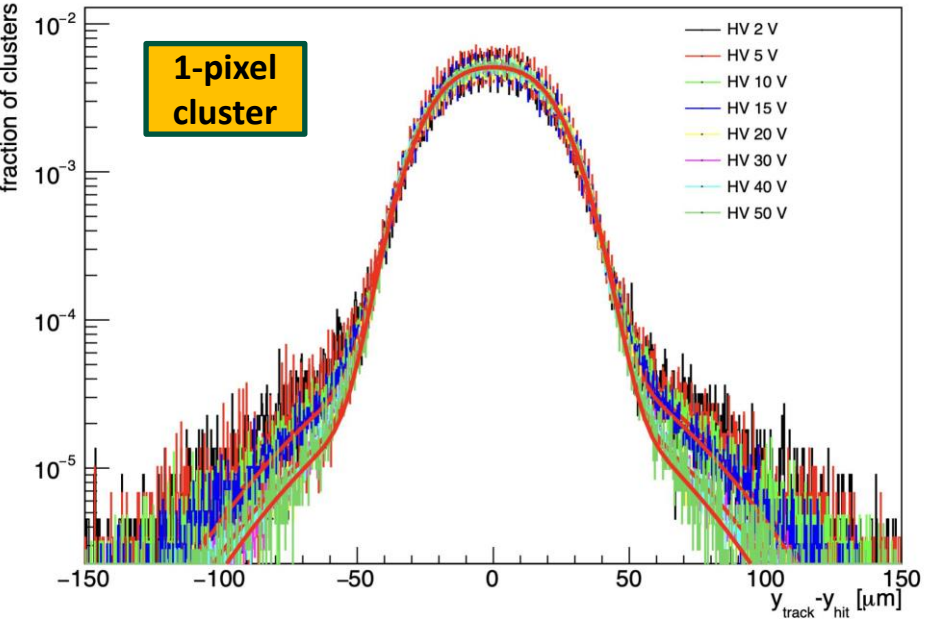


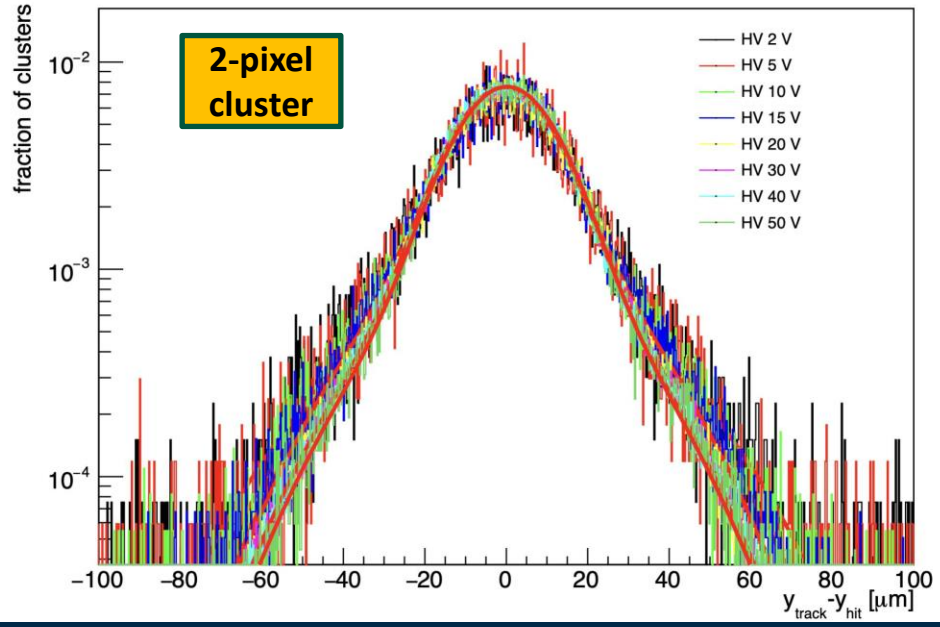
- Two telescopes (**KIT** and **UK**) in standalone systems tested at **DESY** with electron beams
- For the presented data analysis
  - **3-6 GeV electrons** beams
  - **perpendicular** beams
  - hit-driven RO
  - KIT and UK telescopes placed as in figure
  - **HV scan for the UK telescope** (2, 5, 10, 15, 20, 30, 40, 50 V)
- Data reconstruction
  - **Corryvreckan**
  - use **L1** (ref), **L2** and **L4** as telescope planes for iterative **alignment** and **tracks reconstruction**
  - associate **L3** as **DUT** plane
    - selected tracks with χ^2/ndof<5
    - cluster associated if within 0.6mm from track interception

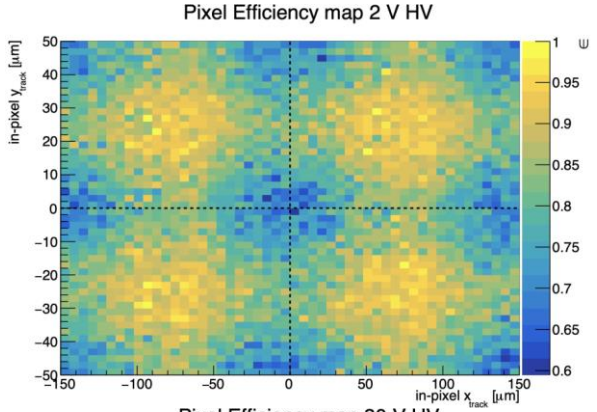
ATLASPIX3: DESY testbeam results

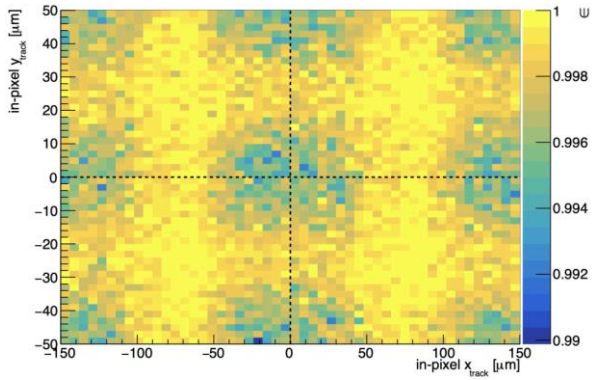
- **Uniform efficiency** is achieved after the junction laterally reaches the p-well strips insulating the pixels: **>99%**
- **Resolution ~11 μm**, as expected from normal incidence beams, dominated by single pixel clusters

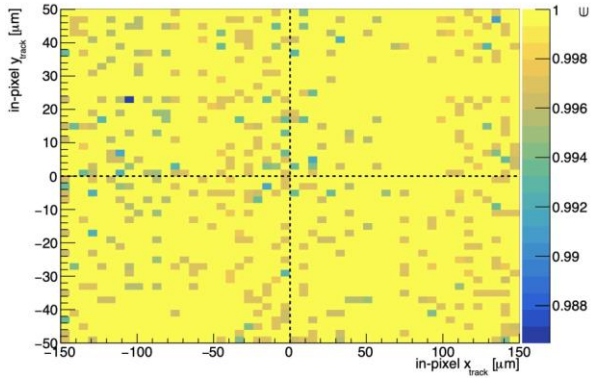






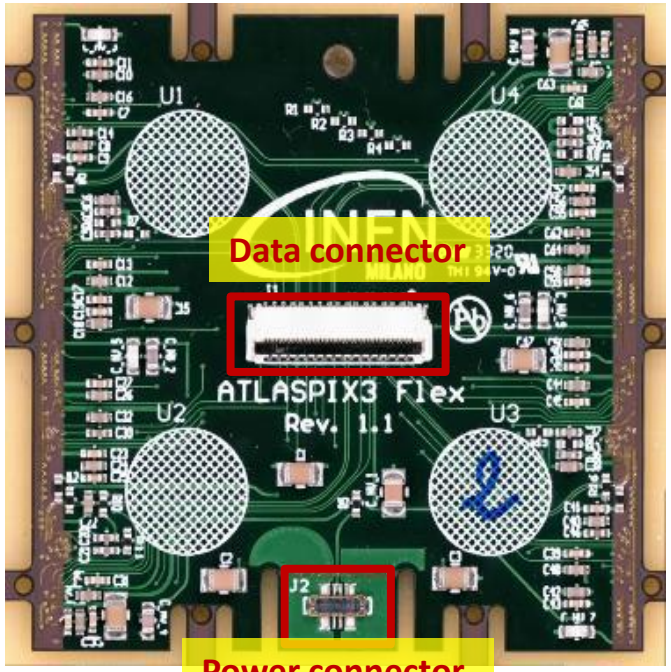


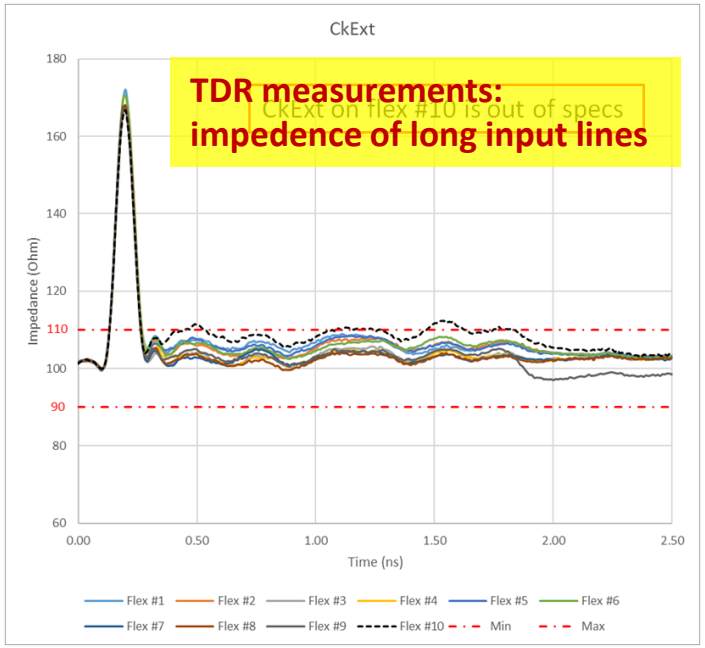


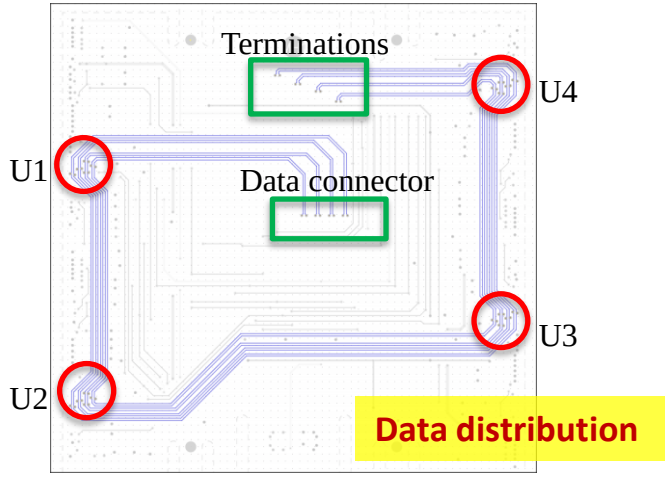


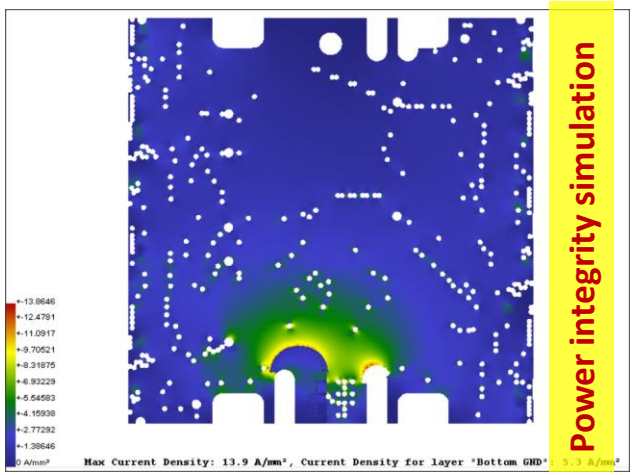
Module concept

- **Readout unit based on 4 chips**
  - shared services among 4 sensors by common power connections and configuration lines
  - benefits of in-chip regulators to reduce connections
  - avoids complications with stitching
  - design based on ATLAS quad-modules
- **Two configuration options**
  - command decoder (LVDS, default)
  - SPI (backup)
- **4-layer flex hybrid**
  - 2 power layers
  - 2 signal layers, impedance-matched lines

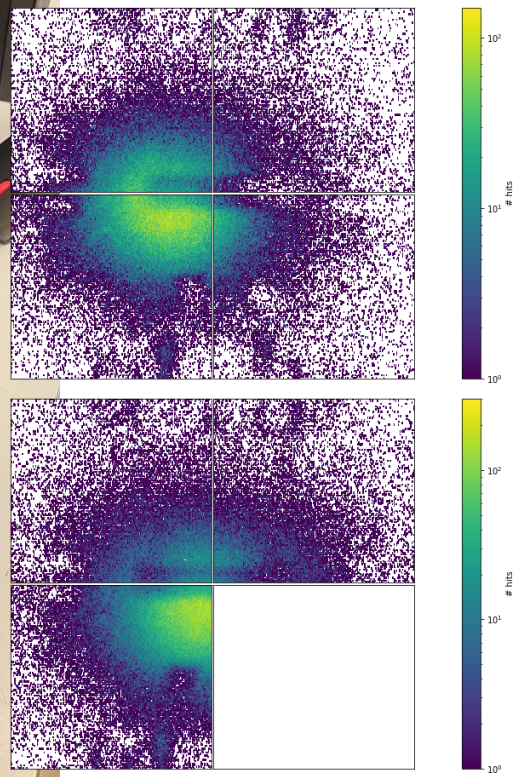




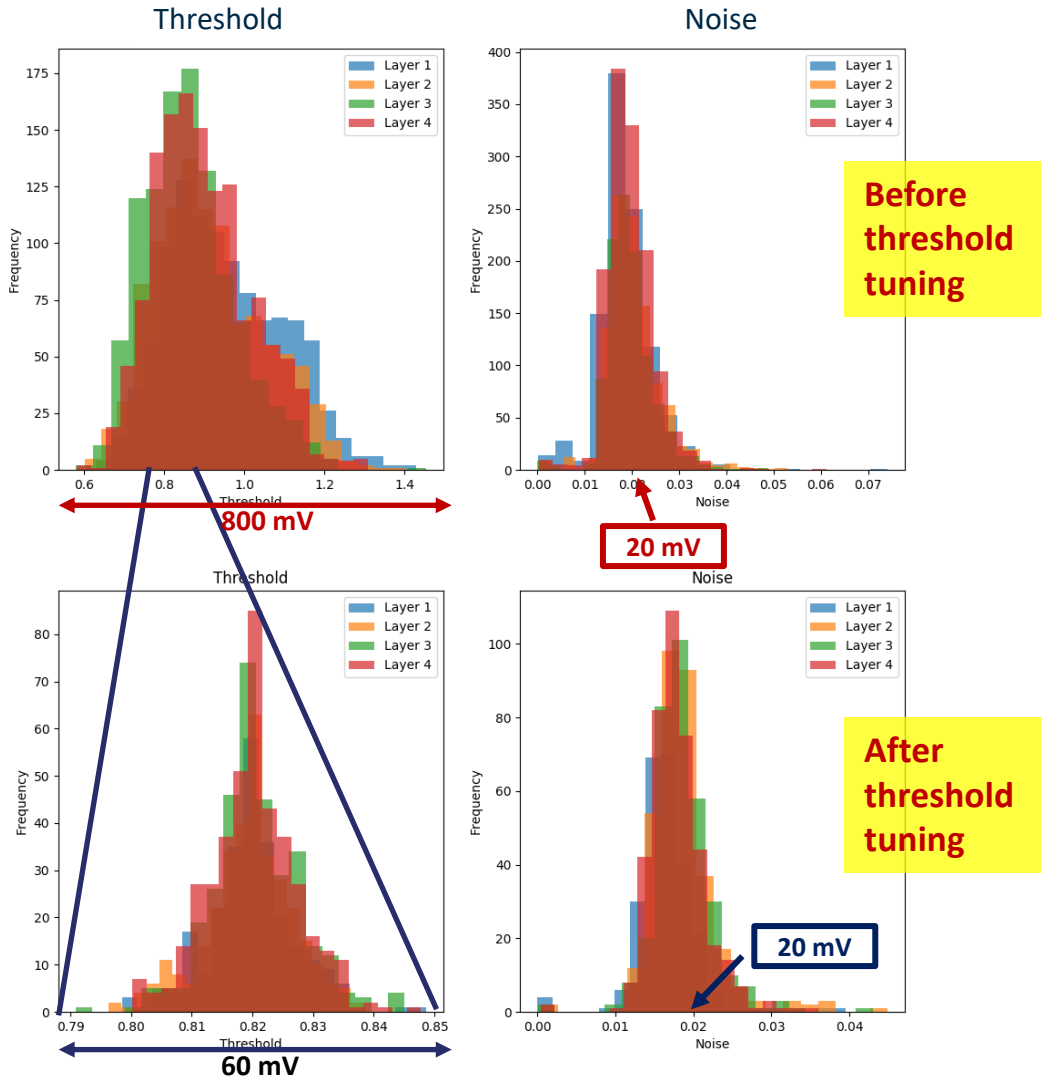




Quad-module performance



Two modules taking data with a 90Sr source
Visible are the shadows of the data connectors



Threshold tuning and noise measurement on modules
No change in performance compared to single chips

Shunt-LDO regulators

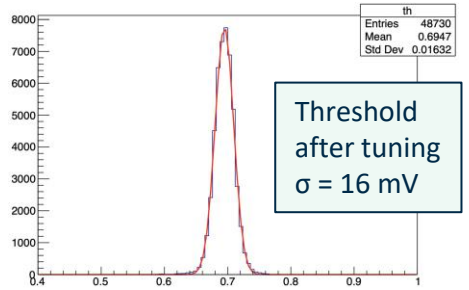
ATLASPIX3.1 can be powered serially using two shunt/low dropout regulators

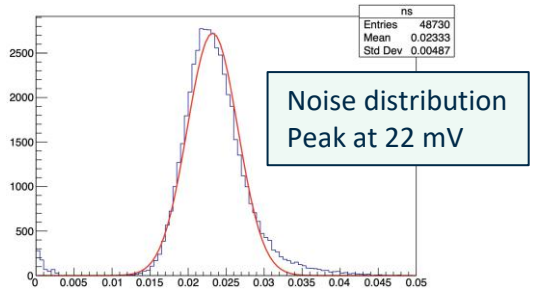
- VinA -> VDDA / VinD -> VDDD
- GND of the analog and digital circuits are shorted.
- Regulator outputs are connected to VDDD/A.

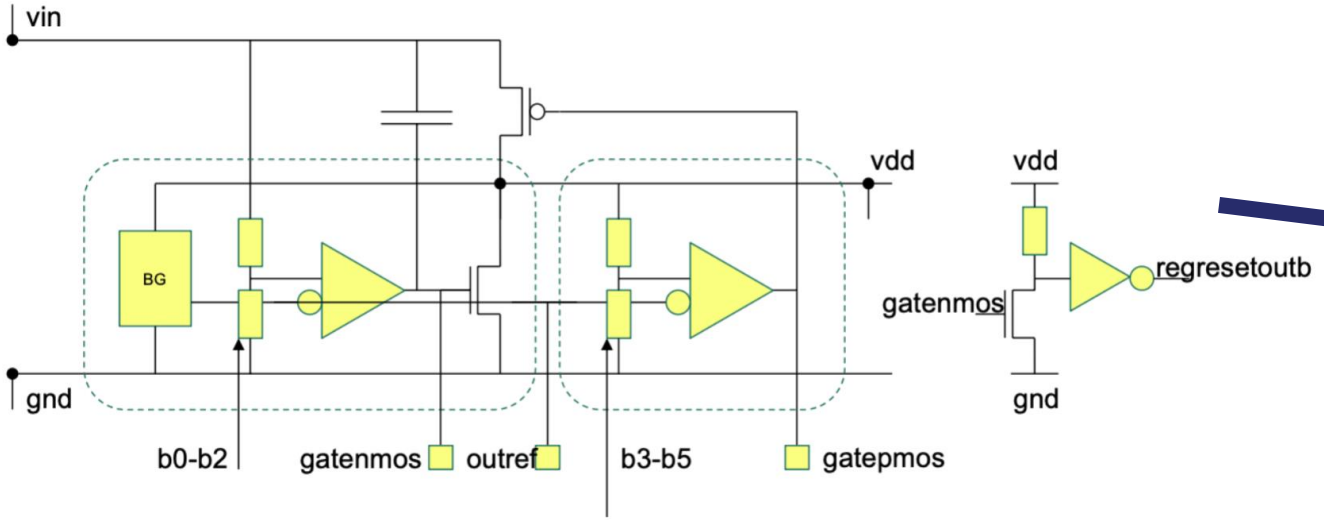
Each regulator 6-bit DAC to adjust the threshold and output voltage:

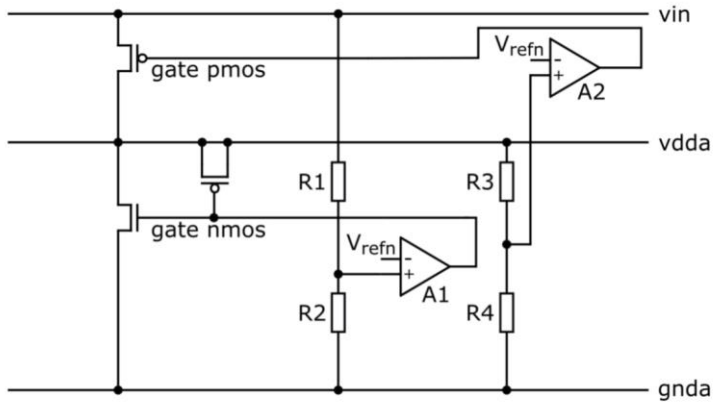
- b0-b2(3-bit) -> the shunt threshold (nominal value ~ 2.34V),
- b3-b5(3-bit) -> the VDDD/A output tuning (nominal value ~ 1.92V)

Analog performance independent from biasing scheme

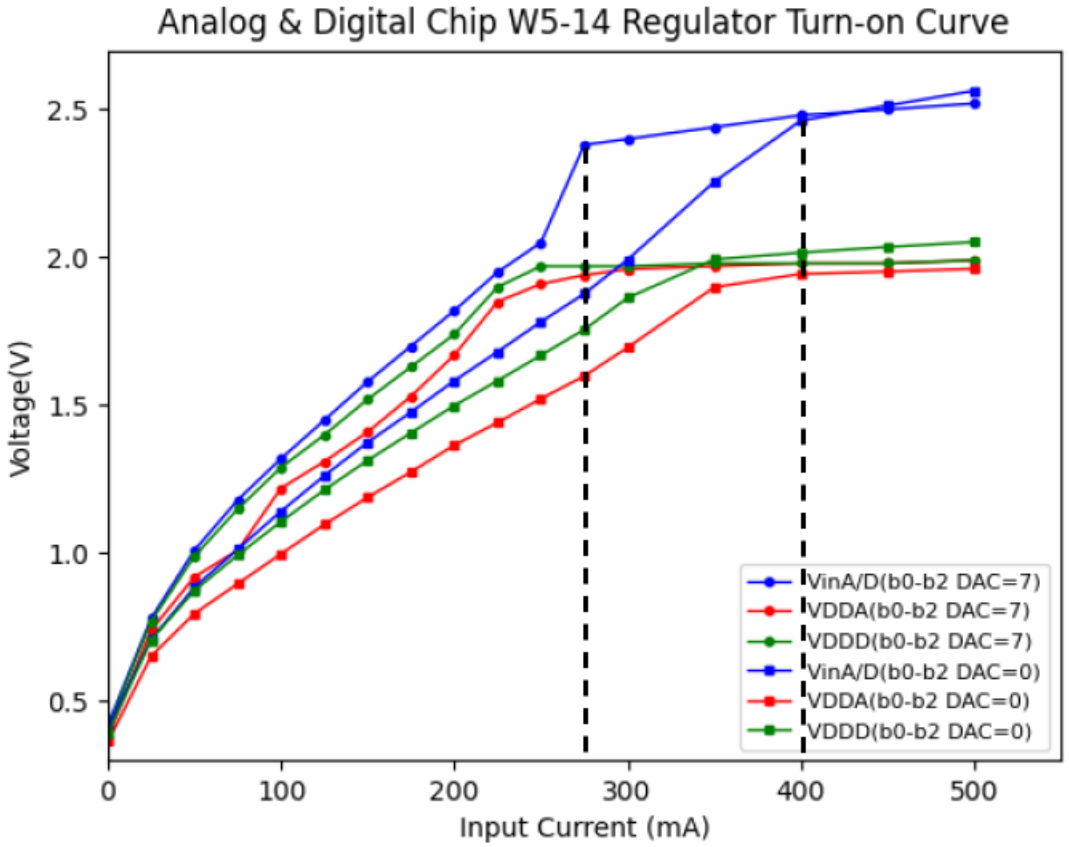




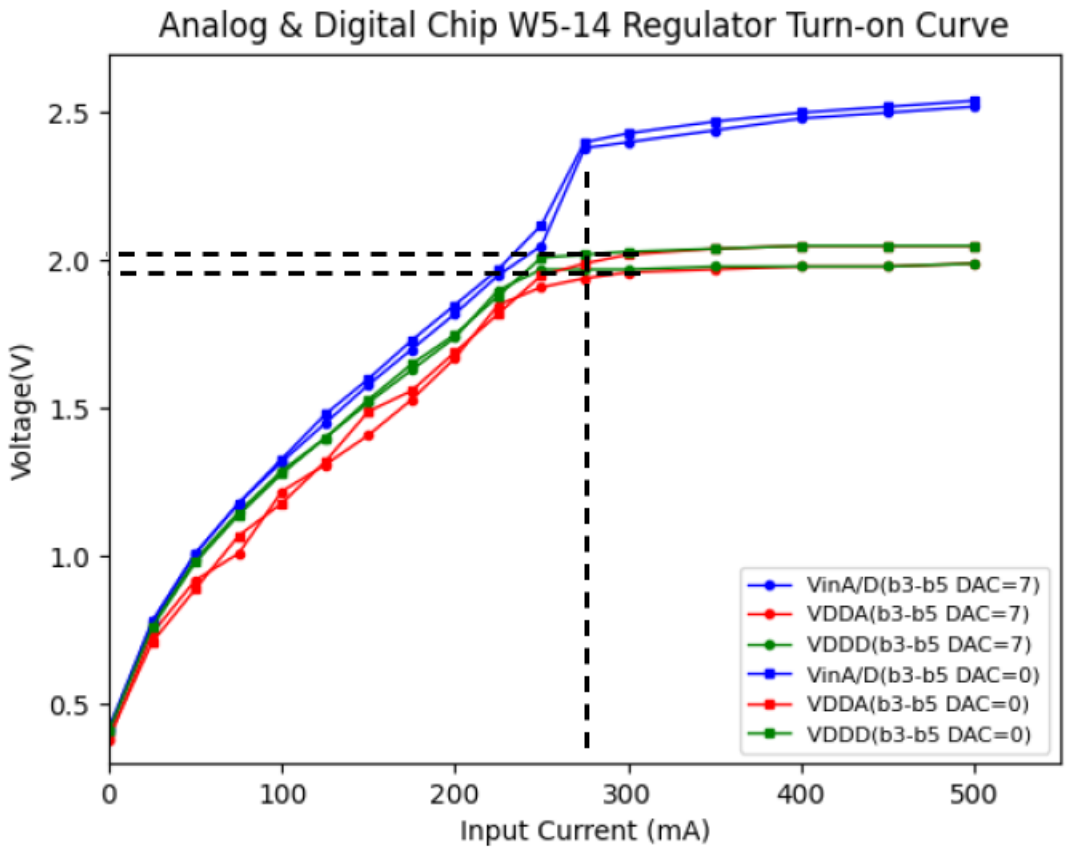




Shunt-LDO characterization



- **b0-b2 DAC pins** for threshold of shunt regulator
  - The VDDD/A voltages are regulated when input current ~**275mA** for (b0-b2) DAC=7, ~400mA for (b0-b2) DAC=0
  - b0-b2 are the pins to set the input current value when the voltage regulation starts.



- **b3-b5 DAC pins** for tuning of VDDD/A
  - The regulation turn-on value is after around 275 mA.
  - The regulated voltage value is ~**1.9V** for (b3-b5) DAC=7, ~2.1V for (b3-b5) DAC=0

Conclusions and outlook

- ATLASPIX3 is a reticle-size, fully-featured depleted CMOS pixel detector
  - It provided full efficiency in test beam
- It has been exploited to understand the complexity of building large area CMOS trackers at future accelerators
  - Multi-chip modules have been successfully operated, as first step toward a prototyping of full system integration
  - Shunt-LDOs for serial powering configuration have been tested
- Now proceeding toward the realization of quad-modules compatible with the serial powering biasing scheme
  - Planning to test a multi-module serial power chain before the end of the year
- Detailed resolution studies will benefit by additional test beam data
  - More telescopes are being assembled within the collaboration
- A WP1 project proposal has been submitted to continue the activity while developing new improved sensors