The ATLASPIX3 CMOS pixel sensor and module performance

Monday 17 June 2024 11:15 (15 minutes)

High voltage CMOS pixel sensors are proposed to be used in future particle physics experiment. The AT-LASPIX3 chip consists of 49000 pixels of dimension $50\mu m \times 150 \mu m$, realized in in TSI 180nm HVCMOS technology. It was the first full reticle size monolithic HVCMOS sensor suitable for construction of multi-chip modules and supporting serial powering through shunt-LDO regulators. The readout architecture supports both triggered and triggerless readout with zero-suppression.

With the ability to be operated in a multi-chip setting, a 4-layer telescope made of ATLASPix 3.1 was developed, using the GECCO readout system as for the single chip setup. To demonstrate the multi-chip capability and for its characterisation, a beam test was conducted at DESY using 3–6 GeV positron beams with the chips operated in triggerless readout mode with zero-suppression. The detector performance have also been tested with hadron beams and operating both with and without the built-in power regulators.

Multichip modules have been operated and behaviour in a serial powering configuration has been tested.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (scientific results or project proposal)

Presentation on scientific results

Primary authors: Prof. ANDREAZZA, Attilio (Università degli Studi e INFN Milano (IT)); USTUNER, Fuat (The University of Edinburgh (GB)); FOX, Harald (Lancaster University (GB)); PERIC, Ivan (KIT - Karlsruhe Institute of Technology (DE)); MENG, Lingxin (Lancaster University (GB)); ZANZOTTERA, Riccardo (Università degli Studi e INFN Milano (IT)); DONG, Ruoshi (University of Science and Technology of China); GAO, Yanyan (University of Edinburgh (GB))

Presenters: Prof. ANDREAZZA, Attilio (Università degli Studi e INFN Milano (IT)); USTUNER, Fuat (The University of Edinburgh (GB))

Session Classification: WG/WP1 - CMOS technologies