DRD3

DRD3 week
17-21 June 2024, CERN
https://indico.cern.ch/event/1402825

Project proposal for WP1:
A versatile pixel matrix in TPSCo 65 nm for future trackers

Jerome Baudot

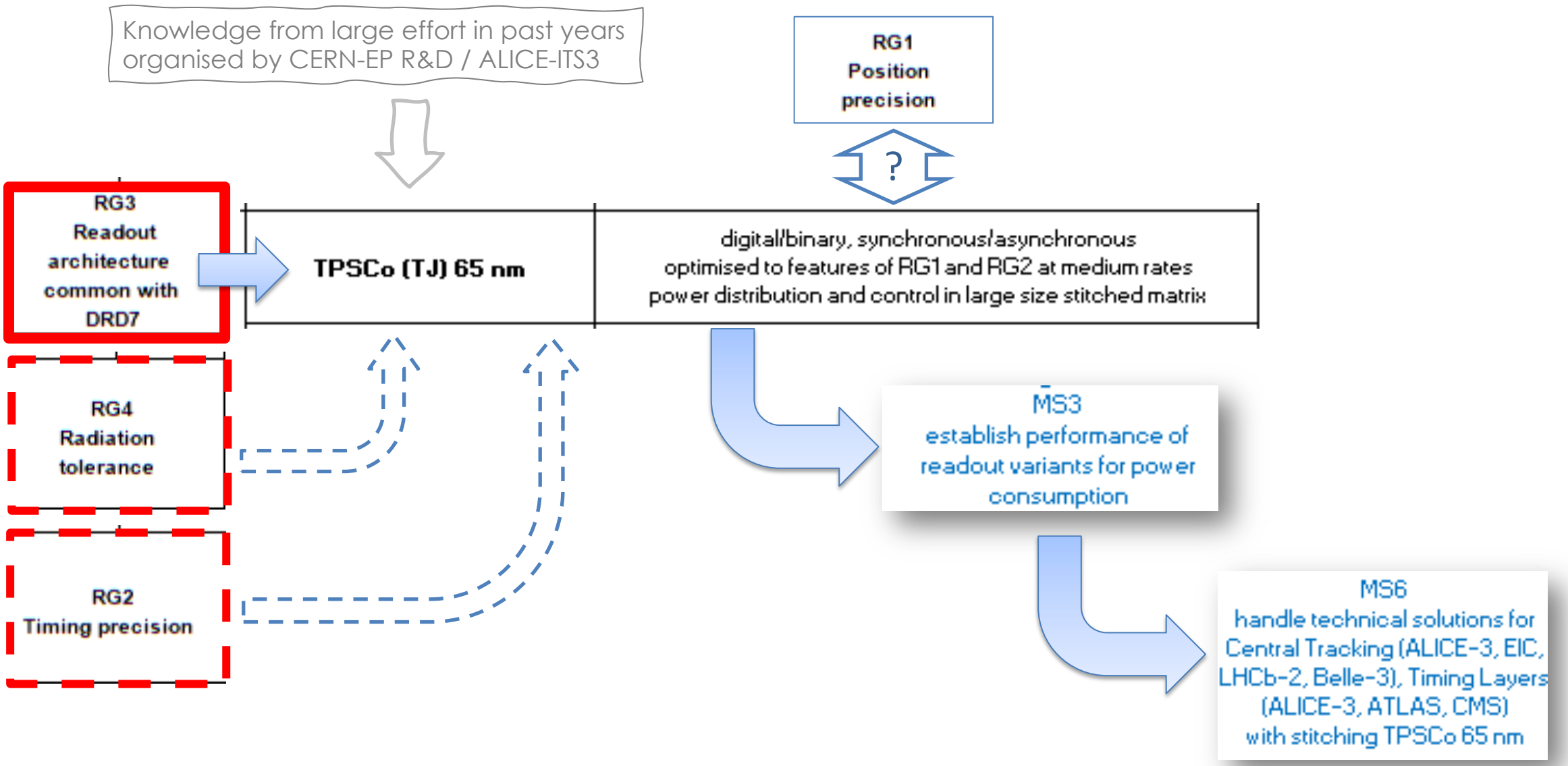
on behalf of a community
in construction

- Targeted DRD3 research goals
- Technical overview
- Timeline & Collaboration

Research goal target

DRD3 WG1 Monolithic CMOS		Assess technology performance for each RG – handle technical solution options for strategic programs of LS4 time scale				Toward 4D-tracking for future colliders
Research Goals	Timeline	2024	2025	2026	2027	≳ 28
	Technologies	Foundry submissions and Milestonses (MS)				
	TPSCo (TJ) 65 nm	design MPW1.1	submit MPW1.1 mid-2025 design MPW1.2	evaluate MPW1.1 submit MPW1.2 Q4-2026	evaluate MPW1.2	design/submit/evaluate MPW1.3-1.n (possibly including in common submissions ER designs for dedicated experiments)
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	design MPW1.1 submit MPW1.1 Q4-2024	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q1-2026		
RG1 Position precision	TPSCo (TJ) 65 nm	electrode size/shape/pitch, process variants 12" ER splits, thin epitaxial layer, stitching optimized for high channel density (low pitch)		MS1 establish position precision versus technology, channel configuration and readout mode MS2 establish time precision versus technology, channel configuration MS3 establish performance of readout variants for power consumption MS4 establish radiation tolerance provide guidlenies for choice of substrates select/merge MPW1.1 features add new technology features submit configurations for Vertex Detector, Central Tracking, Timing Layers, HGCAL	MS5 handle technical solutions for Vertex Detector (ALICE-3, LHCb-2, Belle-3, CMS/ATLAS) 1) high radiation tolerance/rate technlogies > 65 nm 2) high channel density, sitching TPSCo 65 nm MS6 handle technical solutions for Central Tracking (ALICE-3, EIC, LHCb-2, Belle-3), Timing Layers (ALICE-3, ATLAS, CMS) with stitching TPSCo 65 nm MS7 handle technical solutions for low power w/o and w/ precision timing, at medium and high rates	merge RTs and various technology achievements in selected technologies, extend all to stitching implement 3D integration consider finer nodes and new materials
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	electrode size/shape/pitch, wafer type/thickness, process variants 8" ER or MLM splits				
RG2 Timing precision	TPSCo (TJ) 65 nm	similar to RG1 optimized for fast signal collection speed and high S/N				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	similar to RG1 optimized for fast signal collection speed and high S/N including gain layer option				
RG3 Readout architecture common with DRD7	TPSCo (TJ) 65 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium rates power distribution and control in large size stitched matrix				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium and high rates				
RG4 Radiation tolerance	TPSCo (TJ) 65 nm	process features in splits				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	variants of substrates (Cz, epitaxial), resistivity, p-type and n-type				

Research goal target



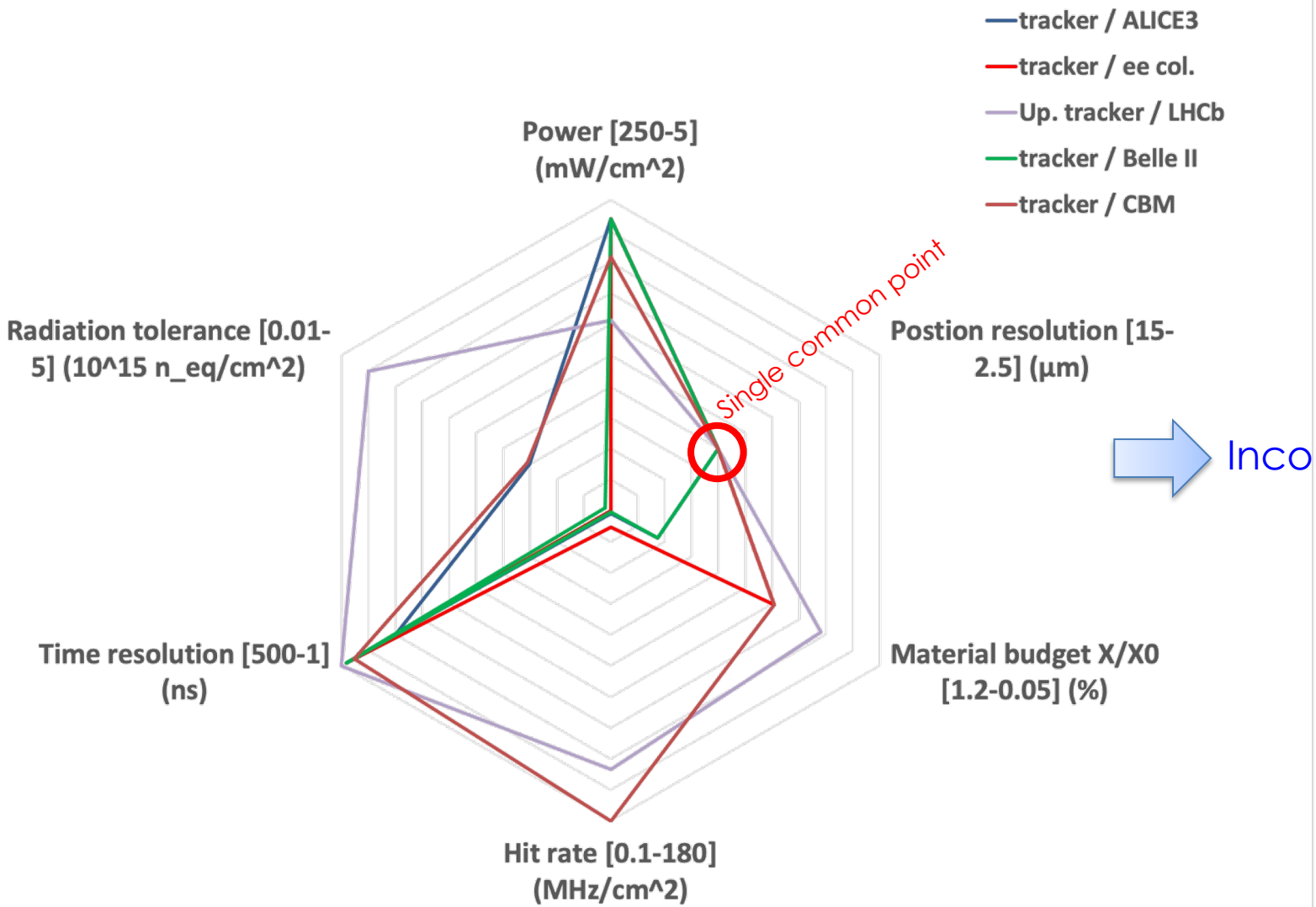
Specifications: numbers!

Source: my own mix of LOI, recent talks and private communication

	ALICE3 OT	Belle II trk	CBM trk	LHCb UT	FCCee trk
Position resolution	~10 µm	<15 µm	~10 µm	<10 µm	<10 µm
Pixel pitch (µm)	50	50	~30	50	50
Hit rate (MHz/cm^2)	0.05 to 2	<1	60/180	160	<10
Data rate (Gb/s)			8	20	
Time figure (ns)	100	~1	25	~1 (<25)	20 to 1000
Triggering	no	yes	no	no	?
Power	~20	<50	~50	<100	~20?
TID (kGy)	50	10?	~10	2400	10?
NIEL	10^{14}	10^{11}?	few 10^{14}	$3x10^{15}$	10^{11}?

Specifications: the graph

Pay attention to axis scales,
not very robust!



Incompatible requirements?

Read-out architecture

Pay attention to axis scales,
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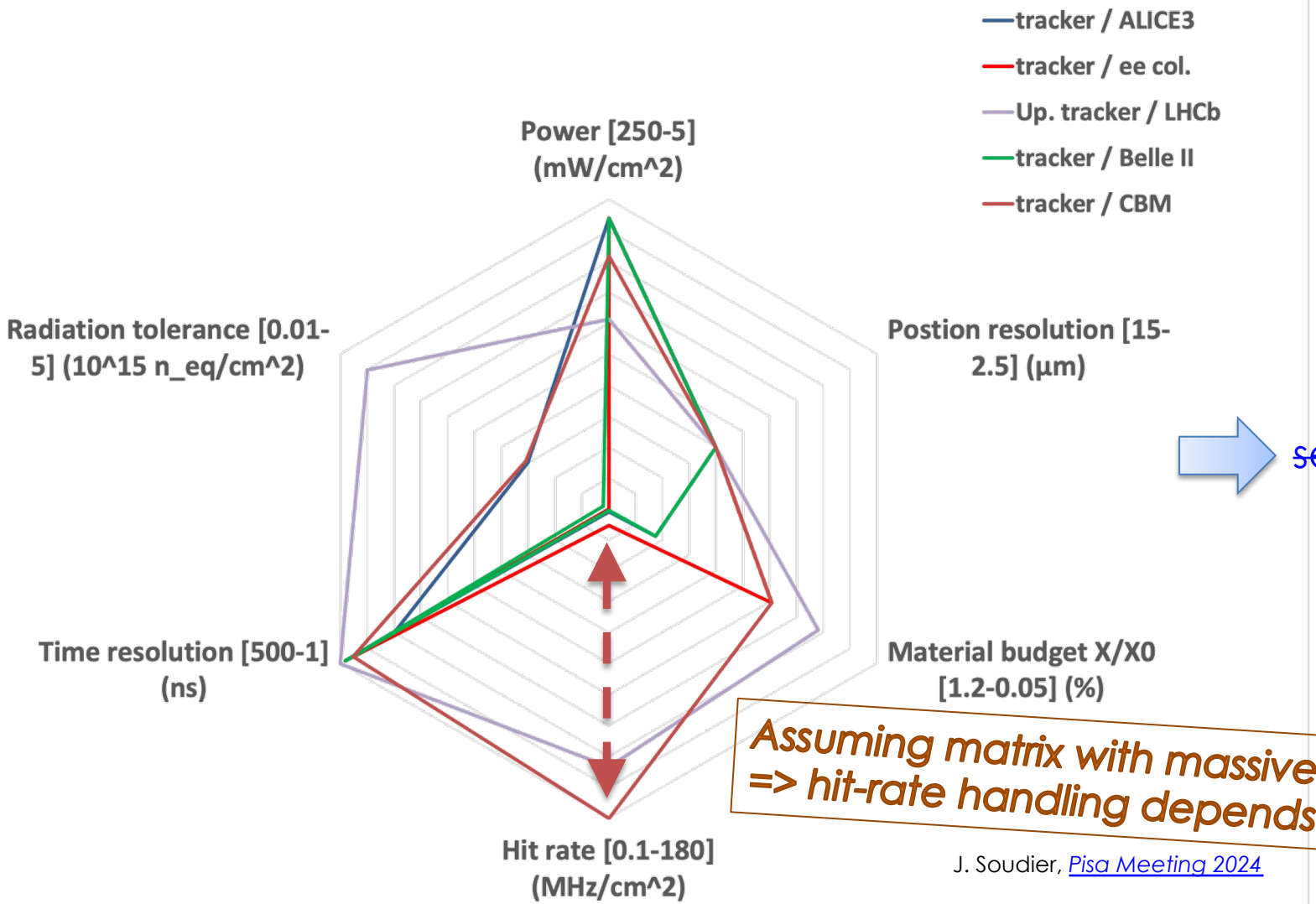


~~sensor~~ => *matrix*

Assuming matrix with massive parallel read-out
=> hit-rate handling depends on periphery

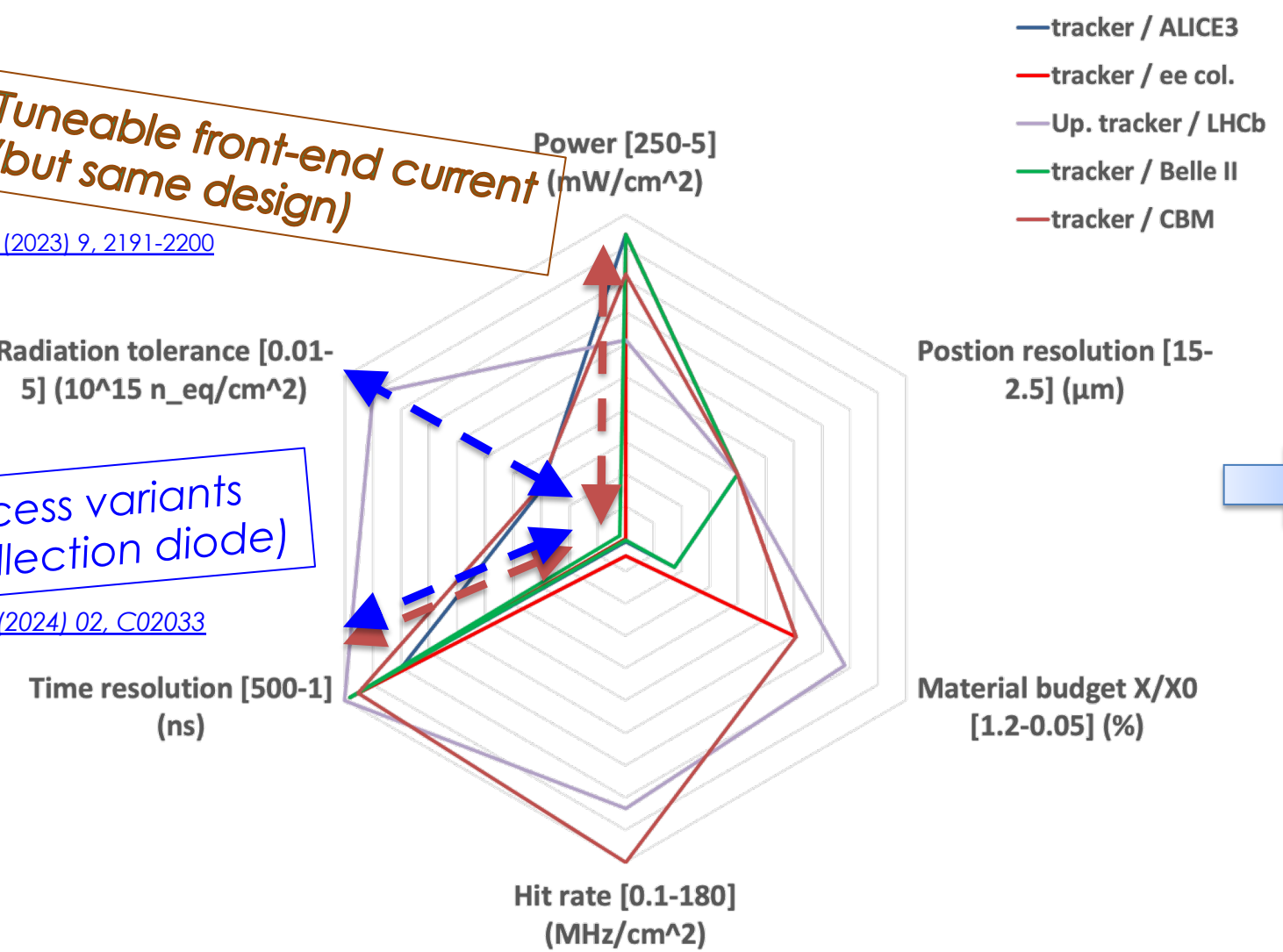
J. Soudier, *Pisa Meeting 2024*

Process & Pixel front-end

Pay attention to axis scales,
not very robust!

Tuneable front-end current (but same design)

F.Piro *et al.*
IEEE Trans.Nucl.Sci. 70 (2023) 9, 2191-2200



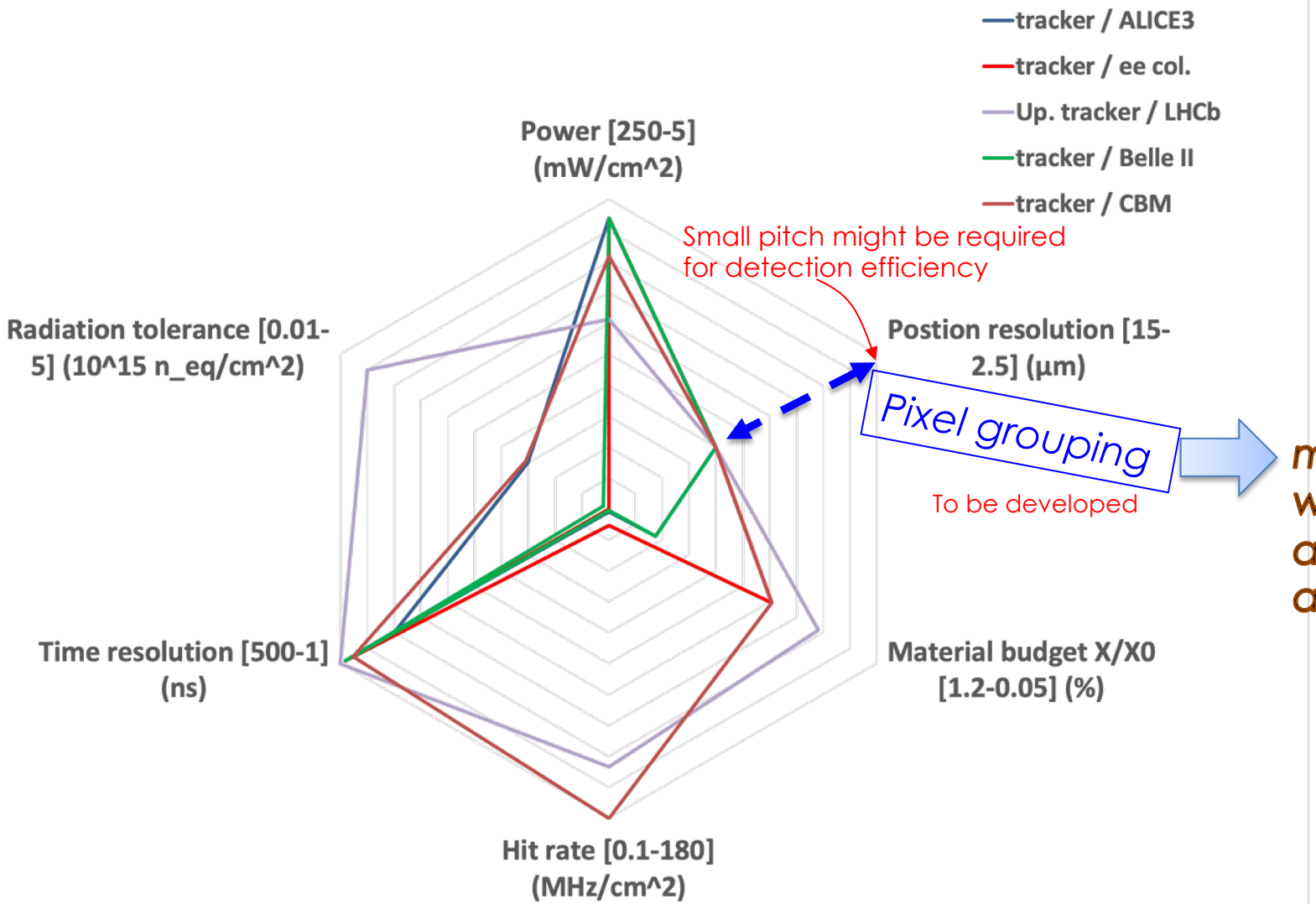
Process variants (collection diode)

C.Lemoine *JINST 19 (2024) 02, C02033*

matrix with tuneable front-end and process variants

Detection efficiency / position resolution

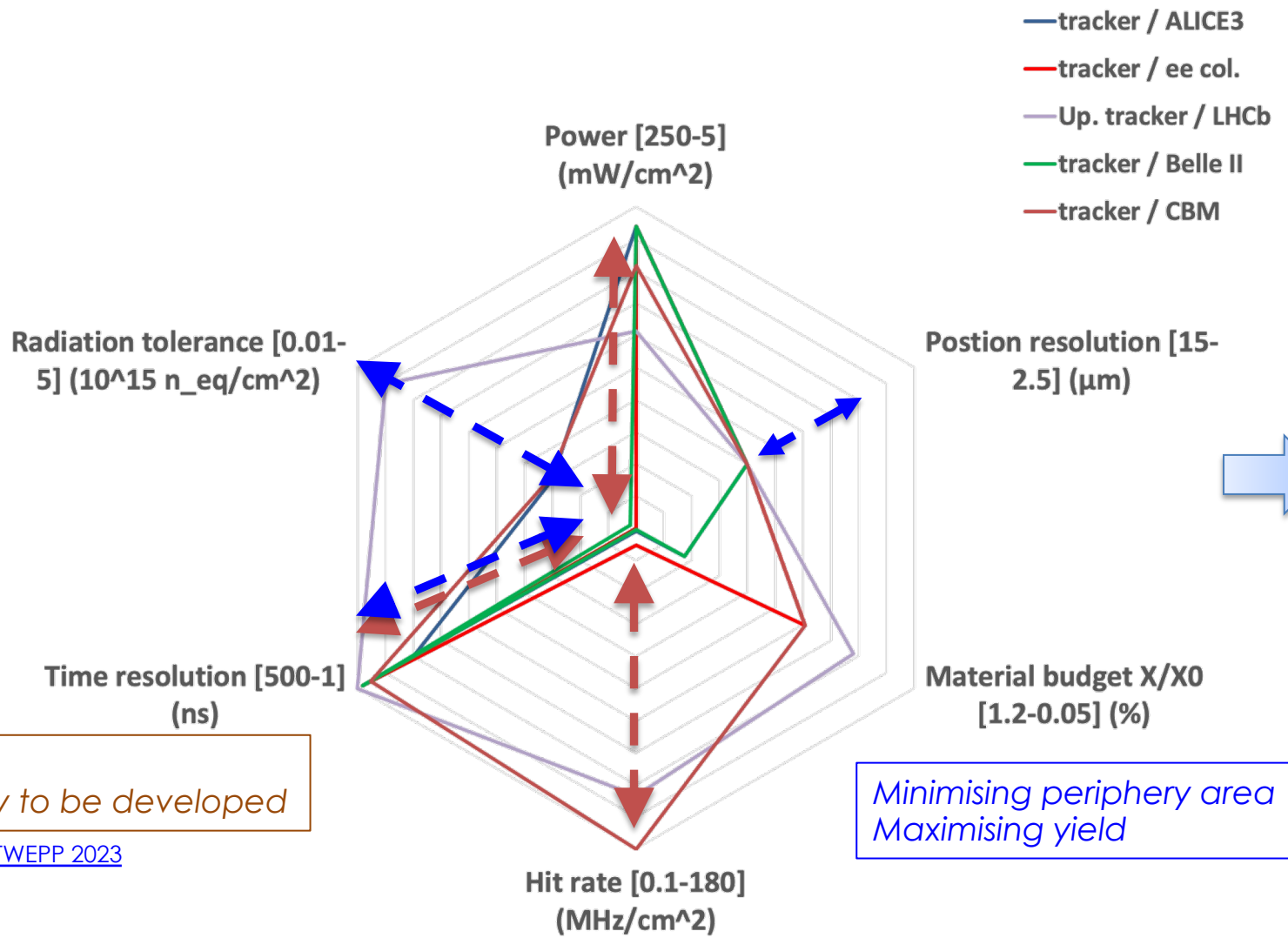
Pay attention to axis scales,
not very robust!



matrix
with tuneable front-end
and process variants
and switchable pixel group

Proposal

Pay attention to axis scales,
not very robust!



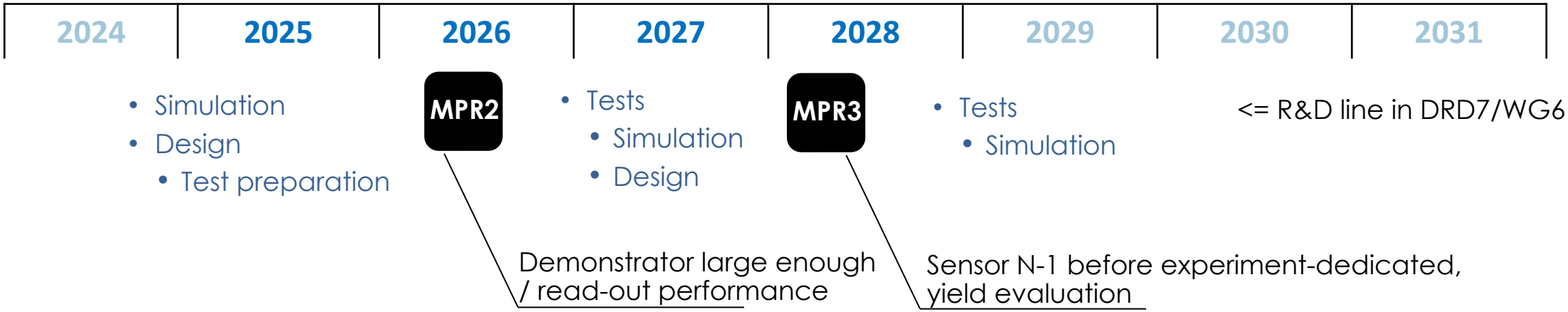
matrix
with tuneable front-end
and process variants
and switchable pixel group

For O(100) ps
=> TDC strategy to be developed

C. Ferrero, TWEPP 2023

Minimising periphery area
Maximising yield

Timeline & Collaboration



- Interested groups so far (mostly under discussion)
  - France: CPPM, IPHC, IRFU, LPNHE, …
  - Germany: GSI, …
  - Italy: Bergamo/Pavia, …
  - Japan: under discussion
  - Spain: IFIC, IGFAE, …
  - USA: under discussion
  - …

- Expected strong synergies
  - DRD3-WP1 projects in same techno
    - Position resolution
    - Radiation tolerance
    - Time resolution
  - DRD7-WG6 for technology access

Conclusion

- **Goal = new generation of tracker detectors**
- **Technology = TPSCo 65 nm**
- **Main deliverable = versatile pixel matrix**
  - Fixed q-collection pitch
  - Process fabrication option
  - Tuneable front-end
  - Programmable periphery

=> Consortium under construction