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Large electrode sensors with intrinsic amplification for ultimate timing performance

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Large size electrode monolithic sensor designs have been explored successfully in the past, mainly for tracking applications. Notable examples of this concept are LF-CPIX, followed by the large size (1 cm2) LF-MONOPIX1, LF-MONOPIX2 and TJ-MONOPIX demonstrators, intended for ATLAS ITK outer layers. LF-CPIX, LF-MONOPIX1 and LF-MONOPIX2 were designed in LF-15A technology, and TJ-MONOPIX is in TJ-180 technology.
One important feature of the large electrode designs is that the geometry of the charge collecting region is very close to a parallel plate capacitor. This is very favorable to obtain good timing performance for MIPs, since the dependence between the signal shape and the impact point position on the sensor is minimal.
This is why we have started investigating the performance of large-electrode sensor designs in LF-15A technology. The most recent designs in this research line are MiniCactus v1 and MiniCactus v2. These sensors are designed in LF15A process and built upon the tracking-oriented demonstrators LF-CPIX and LF-MONOPIX. The MiniCactus chips share many structures that were originally designed and optimized for LF-CPIX and MONOPIX (guard rings, slow control DACs, configuration register, global front-end architecture).

The long-term goal of MiniCactus developments is to provide a timing sensor with performances compatible with LHC timing detector upgrades, to be considered post LHC phase 2. Typically, an evolution of MiniCactus could be a candidate for the replacement of the ATLAS HGTD inner disks.

The foundry process LF15A used has been shown in the past to be intrinsically radiation hard. In addition, since MiniCactus uses a standard foundry process, ASICs based on this principle should be cheap to produce in high volume, as needed for large detectors.

MiniCactus v1 has been developed in 2020-2021. It features several pixel sizes, the biggest being 1 mm by 1 mm, the smallest 50 µm by 50 µm, and several pixels architectures. The best time resolution (65 ps) has been obtained in test beam with a 0.5 mm by 1 mm pixel, with integrated AC coupling capacitor, with a 200 µm thick sensor biased at 450 V. The read out electronics is in the form of an end of column block, to avoid running large metal rails over pixel surfaces to power in pixel electronics. This kind of design has proven in the past (Cactus design, done in 2017-2018) to bring large parasitic capacitance.

MiniCactus v2 builds upon the experience gained with MiniCactus v1. This chip implements mostly the pixel identified as having the best performance with MiniCactus v1. The original charge amplifier front-end has been reoptimized, the discriminator has been improved and digital/analog separation has been reinforced, to minimize couplings observed on MiniCactus v1. In addition, Minicactus v2 features several new front-end architectures, inspired from the Altiroc analog front-ends. These new front-end should according to simulation give performance somewhat better than the original charge amplifier, and the output signal duration is below 25 ns, making them tailored for integration in an LHC experiment.

The time resolution depends not only on the jitter but also the landau fluctuations of the sensor. These are of tens of ps, the same order of magnitude as the jitter. Therefore, in order to obtain smaller time resolutions, it is not only mandatory to improve the electronics but also the sensor. Landau fluctuations can be reduced by thinning the sensor, but less charge is collected and the signal to noise ratio is degraded. To overcome this limitation, we propose to explore the implementation of a buried PN junction, acting as a charge multiplication layer below the active electronics of a CMOS monolithic sensor. This will improve the signal over noise ratio, allowing to simultaneously improve time resolution, reduce the front-end power consumption, and exploit smaller pixel sizes. It should be noted that implementing a gain layer in the framework of a commercial CMOS process opens up the long term possibility of an intrinsically amplified, fully integrated sensor, with analog front-end and digital blocks on the same substrate, making it a potentially cheap solution suited for large detectors.
TCAD simulations have been completed and show that a gain of the order of 10 is achievable using the existing available layers and available implant energies for the LF-150 technology. Test structures have been submitted in May 2024 and will be characterized in the coming months.
In addition to the LF-150 technology, we intend to study the same concept with the more advanced technologies TPSCO 65

Type of presentation (in-person/online)

in-person presentation

Type of presentation (scientific results or project proposal)

project proposal for future work

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