Radiation hard read-out architectures

C. Solans

1st DRD3 week on Solid State Detectors R&D

18 June 2024

DRD3

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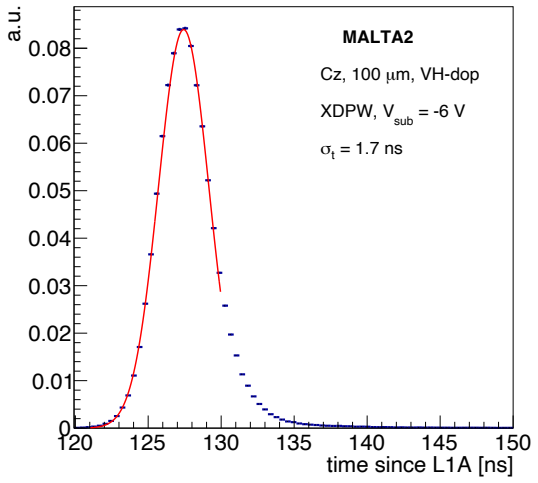
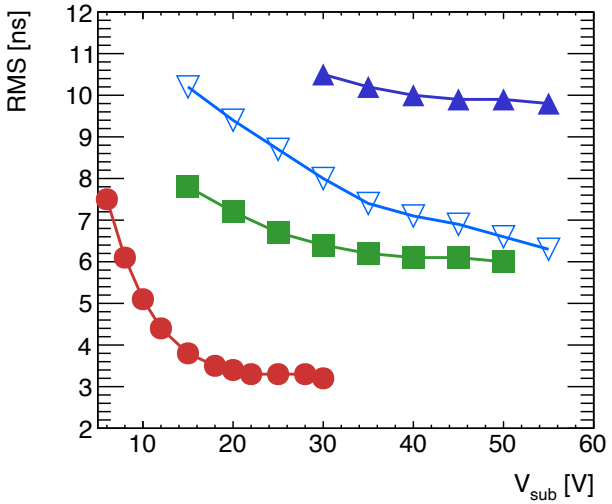
Introduction

- Propose R&D on rad hard read-out architectures close to MALTA R&D (ongoing ~2018)
- In-line with research goals of Monolithic silicon technologies (WG1) and characterization techniques and facilities (WG5) inside DRD3 WP1
- Benchmark time resolution ~1 ns driven by pixel design and doping concentration
  - Clear impact of doping concentration to improve radiation hardness
- Can we do better with less power?

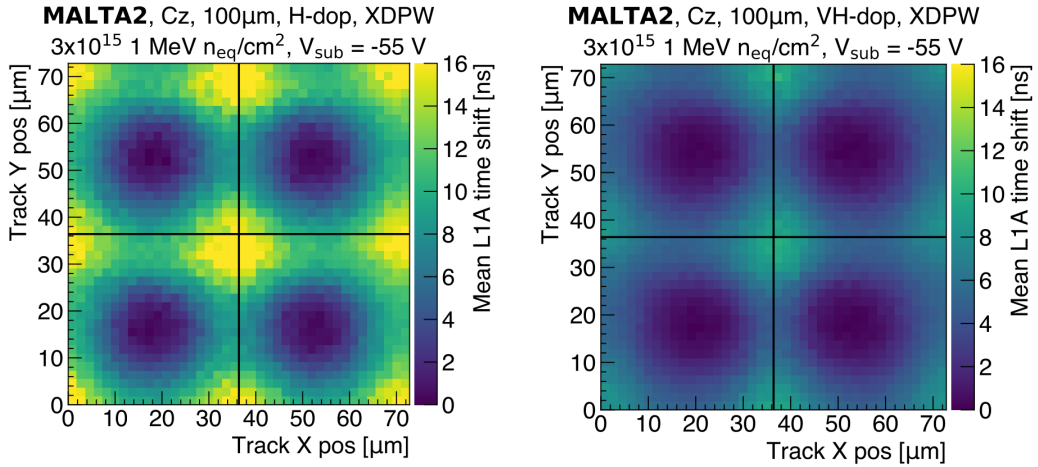
More details: "Radiation hardness and timing performance of MALTA monolithic Pixel sensors in Tower 180 nm" (WG1 L. Fasselt) Mon 12:15



Time of arrival of leading hit in a cluster w.r.t. scintillator reference



Timing deteriorates with irradiation due to charge trapping slow collection from pixel corners



Timing improves with doping concentration of the n-layer

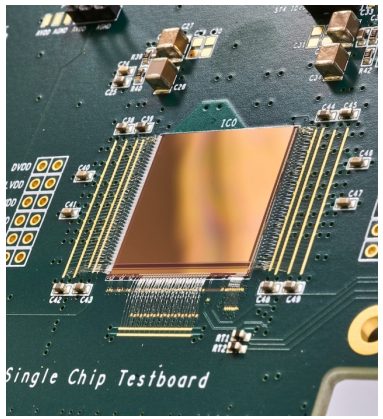
Brief history of MALTA R&D

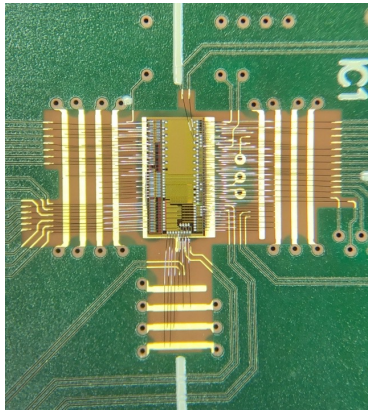
DRD3

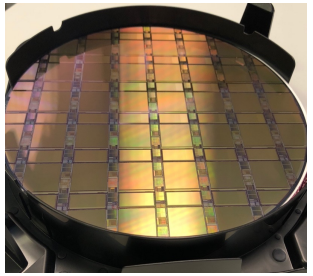
STREAM

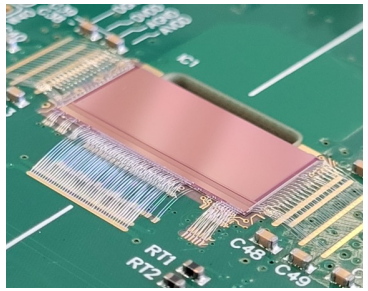
AIDA Innova WP5 and CERN EP R&D WP 1.2

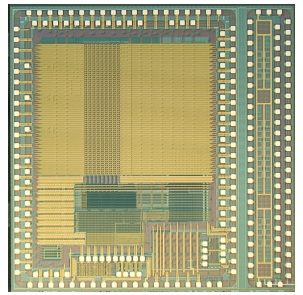
DRD3











Matrix segmentation?

Pixels with internal gain?

Detector compatible?

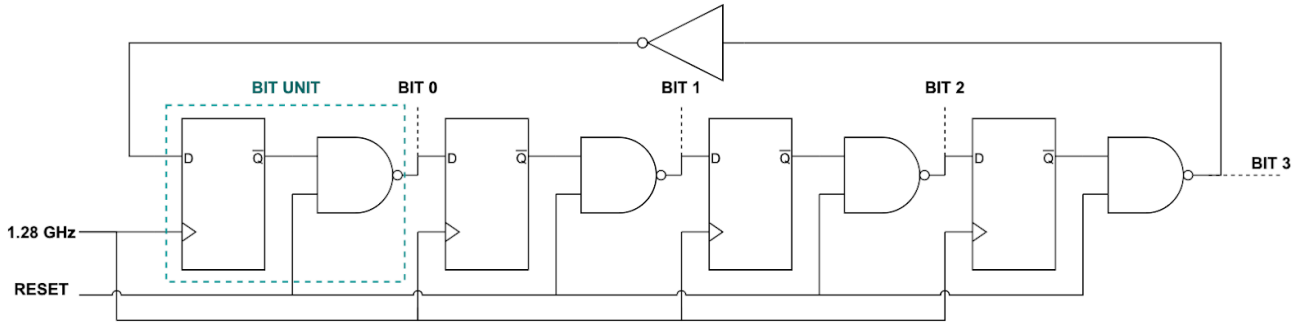
MALTA1 & MLVL	Mini-MALTA	MALTA C	MALTA 2	Mini-MALTA 3	MALTA 3
Jan 2018	**Jan 2019**	**Aug 2019**	**Jan 2021**	**Dec 2023**	
Asynchronous readout 80 mW/cm2 total power	Process and mask modification	New slow control Czochralski substrates	New front-end Higher n-layer doping	New periphery Time tagging	Larger than 2x2 cm2 Radiation hard better than 3e15 n/cm2 Time tagging below 1 ns
First full-size demonstrator	Full efficiency after 1e15 n/cm^2	Larger cluster size	Radiation hard 3e15 n/cm^2 Timing better 2 ns	on chip synchronization	

More details: "CMOS Active SenSor with Internal Amplification" (WG1 T. Suligoj)

Mini-MALTA3 pixel detector prototype

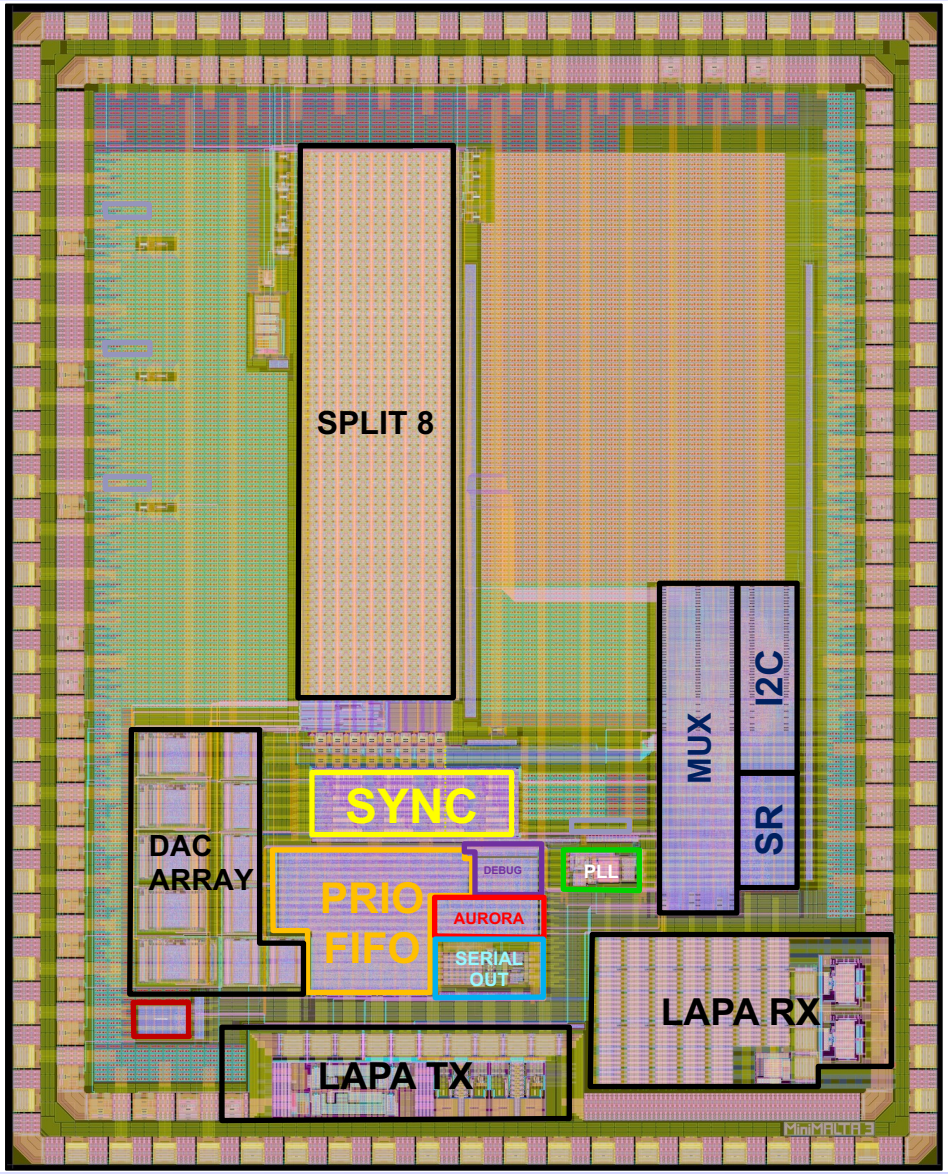
DRD3

- Details
  - 5x4 mm^2 demonstrator with 48x64 pixels of size 36.4 um^2
  - Low noise font-end from Mini-MALTA (split 8)
  - Time tagging 0.78 ns time resolution with no clock over matrix
  - 1.28 GHz clock derived from 80 MHz input via PLL
  - Slow control in I2C and shift register
  - 5 Gbps-capable pseudo-LVDS driver for input and output
  - Output data scrambled using Aurora
- Demonstration goals
  - Tag timing capability below 1 ns and up to 1 LHC orbit (89 us)
  - Serialized slow control input for reset and pulsing

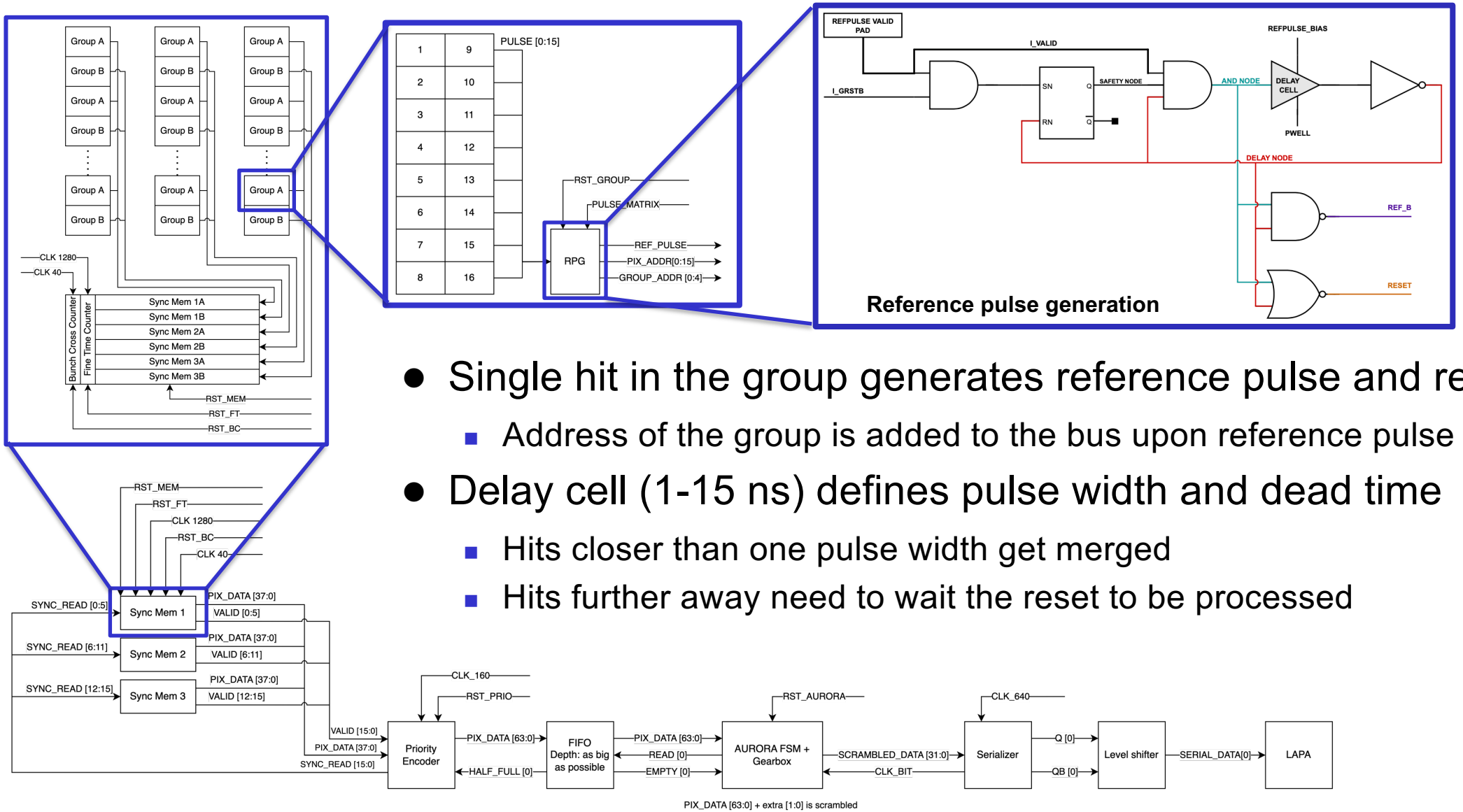


Twisted ring counter used in the synchronization memory

D. Drobrijevic et al. JINST 18 (2023) C03013



Mini-MALTA3 block diagram

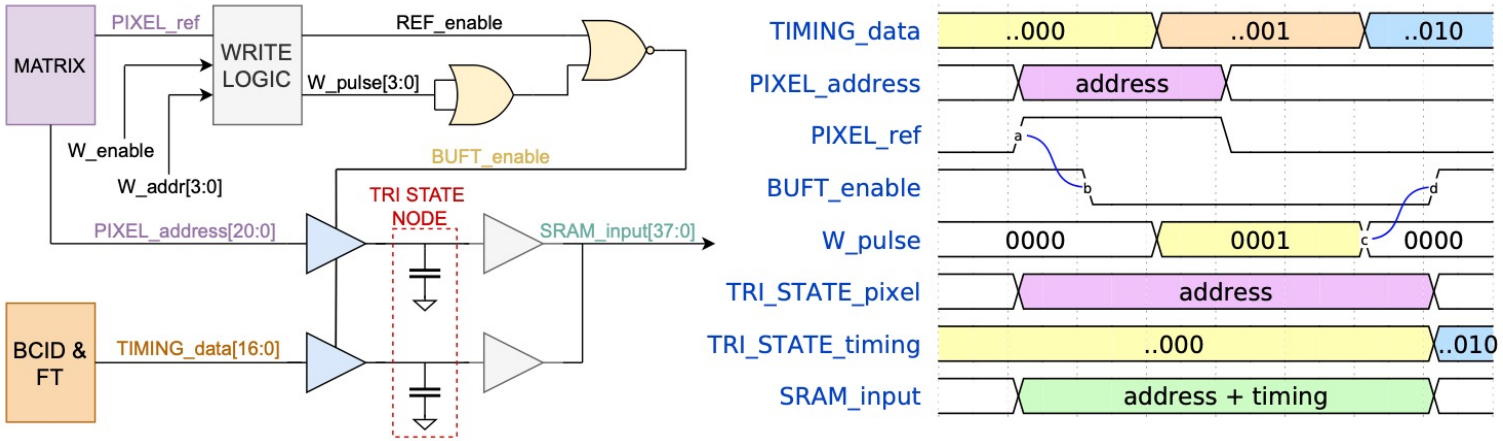


- Single hit in the group generates reference pulse and reset signal
  - Address of the group is added to the bus upon reference pulse generation
- Delay cell (1-15 ns) defines pulse width and dead time
  - Hits closer than one pulse width get merged
  - Hits further away need to wait the reset to be processed

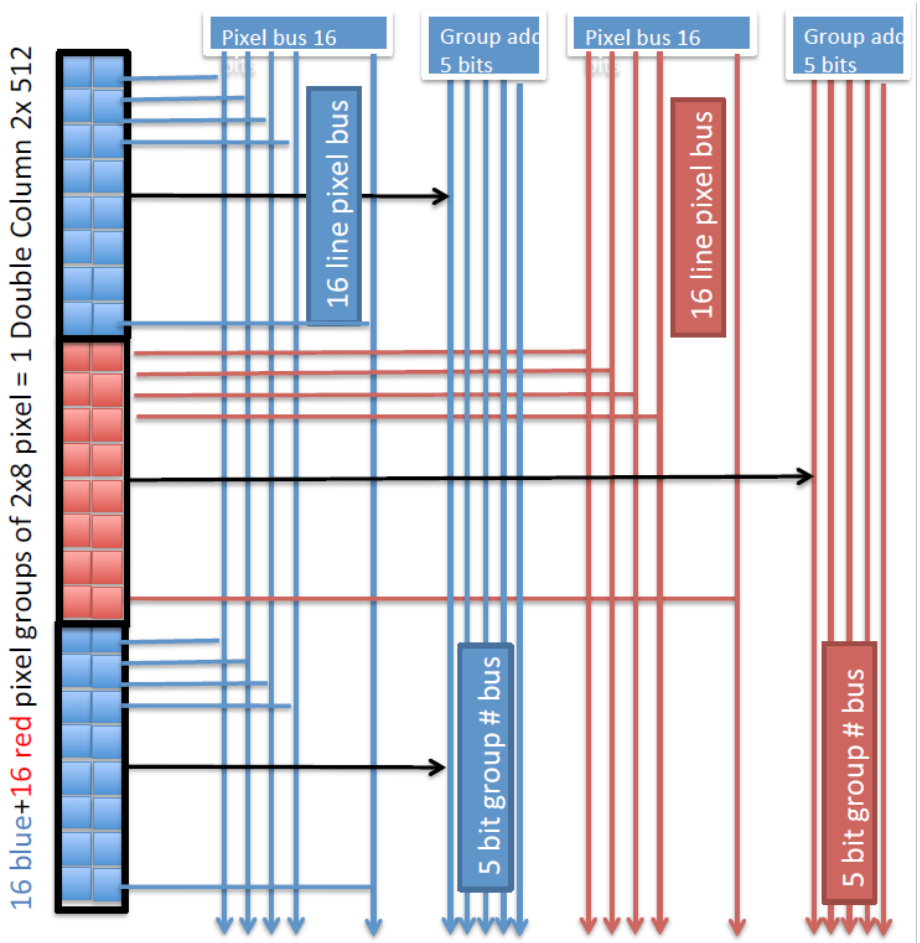
Asynchronous readout architecture in MALTA

DRD3

- Asynchronous reference pulse generation drives readout
  - Inherently radiation hard, no memory needs to be stored, SEUs recovered by next cycle
- 8 rows x 2 cols pixel grouping spaces hits from neighbors
  - Reference pulse logic implemented in each block
  - 2 address buses interleave data from groups for extra spacing
- Time of arrival based on group position can be corrected
- Tri-state synchronization memory stores the first value of the timing upon arrival of reference bit
  - Standard SEU mitigation techniques not considered yet (TMR)



Tri-state input logic of the synchronization memory of MiniMALTA3

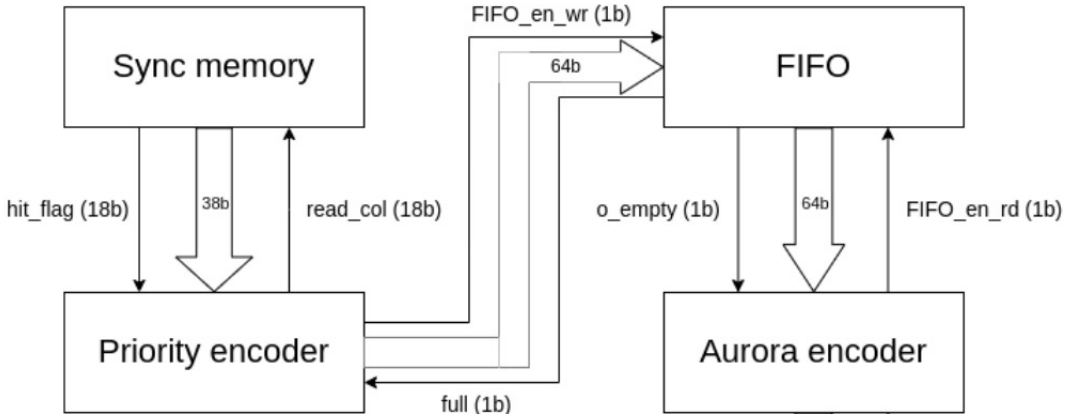


I Berdalovic et al. JINST 13 (2018) C01023

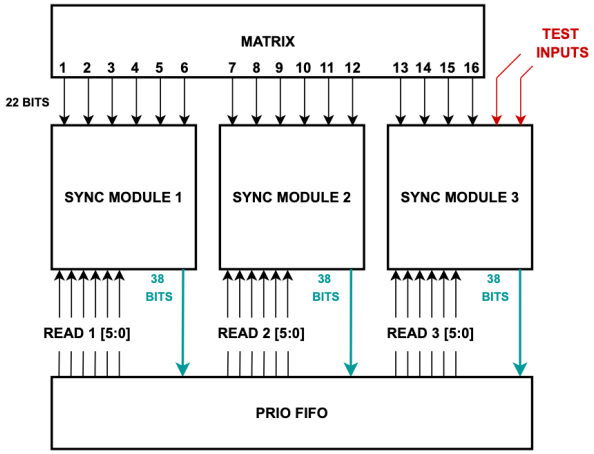
Priority encoding and matrix readout

DRD3

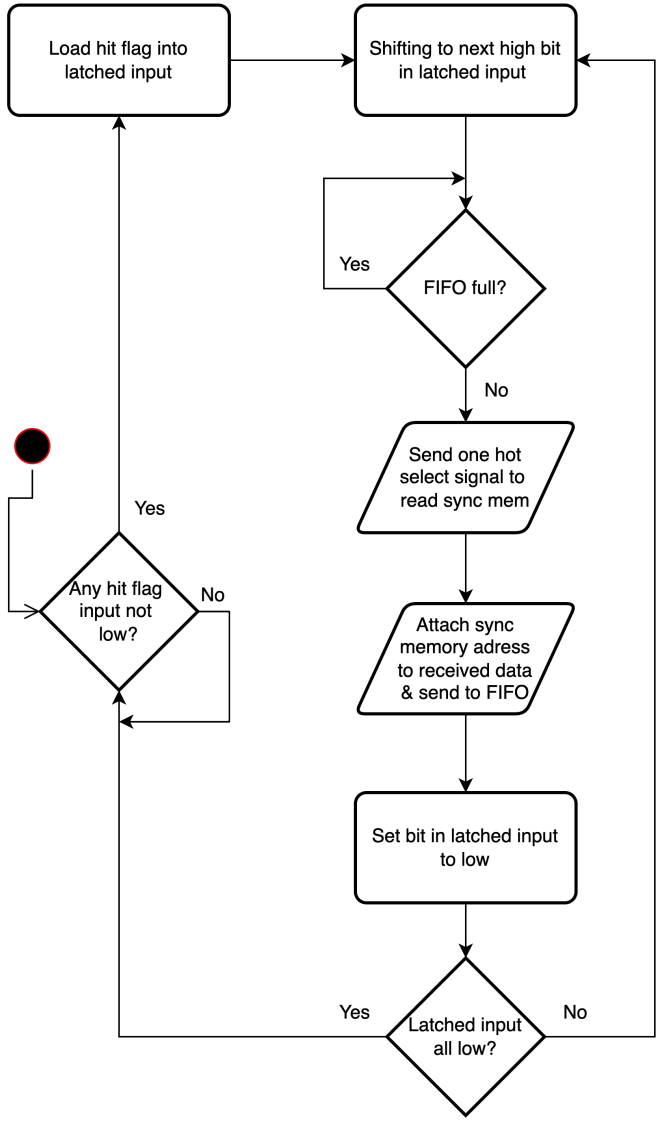
- Priority encoder places hits from three synchronization memories into one FIFO at 160 MHz (optimized for 320 MHz)
  - Classic left to right memory selection
  - Readout one hit from each memory before checking again
- Data on FIFO is Aurora scrambled and sent to serializer running at 1.28 GHz
  - Compatible with standard serial lines of rad-hard transceivers (lpGBT)
- Several links from same detector for high hit rates desirable



Data path from synchronization memory to Aurora encoder



Routing of sync memories to priority encoder



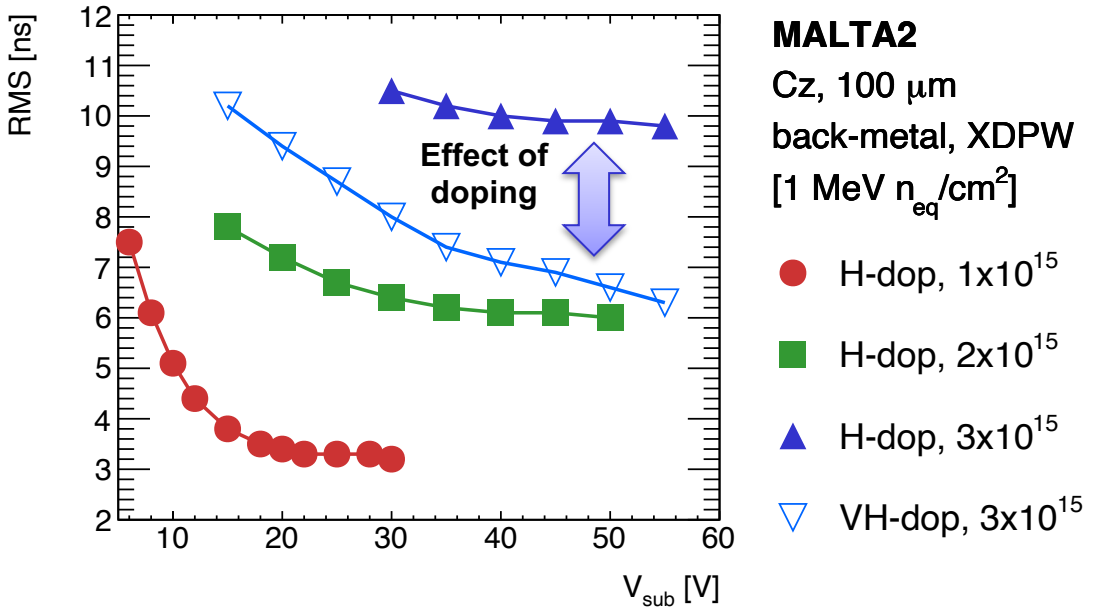
Priority encoder block diagram

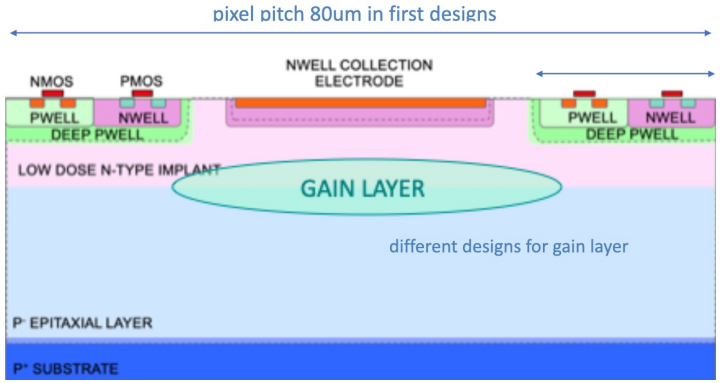
Proposal to DRD3 WG1

DRD3

- 4 months: resubmission Mini-MALTA3
  - Evaluate ultra-high doping (UH-dop) of n-layer
  - Very-high doping (VH-dop) improves wrt high doping (H-dop) after 3e15 n/cm2 Eur. Phys. J. C 83 (2023) 58
- Next 12 months: submission MALTA3
  - Demonstrator larger than 2x2 cm2
  - Optimized PLL for time tagging below 1 ns
  - Reduce the number of serial lines to the chip
  - Full command protocol for chip configuration
  - Optimize number of bits per hit
  - Multiple serial outputs from single chip
- Next 24 months:
  - Evaluate alternative pixel designs: CASSIA?
  - Evaluate alternative group geometries
  - Large area modules: interconnection designs

Detail between high doping (H-dop) and very high doping (VH-dop)



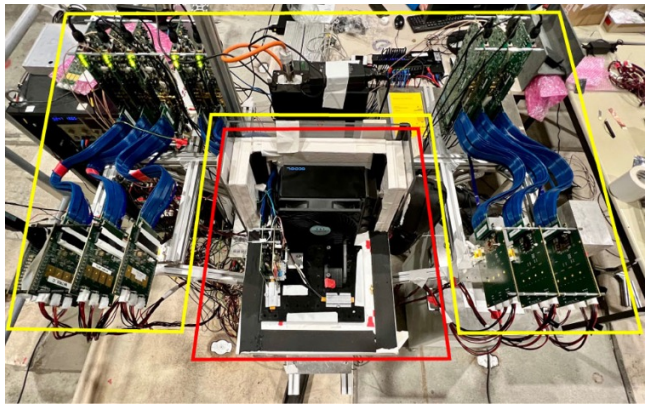


More details: "interconnections and multi-chip flex developments" (WG7 A. Sharma)

Summary

DRD3

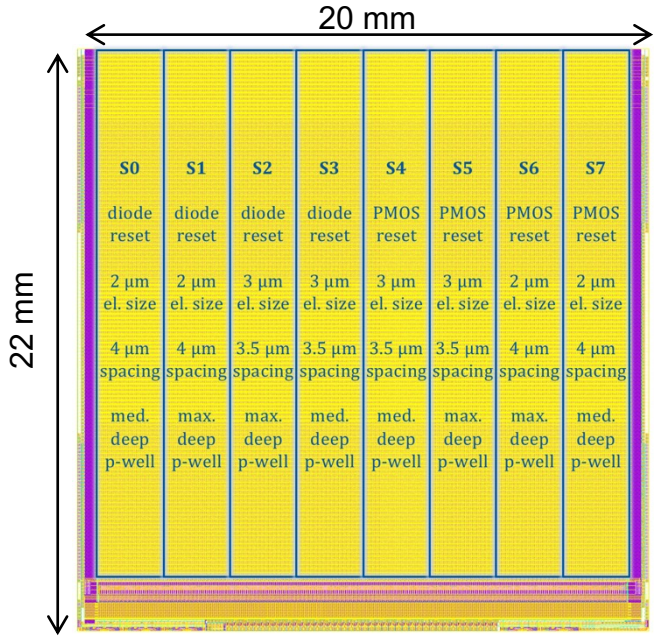
- Asynchronous read-out architecture was developed for MALTA R&D
  - Self-generating reference pulse in groups of 8x2 pixels without clock distribution
  - Power consumption of 80 mW/cm2 and a hit rate capability larger than 1 GSps.
- Propose to develop this architecture further to reach hit rates above 100 MHit/cm2, radiation hardness better than 3e15 n/cm2, and on-chip time tagging below 1 ns, on a matrix larger than 2x2 cm2 compatible with an experiment
  - Hit rates and radiation hardness evaluated with MALTA and MALTA2
  - Sub-nanosecond timing resolution being evaluated with Mini-MALTA3
  - Start with Tower 180 nm CMOS imaging process that is very accessible
- Proposal has direct application in WG5 inside DRD3 WP1
  - MALTA telescope in operation at CERN SPS H6 since 2021
- Project is open for further collaboration

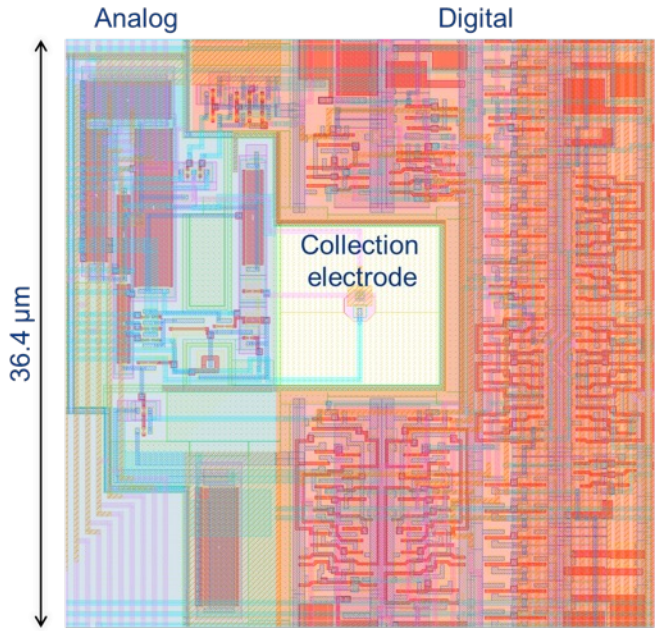


MALTA telescope in SPS H6

Bonus

TowerJazz MALTA





- 22 x 20 mm^2 full size demonstrator
- 512 x 512 pixels
- 8 sectors with different pixel flavors
- Fully clock-less matrix architecture
- Charge information from time-walk
- 10 mW/cm^2 digital power

1. Pixel size 36.4 x 36.4 μm^2
2. 2-3 μm collection electrode
   1. small input capacitance
3. 3.4 - 4 μm spacing to electronics
   1. low cross talk
4. 1 μW/pixel analog power
   1. 70 mW/cm^2 analog power

Mini-MALTA3 block diagram