1st DRD3 week on Solid State Detectors R&D
June 17th-21st - 2024

Adaptation and Modularization of MPW4 Firmware for Integration into the Caribou Boreal Architecture: A Pilot project

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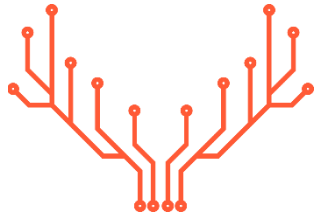
DRD3

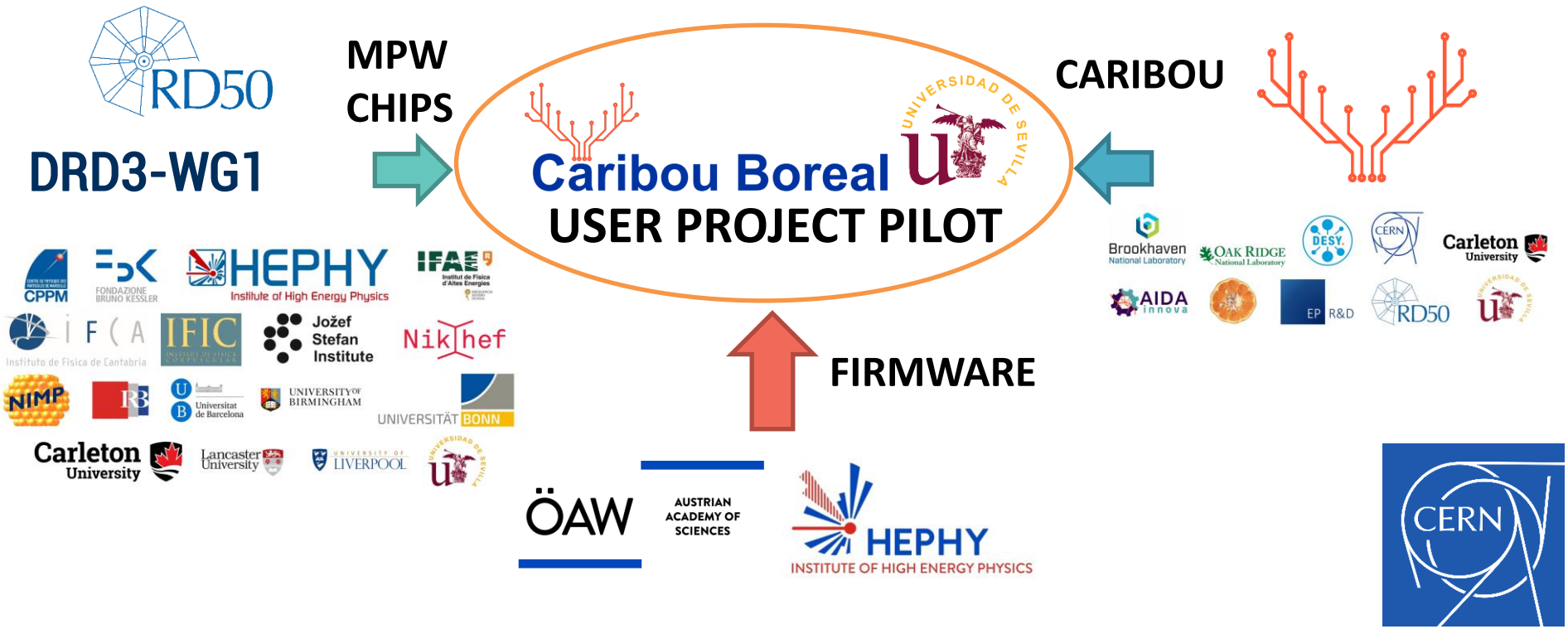


WG1 - https://indico.cern.ch/event/1402825/

INTRODUCTION

Context

This project receives input from the following institutions



INTRODUCTION

Objectives

The main objective of our project is to modularize and adapt the MPW4 actual firmware to the Caribou's new Boreal firmware architecture.

Our present DAQ runs only in the Zynq 7000 SoC FPGA. The new Boreal architecture is modular, with clear frontiers between blocks, easying maintenance, adaptability and opening the possibility to use also the new Zynq UltraScale+ SoC FPGA.

Caribou System Architecture

1) System-on-Chip (SoC) board

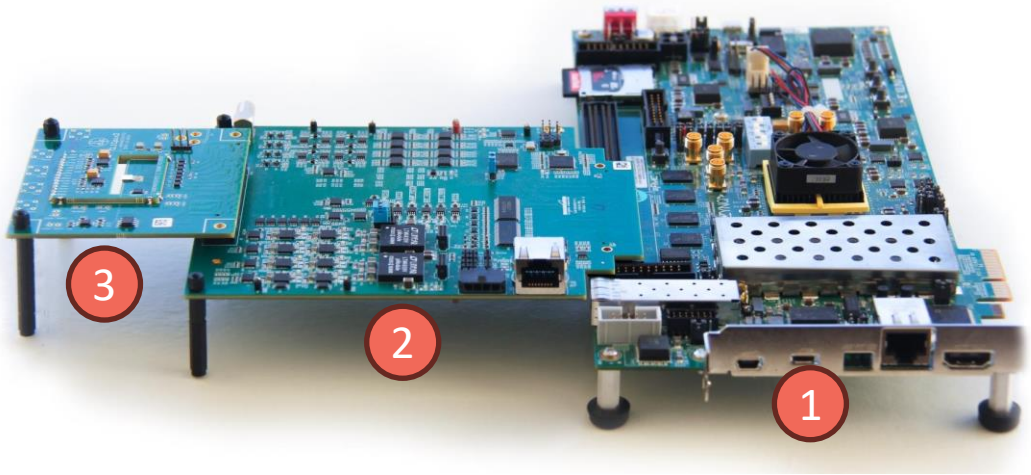
- ie: Xilinx ZC706 evaluation board
- Embedded CPU runs DAQ and control software
- FPGA runs custom firmware for detector control and readout

2) Control and Readout (CaR) interface board

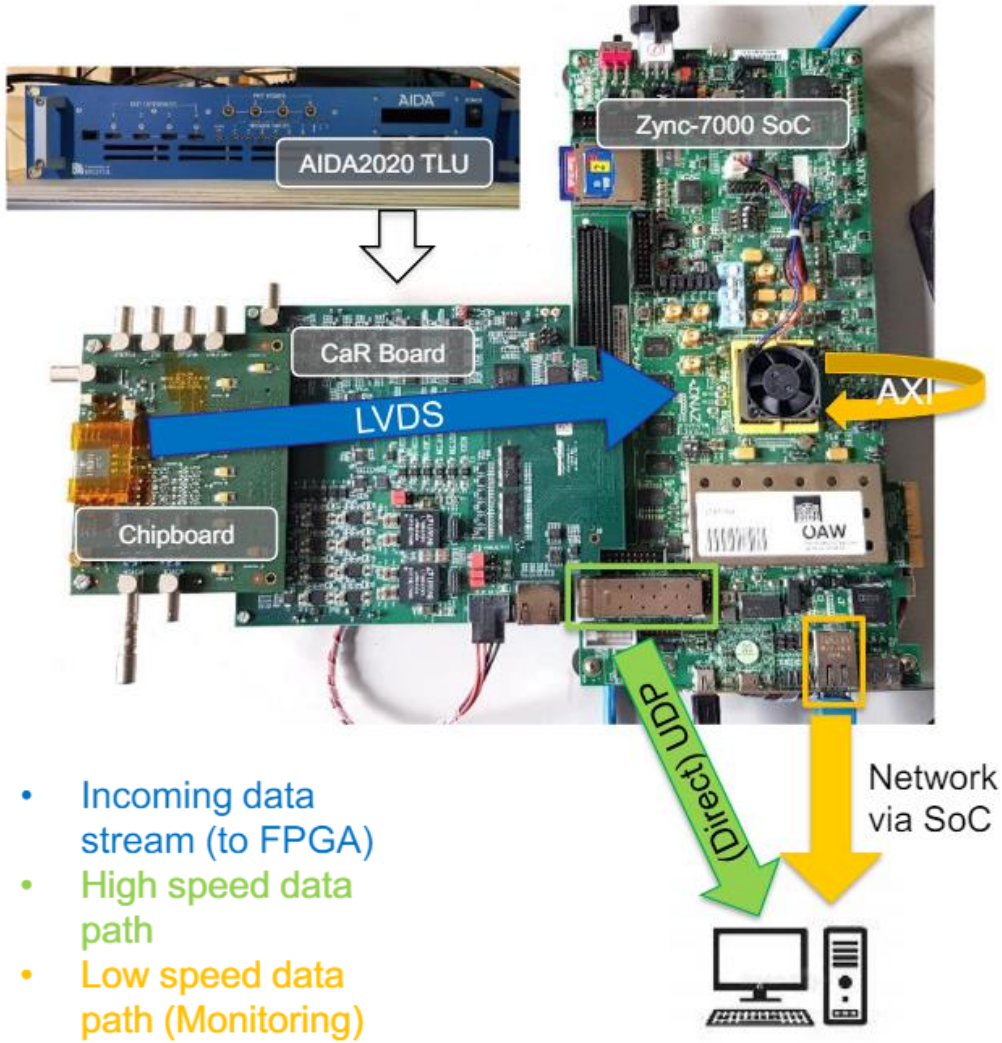
- Physical interface from SoC to detector
- CaR – SoC connection extendable via FMC cable

3) Detector chip board

- Custom low-cost PCB



RD50-MPW Actual DAQ



Hardware:

- Chip Board (Wire-Bonding MPW4)
- Caribou Card (1.4)
- Zynq ZC706 (Zynq 7000 SoC)

Firmware (SoC, PL):

- Propietary firmware for MPW3-MPW4 (developed by HEPHY)
  - Communication via AXI with PS

Software (SoC, PS Arm Cortex-A9):

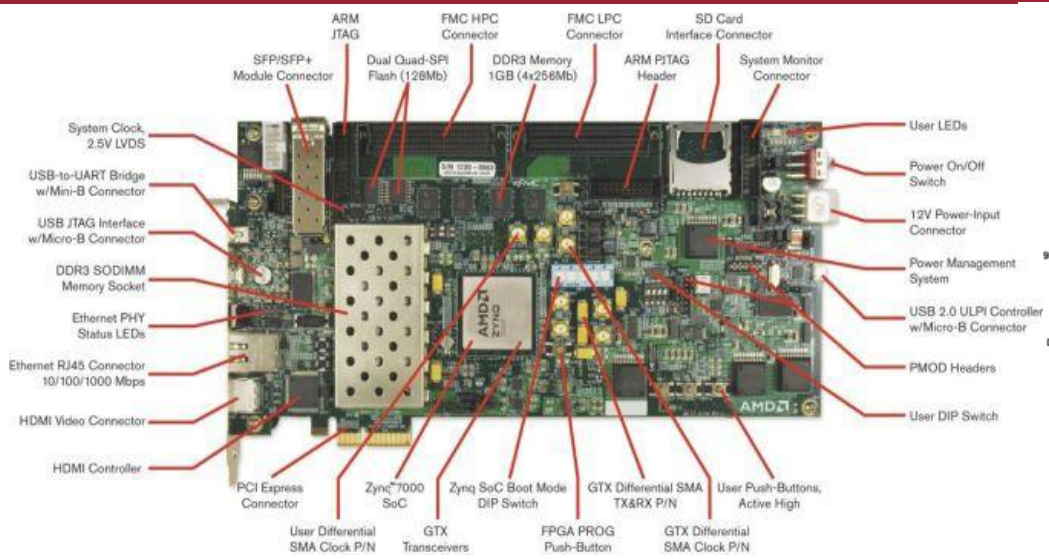
- Yocto Linux SO
- Caribou Peary Framework
  - 2 Read-out Paths (High and Low)

Software (External PC or SoC):

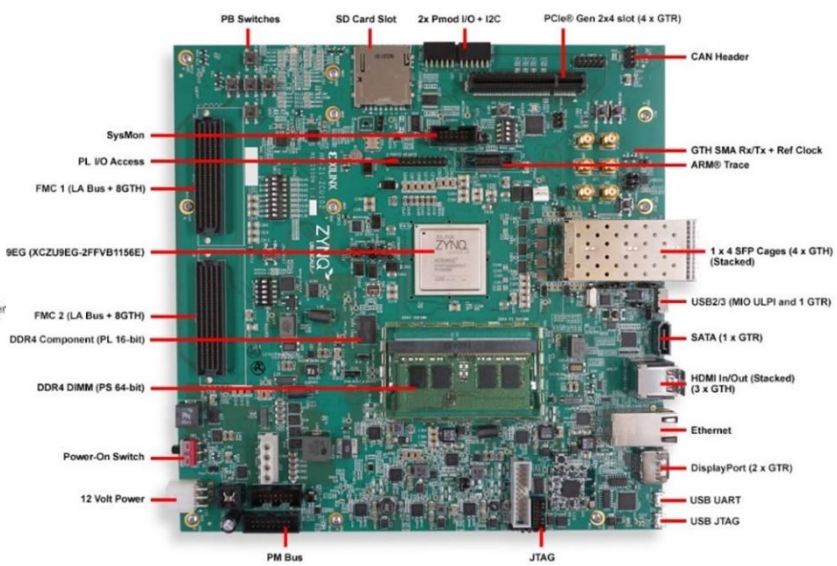
- GUI-Client (connect to Peary)

*Figure from Patrick Sieberer

RD50-MPW DAQ Evolution



ZC-706 Card (Zync 7000 SoC FPGA)



ZCU-102 Card (Zynq Ultrascale+)

	Legacy	**Boreal Pilot project**
Hardware	ZC-706	ZCU-102/ZC-706
Firmware	Propietary	Boreal Caribou
Software	Peary	Peary (Boreal adapted)
GUI	Propietary	Propietary (Boreal adapted)

RD50-MPW4 Digital Periphery

- **Control Status Registers (CSRs)**:
  - -Divided into EOC (configures pixel bits in double columns) and Peripheral (controls data transmission, TimeStamps, DACs).
  - -Accessed through a Wishbone bus.
- **Slow Control (I2C)**:
  - -Configures the ASIC and reads internal circuit information.
  - -I2C module acts as the master on the Wishbone bus for read/write operations.
- **End Of Columns (EOCs)**:
  - -Handles the readout and configuration of double columns.
  - -Utilizes finite state machines for data handling.
  - -Contains 544 control status registers for pixel configuration.
- **Control Unit (CU)**:
  - -Manages data flow from EOC FIFOs to the transmission FIFO.
  - -Ensures smooth data handling and readout.
- **TX Unit**:
  - -TX FIFO: Temporarily stores data from EOCs before it is read by the Data TX Unit.
  - - The Data TX Unit Packs data into frames, serializes, and transmits data at 640 Mbps after encoding.
- **Analog Bias Block**:
  - -Sets bias voltages needed in the pixel matrix.
  - -Configured through DACs programmed via Wishbone on CSRs.

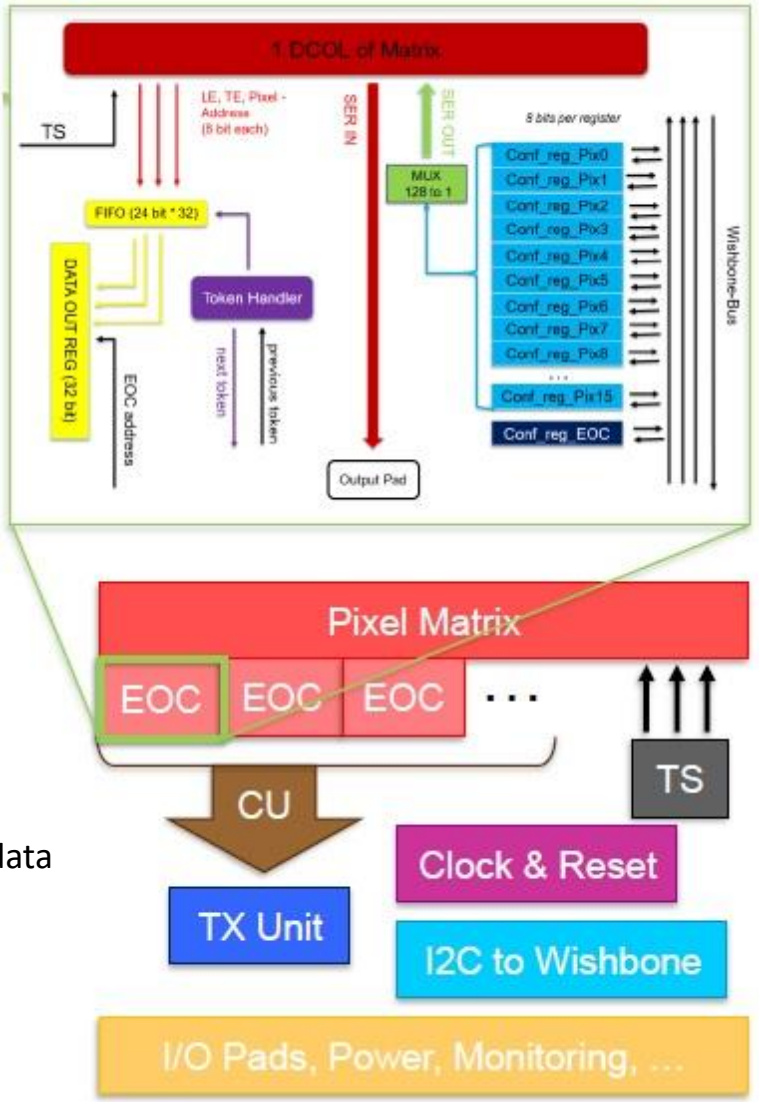


*Figure from Patrick Sieberer

Firmware Analysis

Pilot project: **ADAPT AND MODULARIZE firmware MPW4** for integration to **User Part** of **Caribou Boreal Firmware** architecture. See details in presentation by Younes Otarid

1. Starting from the **original MPW4 firmware provided by HEPHY**

2. The blocks that we have analyzed from the firmware are the following:
    - Processing System (ZC706)
    - Clock Generation (PLL)
    - Reset Block
    - AXI Interconnect
    - Controls Registers
    - Status Registers
    - I2C Slow Control
    - AXI Stream FIFO RX Data
    - GBE-SFP Fast-Readout
    - TLU Control
    - Simulations Blocks (TLU, MPW4)
    - External Control
    - Buffers I/O

***More details: See WG5,** Caribou: A versatile data acquisition system for silicon pixel detector prototyping, Younes Otarid*

Firmware Modularization

- **The blocks that we are going to adapt and modularize:**
  - MPW4 Slow Control (I2C)
  - MPW4 Slow Readout (AXI Stream FIFO)
  - MPW4 Fast-Readout (GBE-SFP)
  - TLU Control
- **The Processing System blocks for the Processor, including Clock Generation (PLL), Reset Block, and AXI Interconnect, are integrated into the Boreal System Part*.**
- Control Registers and Status Registers are integrated into the user registers block.
- The External Control and Buffers I/O are integrated into each of the respective DUT modules.

***More details: See WG5,** *Caribou: A versatile data acquisition system for silicon pixel detector prototyping, Younes Otarid*

Workflow and Software

Simulation

- Simulation of the every block of MPW4-DAQ separately and working together (Cocotb in Python).

CI/CD Workflow

- Add the simulation and verification of the MPW4 blocks and verify in the Continuous Integration /Continuous Delivery workflow (Gitlab).

Peary Software

- Integration of libraries of Peary software and GUI Client for the MPW4 device in the new Boreal Firmware Architecture

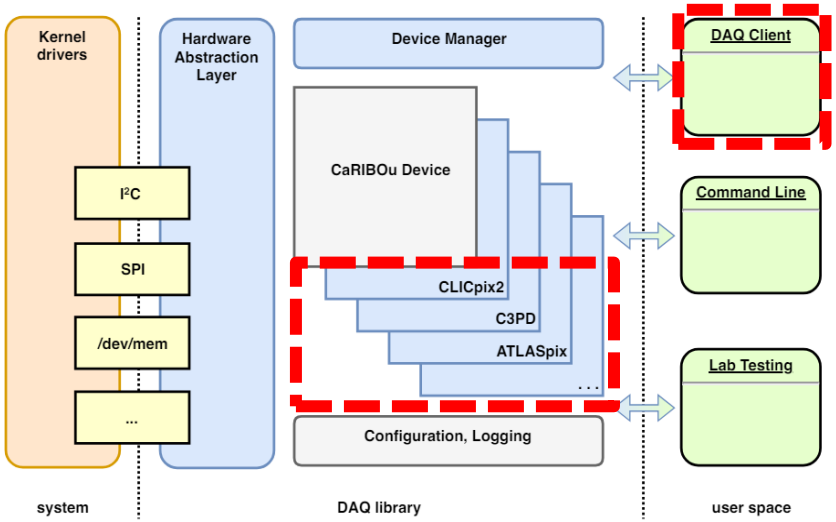
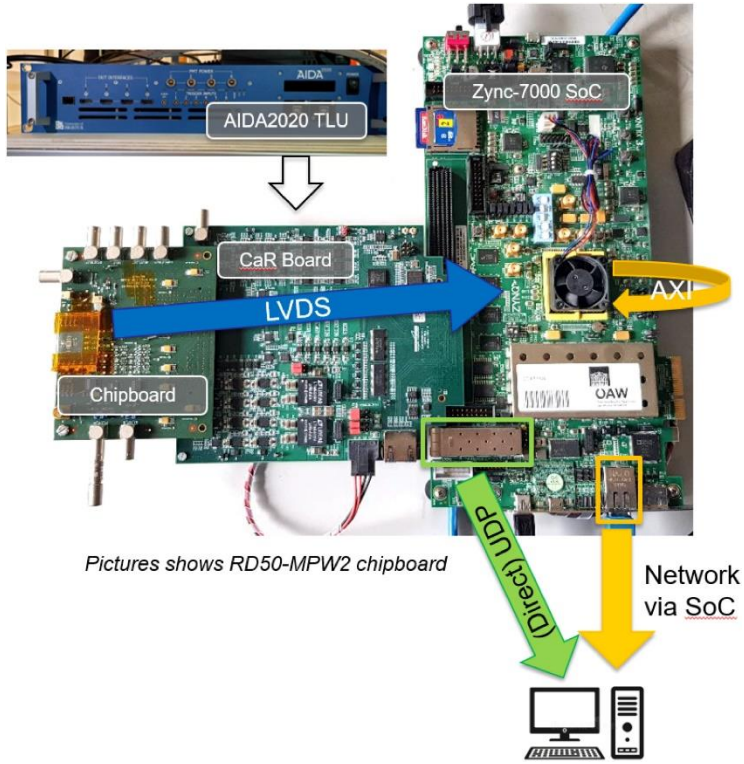


*Figure from Thomas Vanat

Testing

Test the complete system on both the ZC706 board and the ZCU102 board (UltraScale+)



Pictures shows RD50-MPW2 chipboard

Phases

Phase 0: Study, analyze, and divide the original HEPHY firmware code into functional components.

Phase 1: Base example in Boreal architecture (developed by Younes) and integration of MPW4 chip I2C control.

Phase 2: Cocotb Simulation and CI workflow of MPW4 I2C control.

Phase 3: I2C control and configuration of the Caribou power supplies in the Peary software. Verification of I2C control with the system and MPW4.

Phase 4: Integrate module firmware TLU control and readout of the MPW4 chip.

Phase 5: Cocotb Simulation and CI workflow of TLU an readout of the MPW4 chip.

Phase 6: Integrate the libraries for readout and TLU Peary software

.

Phase 7: Conduct a test with the complete systems (ZC706 and ZCU102).

CONCLUSIONS

We aim to modularize and adapt the MPW4 firmware developed by HEPHY into the user part of Caribou's new Boreal firmware architecture.

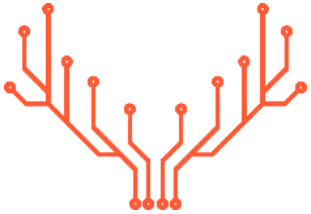
Additionally, the following tasks will be carried out:

- Simulations with Cocotb and Questa of the modular blocks.
- Integration in CI Workflow
- Adaptation of Peary software libraries for the use of MPW4 in Boreal.
- Verification in ZC706 and the UltraScale+ ZCU102.

This pilot project uses the MPW4 as the first chip in the new Boreal architecture.

ACKNOWLEDGMENT

- **Caribou Collaboration**



- **Institutes of High Energy Physics**

- **DRD3(RD50)-MPW Collaboration**

Thanks you for your attention

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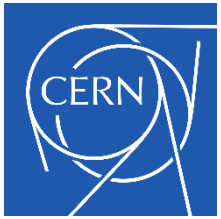

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