CMOS Sensors with internal gain

CASSIA **C**MOS **A**ctive **S**en**S**or with **I**nternal **A**mplification

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- based on our experience with Tower Semiconductors we recently started a new development to implement **pixel implant structures with internal gain** in CMOS TJ 180nm
- Development started in 2023 between CERN and University Zagreb/ Institute of Electronics FER
- **We actively look for groups interested to join developments**

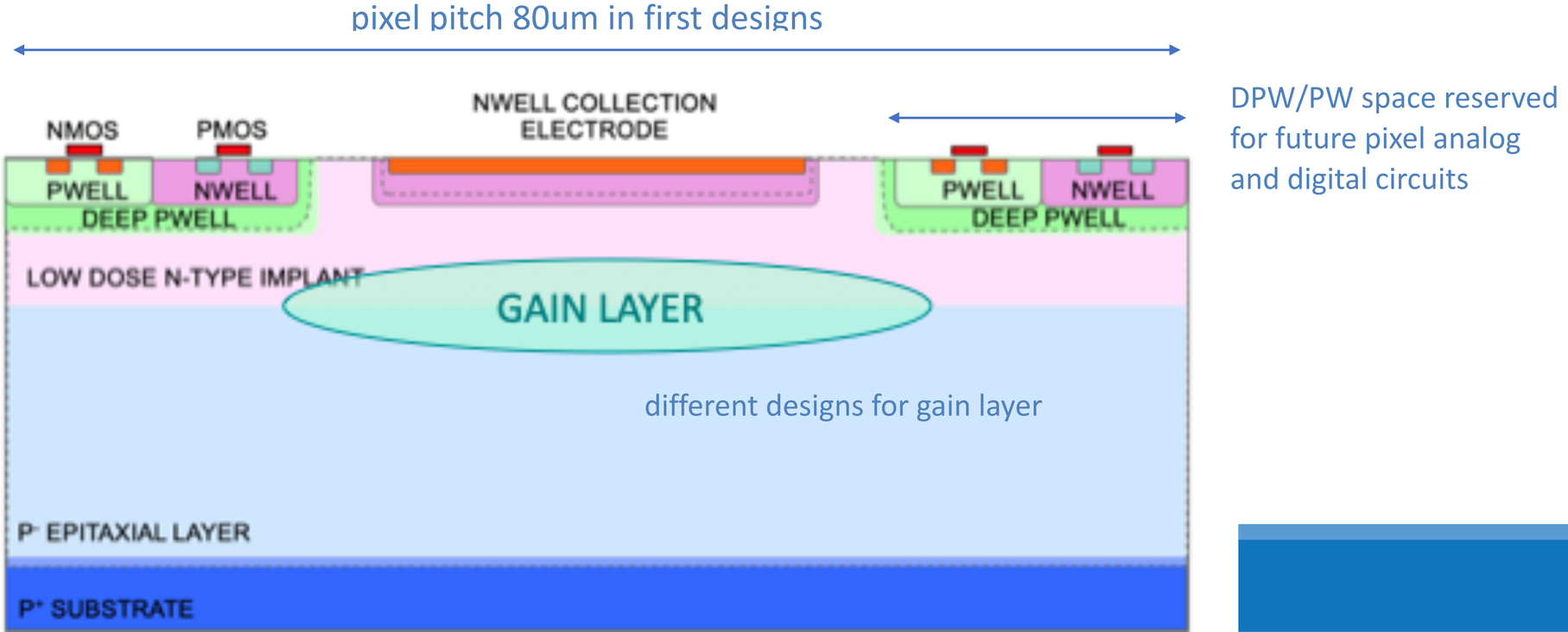
Sensor with internal gain in CMOS imaging process

- Main goal is to implement a **pixel implant structure with internal gain** in a CMOS imaging process for future use in MAPS for **tracking, timing or time-tagging**
- Design the **pixel implant structure with internal gain** in a way that it can be **implemented in commonly used MAPS pixel matrix** (either existing or future sensors)
- **Internal gain** for
  - Much higher signal-to-noise in thin monolithic sensors
  - Substantial improvement of time resolution for tracking sensors
  - Aim at limited gain in linear amplification range to keep noise rate low enough for HEP trackers
- **Discussion with Tower Semiconductor** Research director indicated that this **can be done in TJ180nm CIS imaging process** on which many HEP sensors are based and we have substantial experience for tuning implant profiles
- A **transfer of results to finer-pitch processes** (e.g. 65nm) is envisaged for a future stage after initial developments in 180nm

Initial design idea for sensor with internal gain

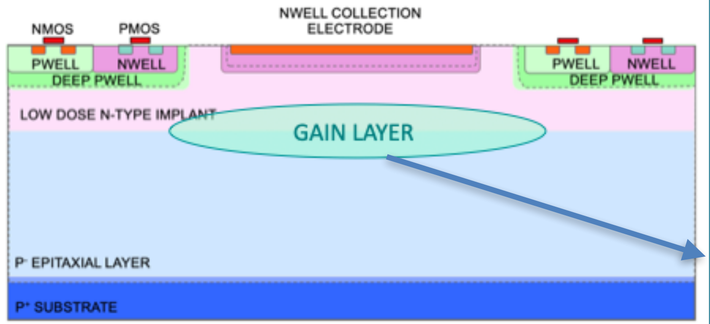
- inspired by development of LGAD sensors but applied to industrial CMOS process (200mm wafer, 0.18um CMOS process with high production volume)

- **“Tracker-like” pixels with 80um pitch** (first prototype)
  - larger round electrodes (~40um diagonal) but also enlarged area for analog and digital circuit
  - DPW for full CMOS electronics in pixel already foreseen now to allow future scaling of results to larger matrix



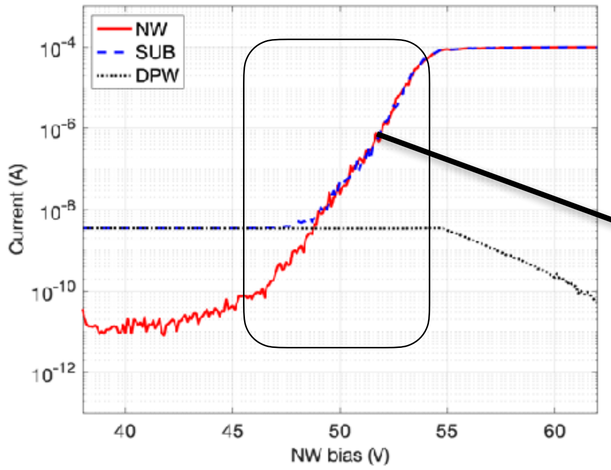
Gain layer design ideas implemented in first CASSIA prototype

- Main focus of **first prototype:**
  - Is it possible to implement a **functional gain layer in standard 180nm** process within **voltage limitations of CMOS process**
  - Study the **gain layer operation as function of combination of n-implants and p-layer gain implants** (i.e. variation of doping concentration and depth)
  - Can we achieve a **Limited Gain Mode** and where does the **Geiger-Mode start (SPAD)**?
  - What are **"safe" design dimensions** to avoid unwanted break down between different wells

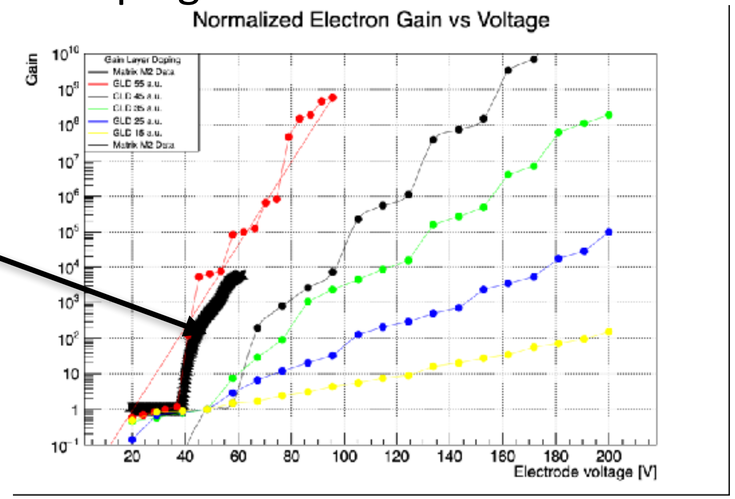


Multiple Gain layer designs in pixel array
- different combination of n- and p-implants
- variation in doping concentration and depth
- different geometries for gain layer edge

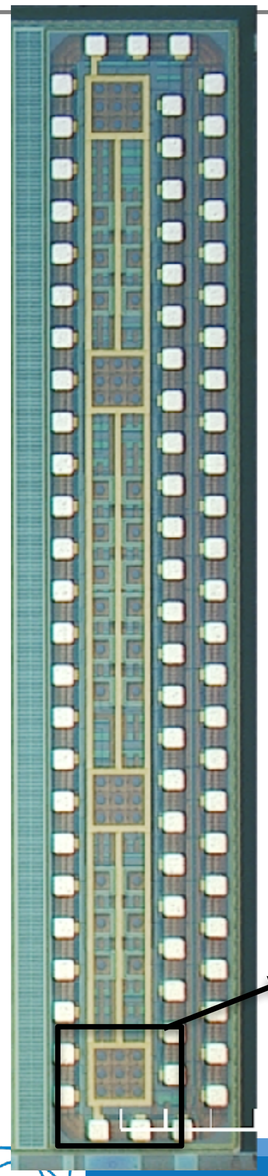
IV measurement on CASSIA Matrix 2



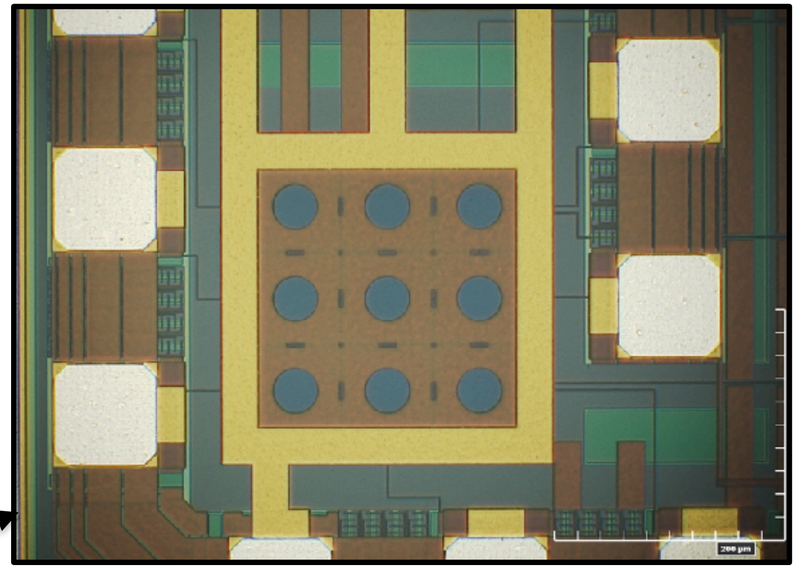
Simulation of gain for different GL doping concentration



First CASSIA prototype for sensors with internal gain



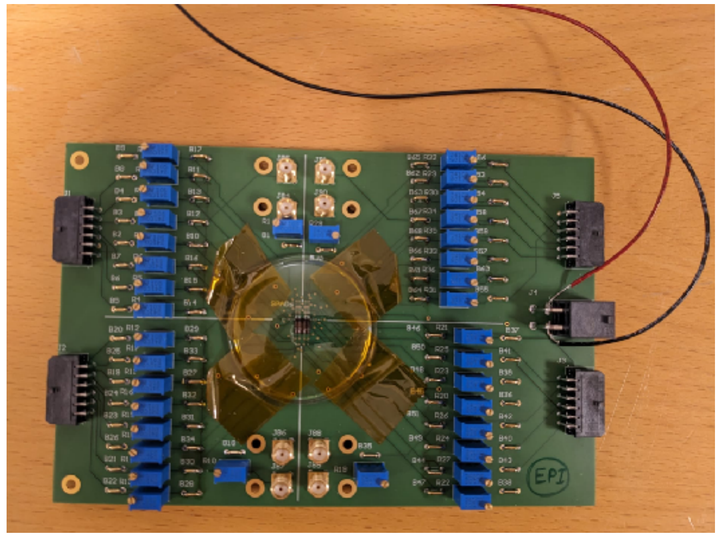
- received end 2023 , produced in TJ180nm CIS in parallel with Mini-MALTA3 MPW on 25um EPI and thick HR Cz substrates
- Designed in collaboration between CERN EP-ADE-TK and Uni Zagreb



- **Prototype contains:**
- **Four 3x3 matrixes** : 1 matrix without gain layer and 3 matrices with different gain layers aimed at tests with sources/beam tests
  - different n-/p-GL doping concentration and depth
- **24 single pixels** with different implant designs for electrical measurements and laser
  - different n-/p-GL doping concentration and depth
  - different GL edge designs and implant spacings

First tests of CASSIA sensors with internal gain

- PCB designed and assembled at CERN for first IV tests and laser tests
- Keithley PSU for IV measurements
  - One for Bias of Central Pixel
  - One For the rest o the Matrix
  - One for DPW
  - One for SUB
- several PCB with sensor in assembly - they can be shared for measurements



- C2-HV BROADBAND AMPLIFIER, 2 GHz, 40 dB
  - Internal Bias –Tee
  - Highly linear
  - Ouput limited to +/- 1V

- First IV tests showed that large voltage can be applied without shorts between implants
- Stable operation with 100V across gain layer and between n-electrode and adjacent PW
- Studied IV measurements on first set of matrices
  - determine break down regions for different designs
- First pulse measurements with IR laser (1060nm)
  - is dual operation in Limited-Gain mode and SPAD-like operation possible?

IV measurements on CASSIA prototype matrices

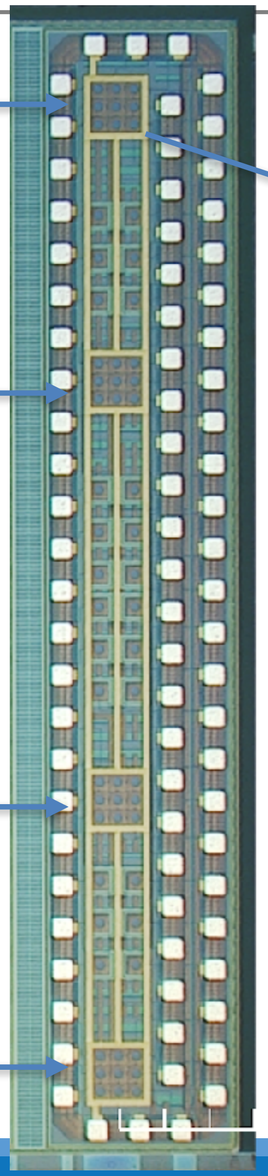
Matrix with GL design M4

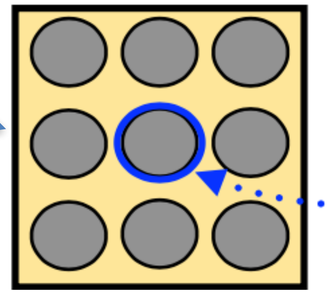
Matrix with GL design M3

different GL doping and depth

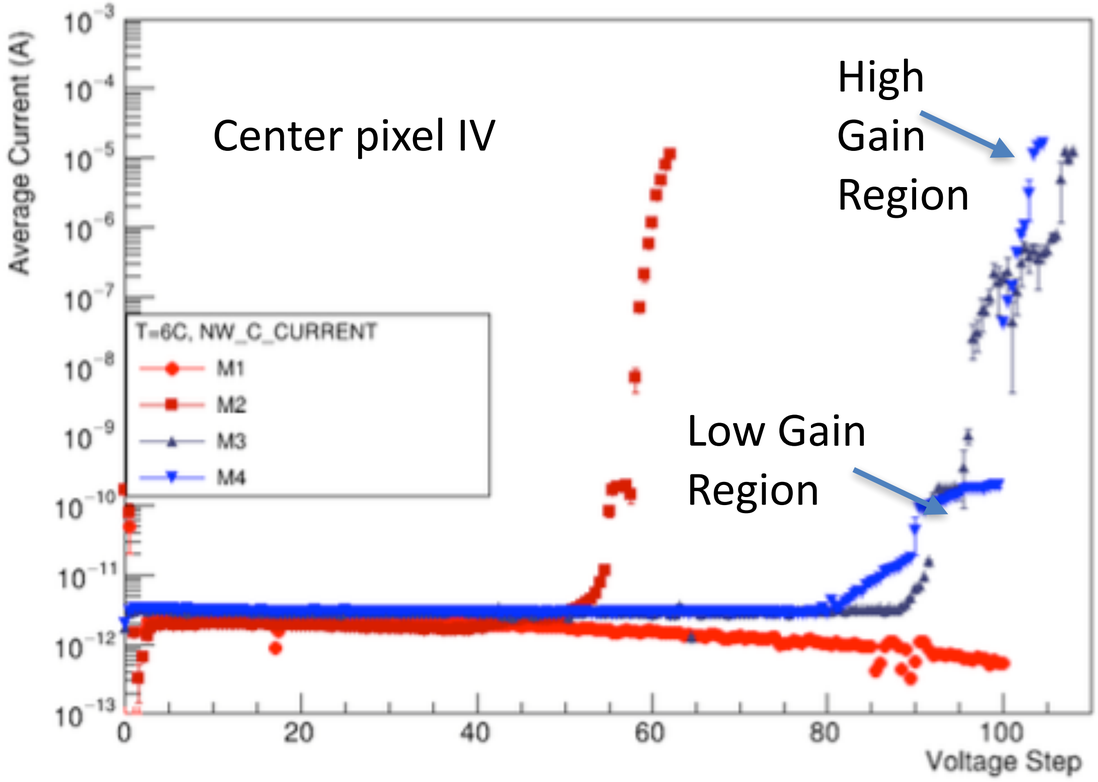
Matrix with GL design M2

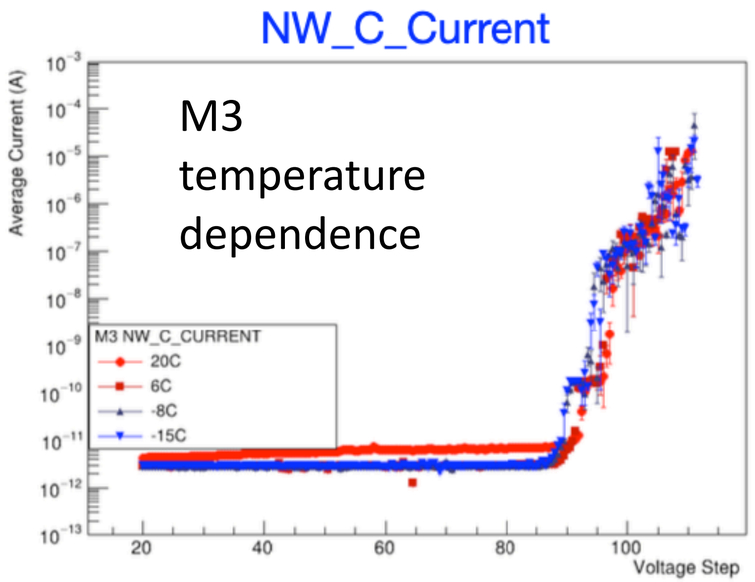
Matrix M1 without GL





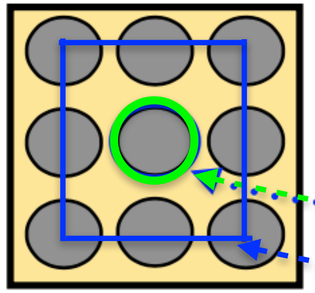
adjacent pixel on NW voltage
PW = -6V
substrate = -10V





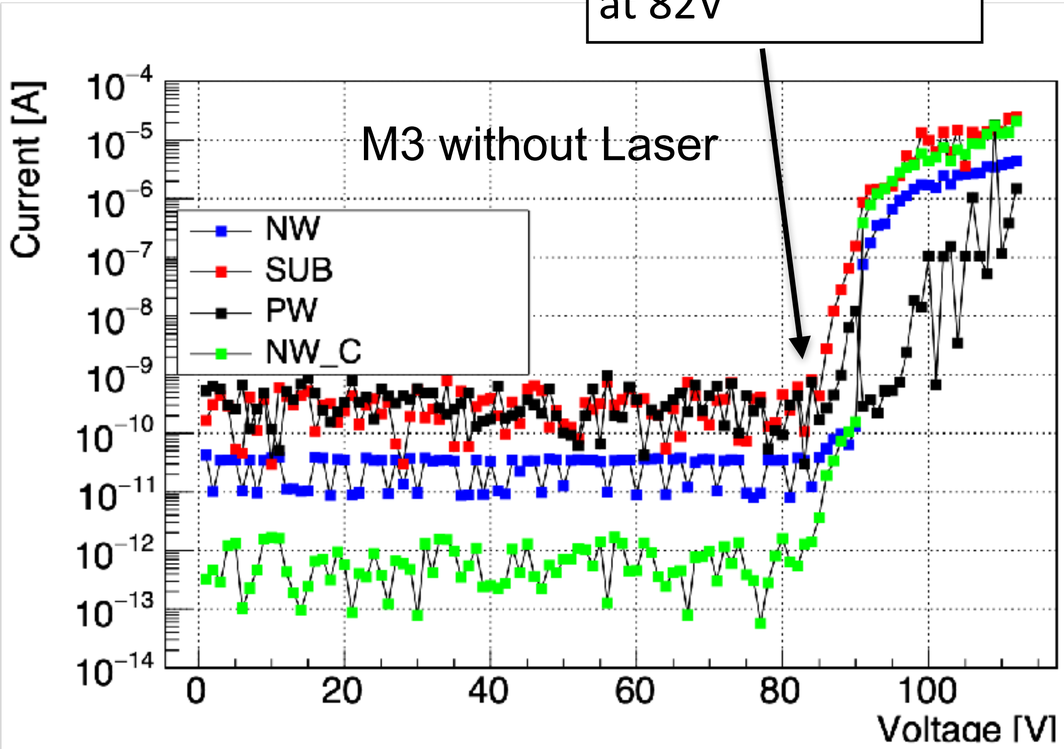
- M2-M4: Observe **gain onset between 50V to 90V** dependent on GL design and adjacent PW
- Observe 2 regions of different gain (Low Gain region and SPAD region
- M1 (no GL) - I~1pA stable to >100V

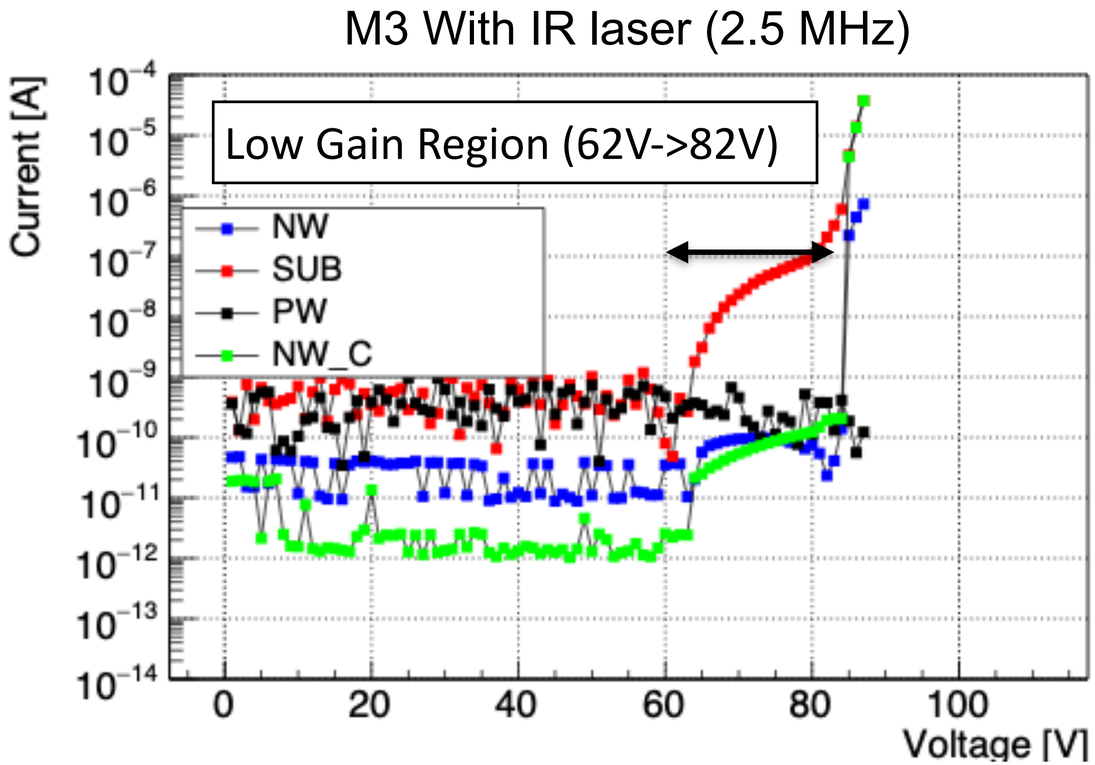
CASSIA prototype matrix M3 with IR laser pulses



adjacent pixel on NW voltage
PW = -6V
substrate = -10V

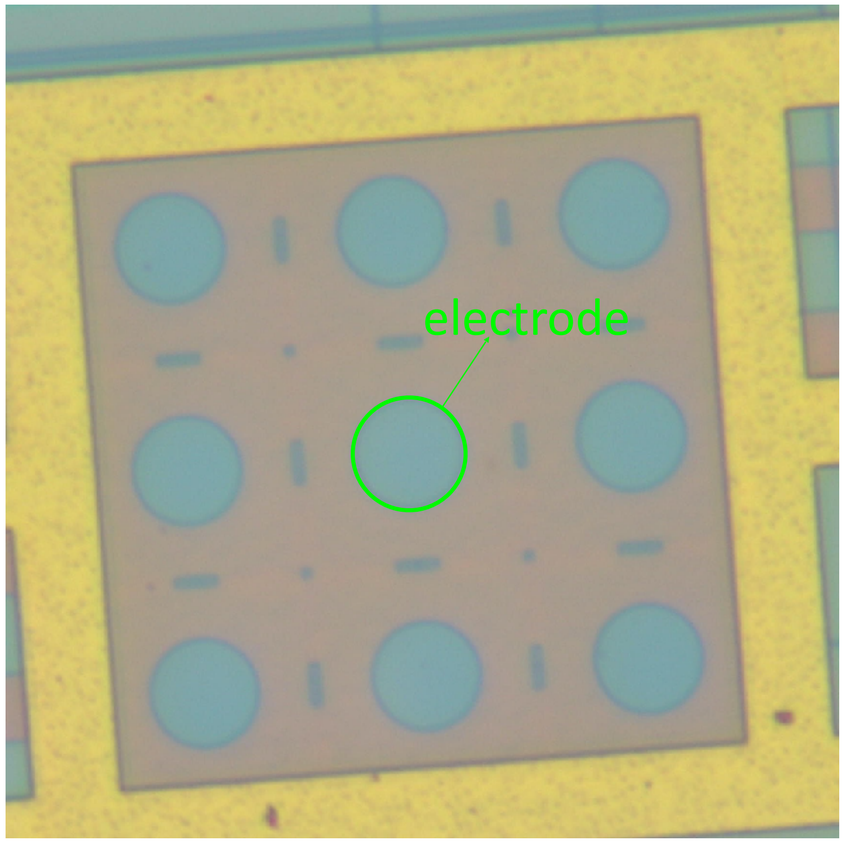
- "Low Gain" region observed between 62V and 82V
  - stable low current at I_pixel~ 1pA in this region
- Promising for low DCR operation





Where does gain happen?

- Light emission measurements -> See Tomislav's presentation

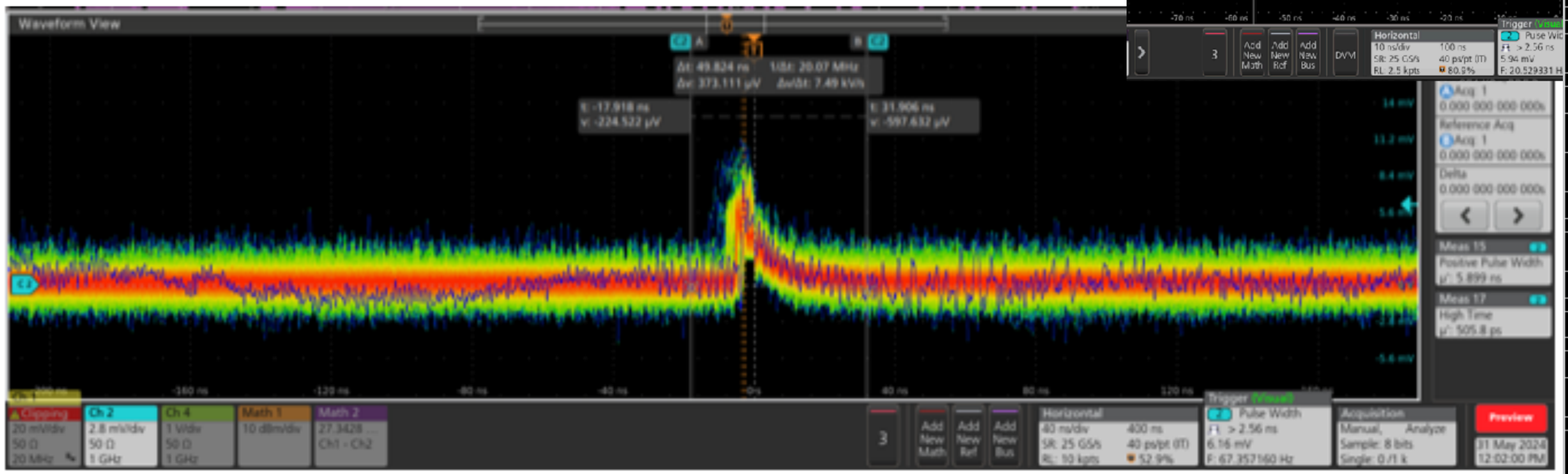


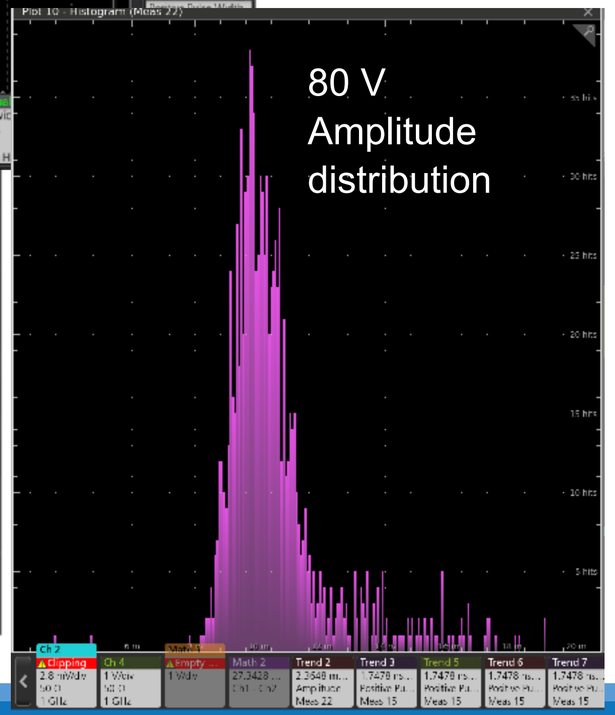
Sensor biased to 110V (high reverse current) to stimulate light emission

- Active area with light emission matches design GL diameter
- this confirms simulation results of gain vs position across GL
- effective tool to study edge break down and future optimisation of GL edge

CASSIA pulse spectrum (IR 1060nm pulses) - Low Gain region

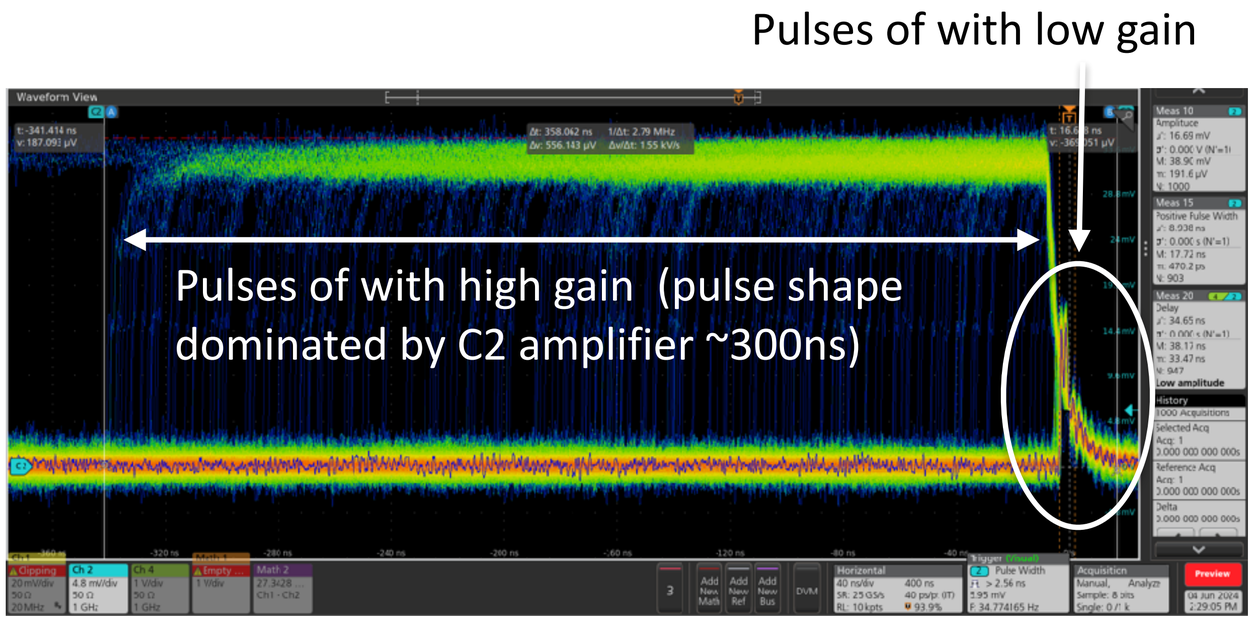
- Tested CASSIA sensor with IR TCT setup in ADE-TK
  - previously also used for Atlas HGTD measurements
  - sensor center pixel connected to Civic C2 amplifier (biased through bias-T in amplifier)
- Operated sensor in Low Gain Mode (78V to 80V)

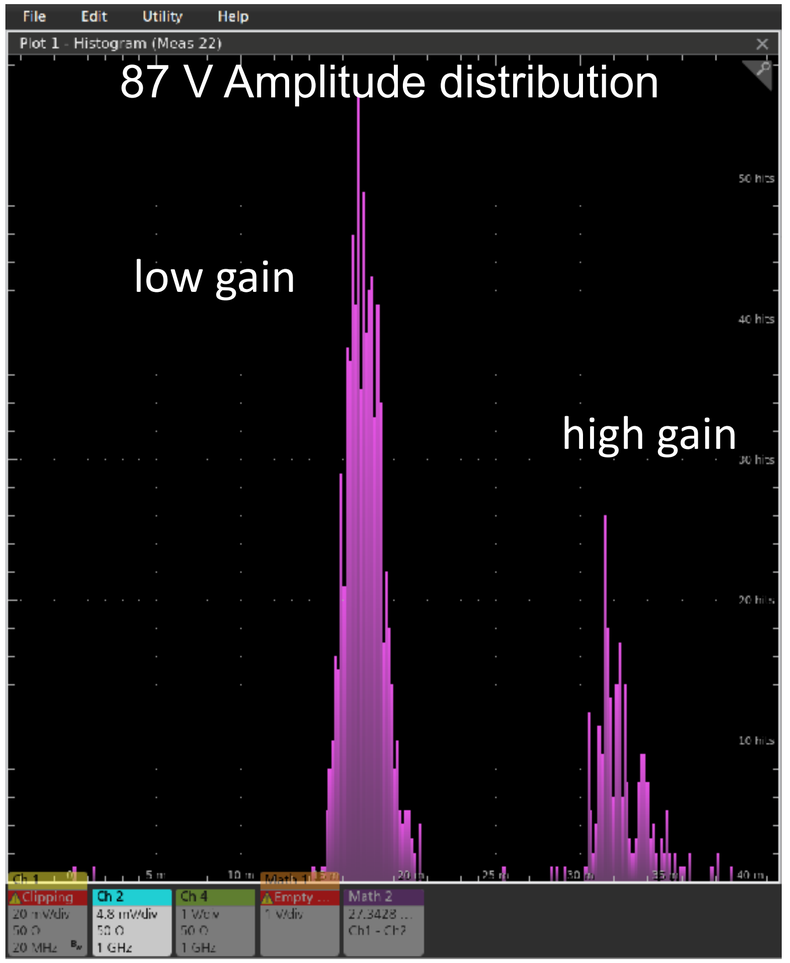




CASSIA pulse spectrum (IR 1060nm pulses) - Transition to High Gain region

- Operated sensor in on-set of high region at 87V
  - observe two spectra of pulses with low gain and high gain simultaneously





See more results in Tomislav's Presentation on the CASSIA project proposal

CASSIA Outlook

- We propose with CASSIA a project to engineer **pixel implant structure with internal gain** in a CMOS imaging process for future use in MAPS for **tracking, timing or time-tagging**
- As a first step we designed **pixel implant structure with internal gain** in a way that it can be **implemented in commonly used MAPS pixel matrix** (either existing or future sensors)
- **The first CASSIA prototype measurements** showed
  - We can operated sensors up to 100V+
  - Gain layer operation starts between 45V and 90V depending on GL design, doping concentration and depth
  - First IR laser measurements indicate a Low Gain Mode of operation voltage window of ~ 20V before high gain/SPAD-like operation starts
- **Next steps are manifold:**
  - Systematic study of GL behaviour as function of implant design/process; study dark-count rate; engineer GL edge for full pixel efficiency ,…
  - Design suitable in-pixel amplifier/quenching circuits, …
- **See Tomislav's presentation on the proposed CASSIA project for DRD3.1**