Applying DMAPS technology to the Upgrade of the Belle II Vertex Detector

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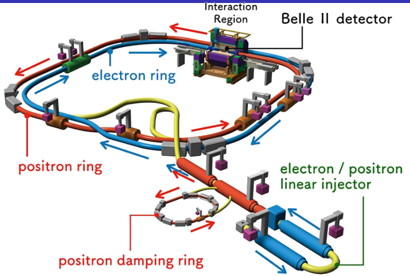
on behalf of the Belle II VTX collaboration

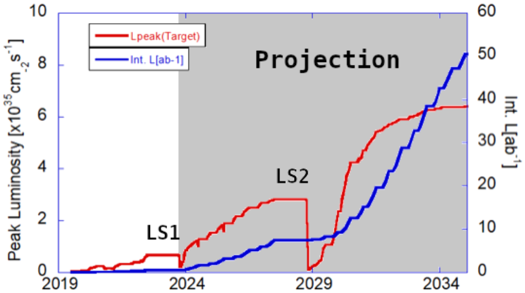
1^{st} DRD3 week on Solid State Detectors R&D

Jun 17^{th} 2024

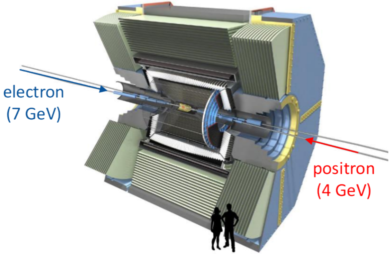
The Belle II Experiment

- Located at the SuperKEKB collider in Tsukuba/Japan
- Asymmetric $e^+ - e^-$ collisions
- $\sqrt{s} = M_{\Upsilon(4S)} = 10.58\,\text{GeV}$
- World record peak luminosity in 2022: $4.7 \times 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$
- Operation just started after Long Shutdown 1 (LS1)



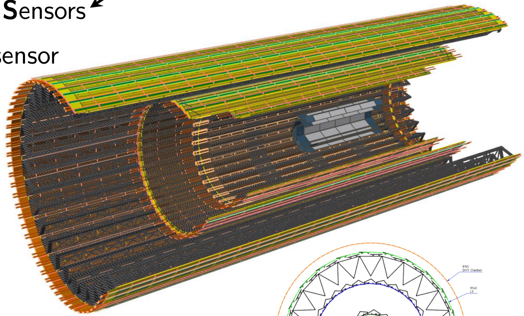


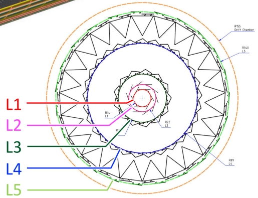
Belle II detector



The VTX Upgrade Proposal

- Planned for LS2 ∼ 2028, CDR in publishing process
- 5 straight layers with **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensors ← Low Occupancy
- Identical chips on all layers: **O**ptimized **BEL**le II p**IX**el sensor
- Different features enabled on different layers
- **L1 & L2 (iVTX):**
  - All silicon ladders
  - Air cooling (constrains power)
- **L3 to L5 (oVTX):**
  - Carbon fiber support frame
  - Cold plate with liquid cooling



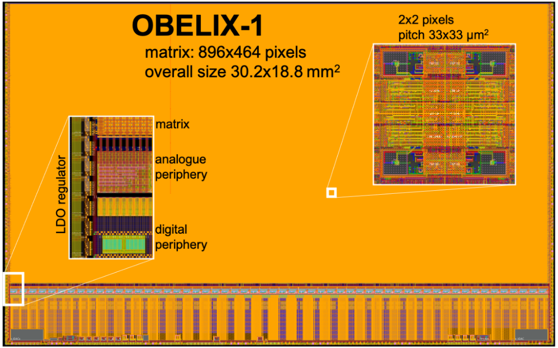


	L1	L2	L3	L4	L5	Unit
Radius	14.1	22.1	39.1	89.5	140.0	mm
# Ladders	6	10	17	40	31	
# Sensors	4	4	7	16	2 x 24	per ladder
Expected hitrate*	19.6	7.5	5.1	1.2	0.7	MHz/cm^2
Material budget	0.2	0.2	0.3	0.5	0.8	$\% X_0$

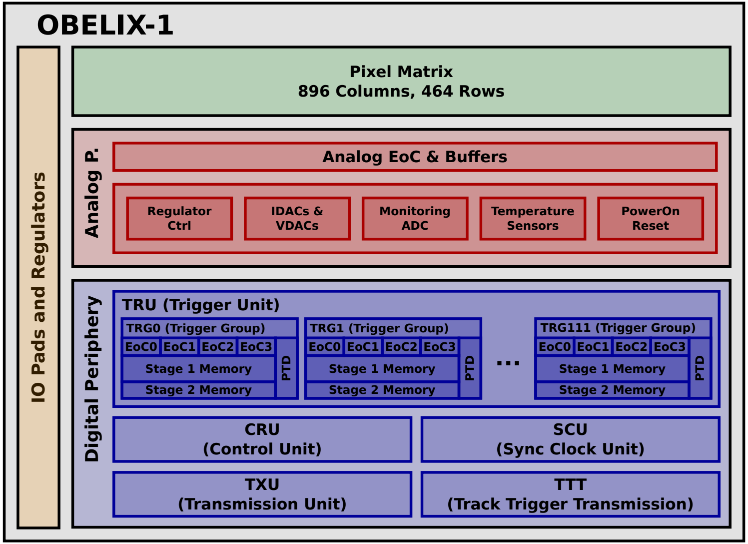
*: Large uncertainties due to beam background extrapolation, possible changes in IR (interaction region)

The OBELIX chip

- Matrix inherited from TJ-Monopix2, size adjusted
- 464 rows and 896 columns
- Timestamp resolution: $\sim 50\,\text{ns}$
- Power: $< 200\,\text{mW/cm}^2$
- TID tolerance: $1\,\text{MGy}$
- NIEL tolerance: $5 \times 10^{14}\,\text{n}_{\text{eq}}/\text{cm}^2$
- Trigger latency $10\,\mu\text{s}$, Trigger rate of $> 30\,\text{kHz}$
- Hitrates up to $120\,\text{MHz/cm}^2$
- ⇨ Hitrate spikes due to injection background
- ⇨ Generous margin for all beam background scenarios
- For TJ-Monopix2 Results, see Talk from Lars Schall



OBELIX Block Diagram



Analog:

- Column drain architecture from TJ-Monopix2
- Monitoring ADC
- Temperature sensors

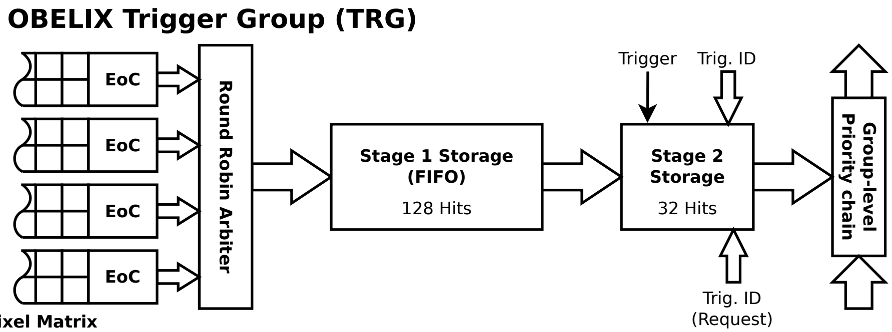
Power Supply:

- On-chip LDOs

Digital:

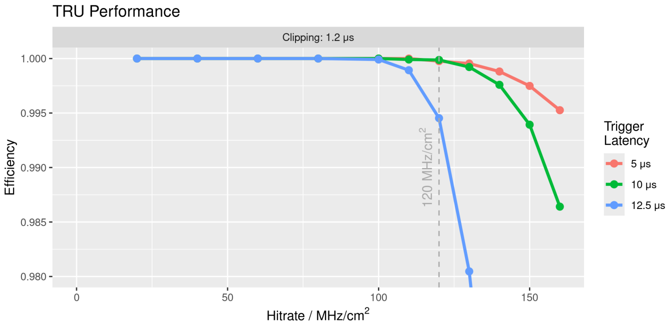
- TRU: Pixel readout, trigger processing
- PTD: Part of TRU for precision timing
- TTT: Fast transmission in parallel for contribution to Belle II Trigger

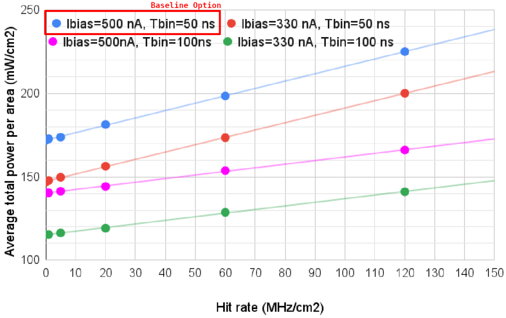
OBELIX Trigger Processing



- Trigger memory: 112 Tigger Groups, for 8 columns each
- Sophisticated 2 stage memory design
- Stage 1: Pre-trigger buffer **SRAM**, low power
- Stage 2: **Associative memory** to match trigger, power hungy
- Buffer sizing driven by power and hitrate, evaluated with extensive simulations

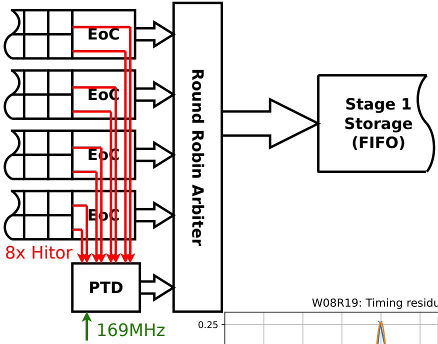
Trigger System: Simulations



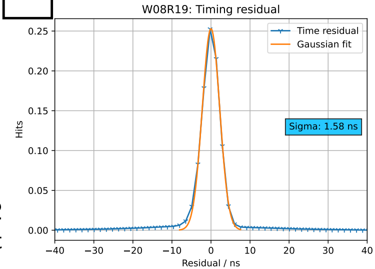


- Simulation includes: clustering & charge/ToT conversion
- Calibrated with TJ-Monopix2 results
- Power slightly above budget for 120 MHz/cm^2
- Clock frequency or analog bias current could be reduced

Peripheral Time to Digital converter

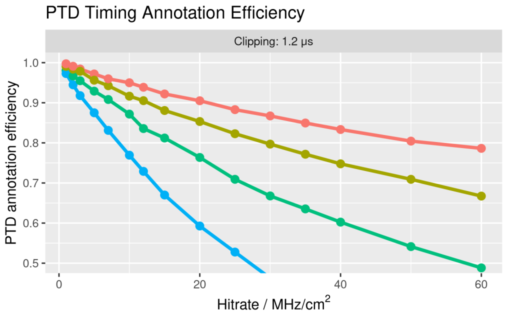


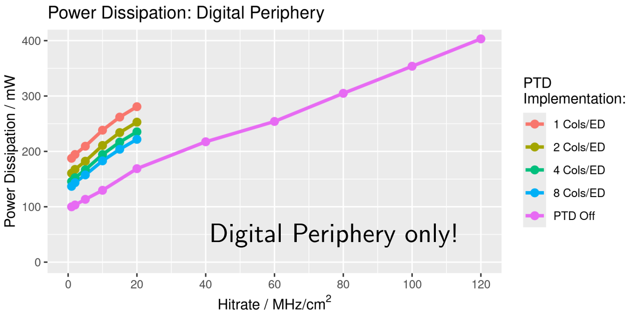
- Hitor: all comparator outputs of one column in an OR-chain (asynchronous)
- PTD: precision timing better than Timestamp (47 ns)
- Sampling: 2.95 ns period (169.7 MHz DDR)
- Power hungry feature: disabled in iVTX
- Little overhead when disbaled (Little die space, clock can be turned off)
- Resolution limited by timewalk and PVT (process, voltage, temperature) variation
- Calibration necessary



TJ-Monopix2 Measurement

PTD: Performance and Power



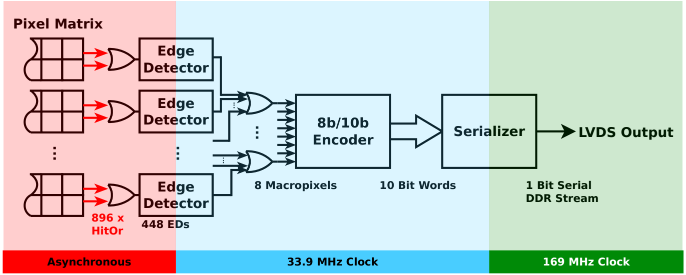


- Suitable for outer Layers
- Power consumption of digital periphery increases when PTD enabled
- At least one PTD annotation per track necessary

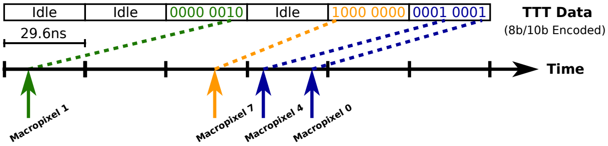
⇨ Very low probability that all three oVTX layer miss the PTD annotation

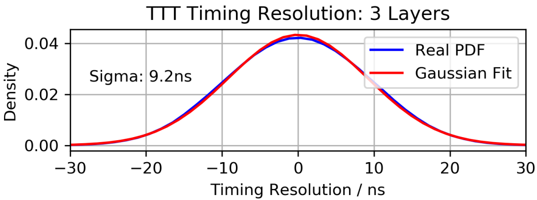
⇨ All timing info we get makes tracking easier

Track Trigger Transmission



- Independent from normal readout
- Whole matrix grouped in 2 to 8 Macropixels
- Time binning: 29.6 ns
- Simple, high throughput transmission





- The OBELIX chip is based on TJ-Monopix2
- Additional features in OBELIX (all on-chip):
    - Voltage regulators
    - ADC and temperature sensors
    - Trigger logic
    - Precision timing module
    - Fast transmission for trigger contribution
- Development and verification is entering final stage
- Aiming submission fall 2024

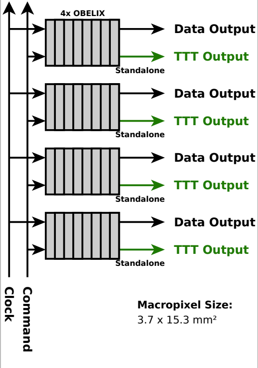
DESY TB Crew Summer 2023

OBELIX Designers Meeting Fall 2023

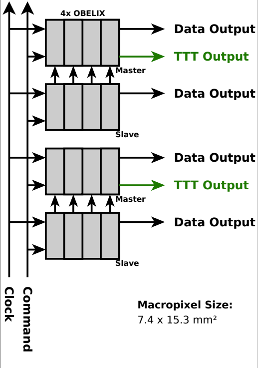
Backup slides

TTT: Configuration and Performance

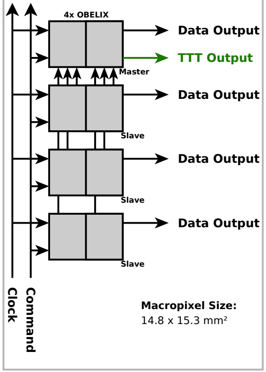
8 Macropixel Configuration

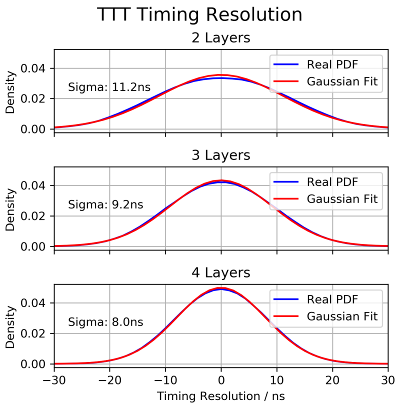


4 Macropixel Configuration



2 Macropixel Configuration





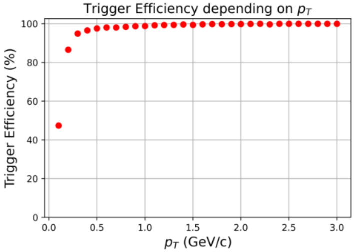
- Different Layers in VTX need different resolution: Can save wireing
- Physics simulation pending

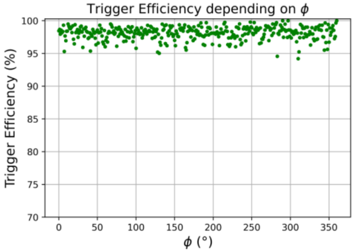
- Timing resolution limited by HitOr delay (45 ns max)
- Averages out with multiple layers
- Baseline: 3 oVTX layers use TTT

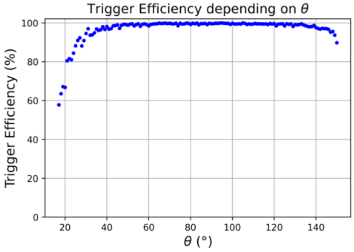
TTT: Efficiency in VTX

Average efficiency = 98.1 ± 1 %

- Trigger Efficiency with respect to :
  - Transverse Momentum
  - Angle ϕ
  - Angle θ

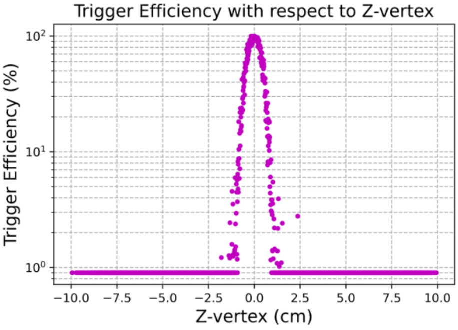




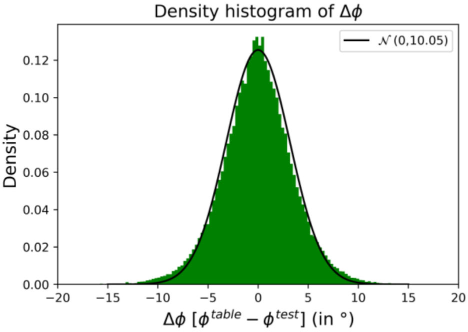


Z-vertex Acceptance and Φ Accuracy

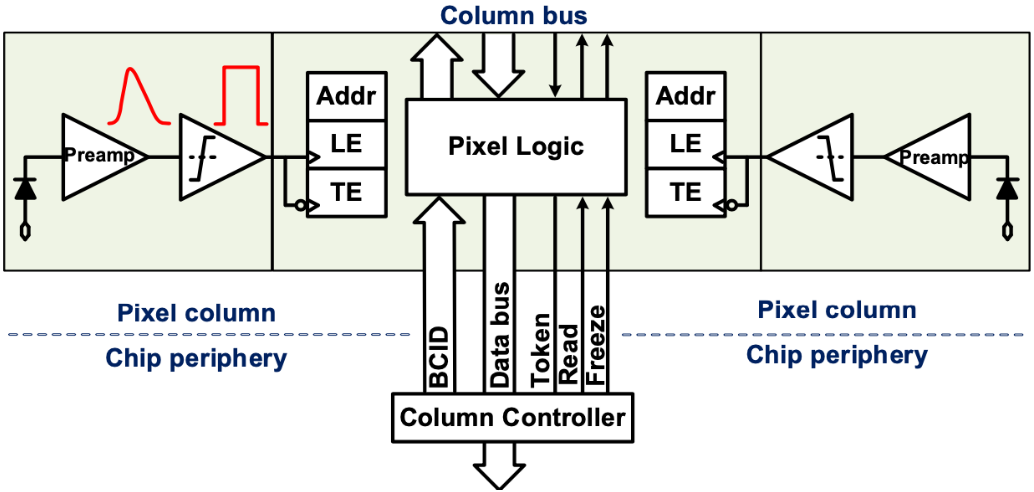
Z-vertex Acceptance : |z| < 2.5 cm



ϕ Accuracy : Gaussian σ = 3.17°



Column Drain Readout



OBELIX Key Requirements

1. High hit efficiency at demanding hitrates with sufficient timesamping
   →
   - Matrix inherited from TJ-Monopix2
   - See CMOS Talk from Lars Schall

2. Handling trigger latency of the Belle II experiment (up to 10 μs)
   →
   - New implementation of digital periphery
   - Simulation to validate performance

3. Power dissipation:
   - air cooling of inner layers
   - liquid cooling of outer layers

   →
   - Optimized digital logic with optional features

4. Little space for cables inside detector
   →
   - On chip voltage regulators
   - 2 LVDS downlinks for groups of chips (Rx)
   - 1 or 2 LVDS uplink(s) per chip (Tx)

OBELIX Optional Features

5. Incresed timing resolution at expense of power
   →
   - Precision timing module in periphery (PTD)
   - Offline timing annotation

6. Contribution to Belle II Trigger
   →
   - Independent fast data path
   - Fast coarse hit transmission

These features require significant power:

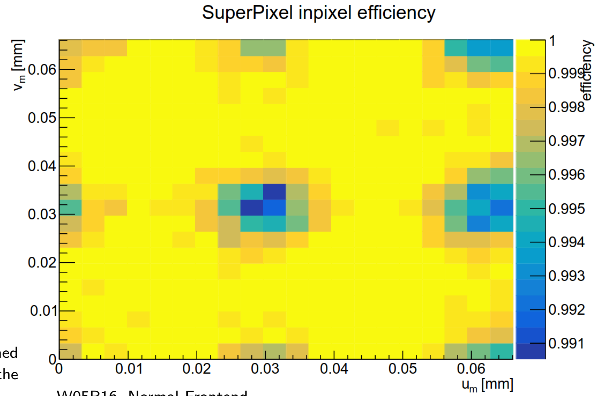
Only switched on for liquid cooled layers L3 to L5

VTX Testbeam at DESY Summer 2023

- First week: Regular measurements with telescope (efficiency and angular scans for depletion)
- Second week: Timing measurements, parasitic to RD50 MPW3 Testbeam
- Beamtelescope with Alpide chips (Duranta)
- Spatial Resolution $< 10\,\mu m$ for all chips

Chip SN	Irradiation	Substrate
W02R05	None	Epi
W05R16	p^+, 5×10^{14} n_{eq}	Epi
W08R19	None	Epi
W14R12	None	Cz

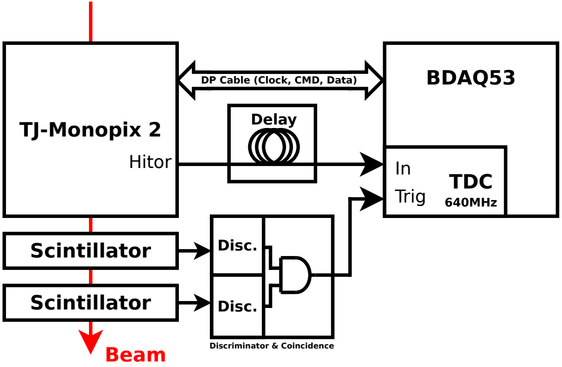
Chip SN	Frontend	Efficiency
W05R16	Normal	0.9999
	Normal Cascode	0.9979
	HV Cascode	0.9913
	HV	0.9811



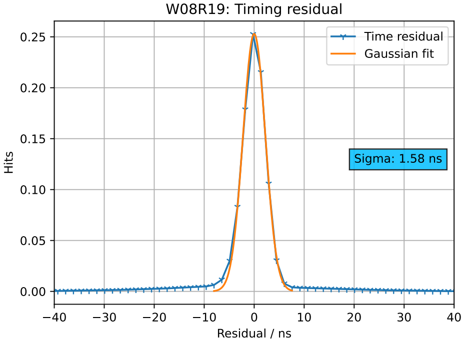
W05R16, Normal Frontend

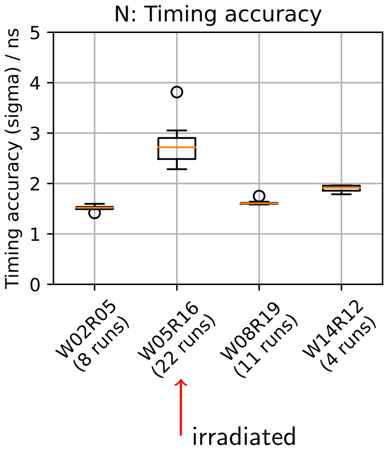
The measurements leading to these and following results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

Timing Measurement Setup



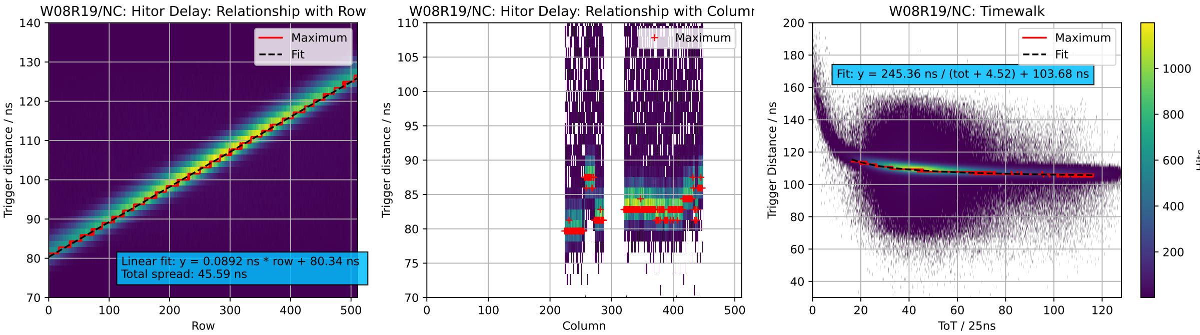
- TDC module of BDAQ53 firmware measures delay between scintillator and Hitor
- TDC words inserted into data stream
- TDC data is matched to hits offline
- Whole chip has one Hitor line: ambiguities arise
- ToT is measured by both, TJ-Monopix2 and TDC module
- Therefore used to match and cut (± 25 ns cut)





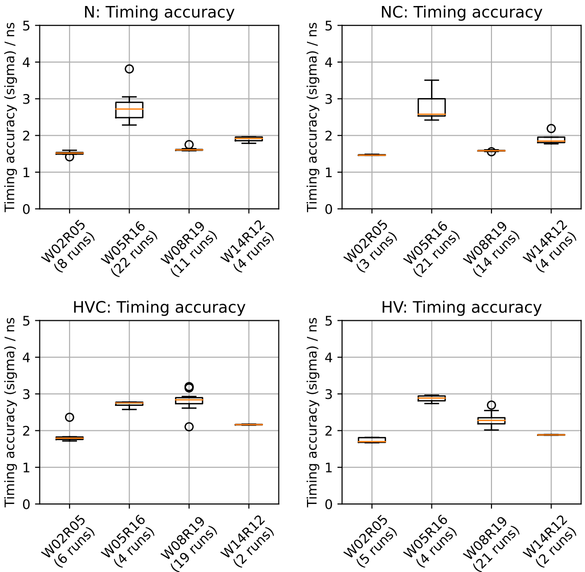
- Three corrections applied:
  - Column delay (Hitor)
  - Row delay (Hitor)
  - Timewalk
- Tail in distribution: wrong associations
- Resolution: < 2 ns (unirradiated), < 3 ns (irradiated W05R16)

Timing Corrections



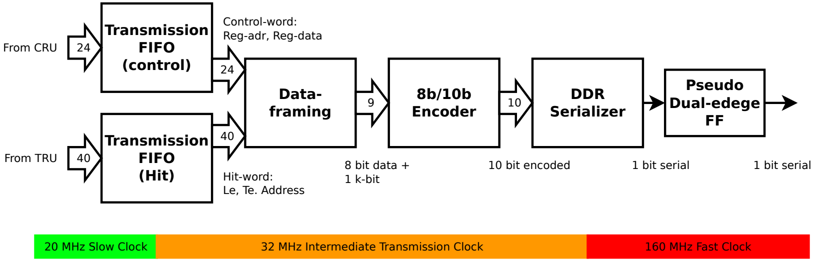
- Iterative fit
- Halos caused by wrong associations

Timing Accuracy Analysis



- N: Normal Frontend
- NC: Normal Cascode Frontend
- HV: High Voltage Frontend
- HVC: High Voltage Cascode Frontend

Transmission Unit (TXU)



- Most TXU components run at 32 MHz (160 MHz/5) intermediate clock
- Serializer needs one byte (10 bit encoded, DDR) per 32 MHz clock cycle
- This allows simple state machines
- Clock boundary to 20 MHz clock is done via FIFO
- Hits are sent in frames sharing the same leading edge BCID