DRD 7.6a – Common Access to Imaging Technologies

DRD7.6 Conveners: M. Barbero, M. Caselle, I. Sedgwick, W. Snoeys – slides on LF by M. Rolo, INFN

DRD7.6a

DRD7 Collaboration

Main aim: develop electronic systems for future HEP experiments, and provide a platform for this development in a context where these systems become more and more complex and costly

- Approved by the CERN research board on June 5th 2024
- Final proposal document and presentation in DRDC June 3 open session: https://indico.cern.ch/event/1406007/
- Workshop on September 10-11 at CERN

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Strategic Goal

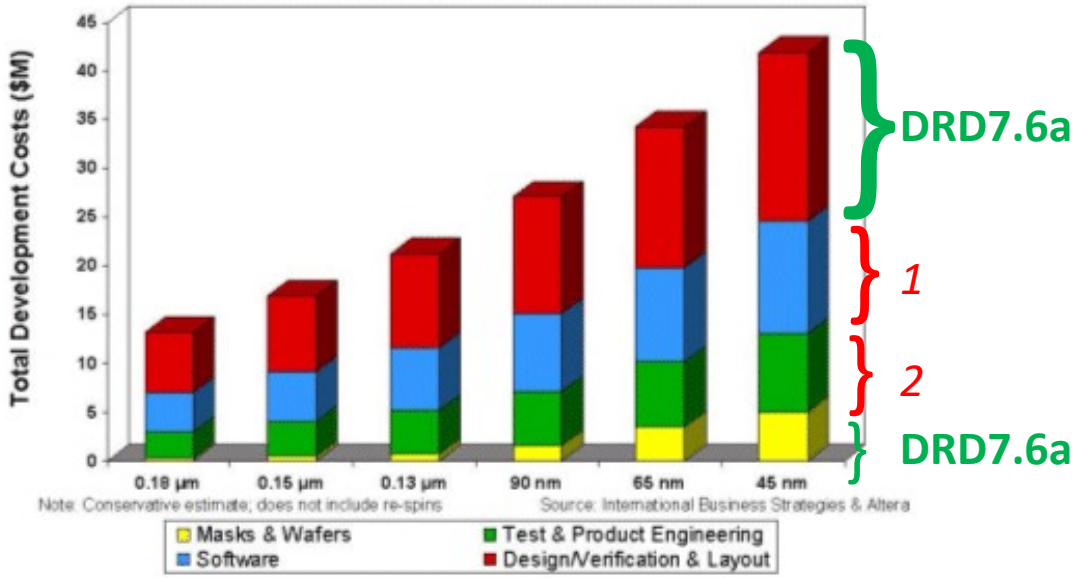
- Provide efficient and affordable access to imaging technologies to projects, DRDs like DRD3, and experiments
- Share and reduce development costs & time
- Requires concentration of resources

Performance Targets

- Shared PDKs, IPs and access to runs
- Chip submissions and test results

Supported Technologies

- TPSCO 65nm
- Tower Semiconductor 180nm
- LFoundry 110nm



https://www.design-reuse.com/articles/12360/fpgas-and-structured-asics-low-risk-soc-for-the-masses.html

Resources for 1: Software & 2: Test setups not included within DRD7.6a

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TPSCo 65nm

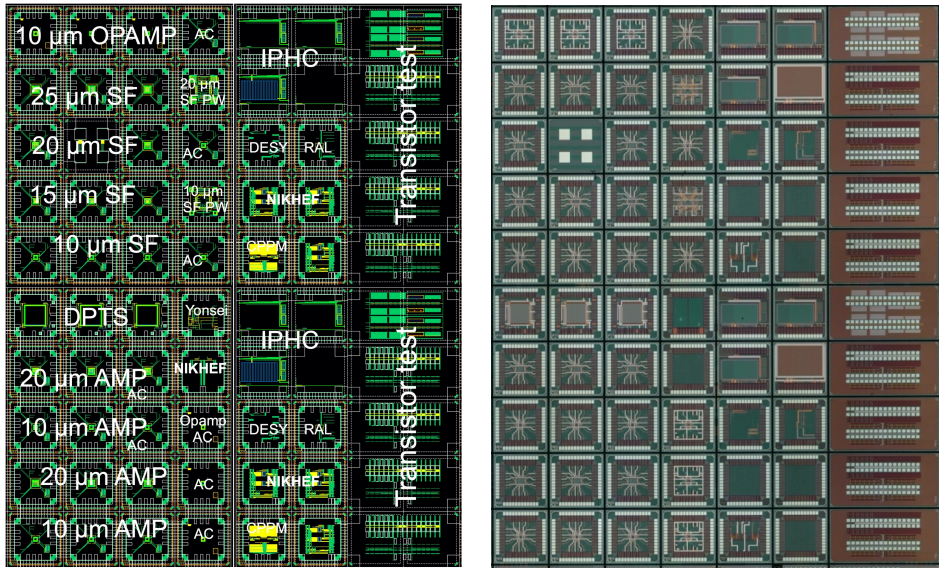
- Currently in use for ALICE ITS3 and EP R&D WP1.2
- Joint runs already carried out – MLR1, ER1
- CERN, IPHC, INFN, NIKHEF, STFC, SLAC, DESY, SLAC, Yonsei…

very significant contribution from ALICE ITS3 (including ~40-50 people test team)

MLR1: *Dec 2020:*

Qualification of TPSCo 65 nm for HEP

1.5 x 1.5 mm^2 test chips



- Fully efficient at RT before and after 10^{15} n_{eq}/cm^2, significant benefit from 180nm experience
- Sensor time resolution ~ 70 ps (10 µm pitch)
- Investigating path to higher irradiation levels and lower input capacitance

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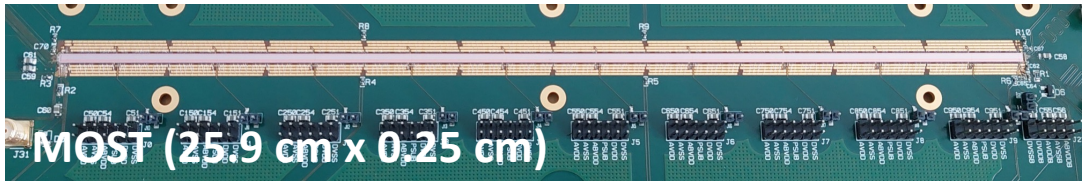
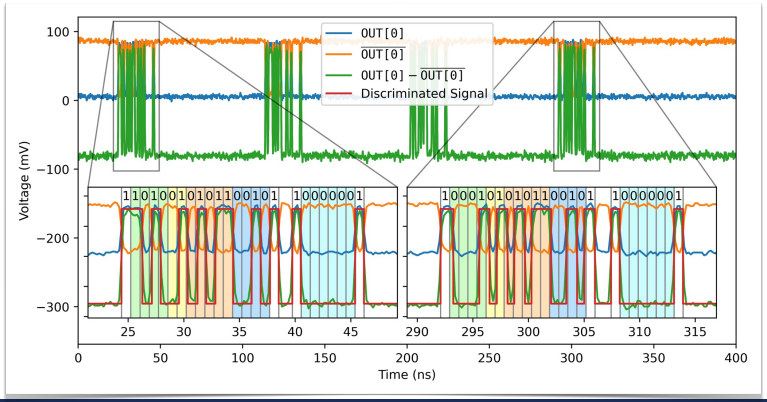
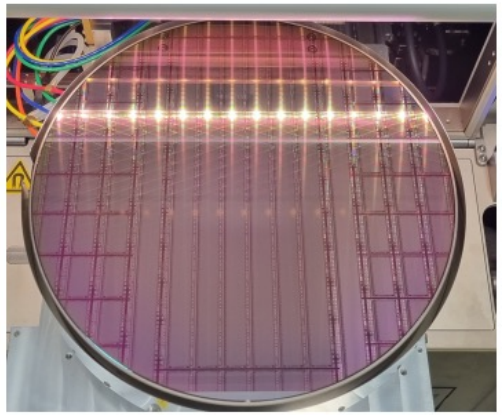
*ER1: Dec 2022: **Learning about stitching***

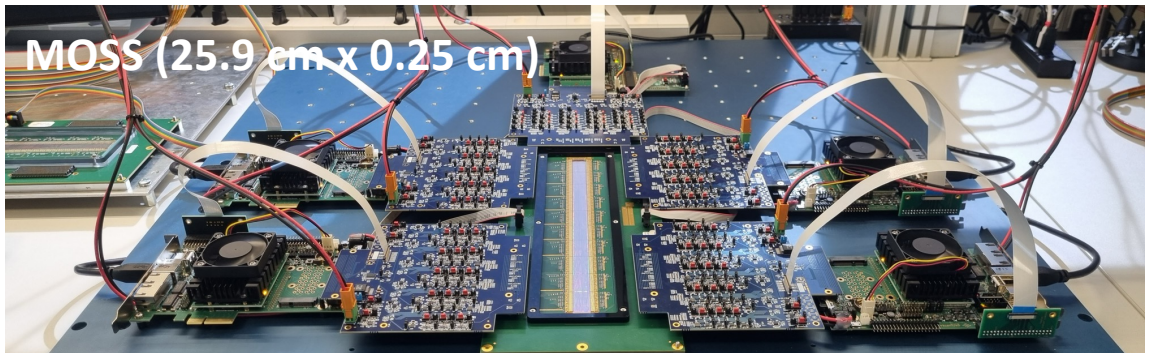
Two stitched sensors with 10 repeated units:
Both functional, learnings to be included in ER2



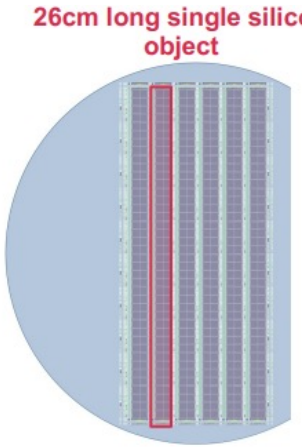
- 18 µm pitch, very densely designed pixel matrix
- Global power distribution + conservatively designed highly granular power switches to switch off faulty parts
- Asynchronous, hit-driven readout, low power consumption + timing information

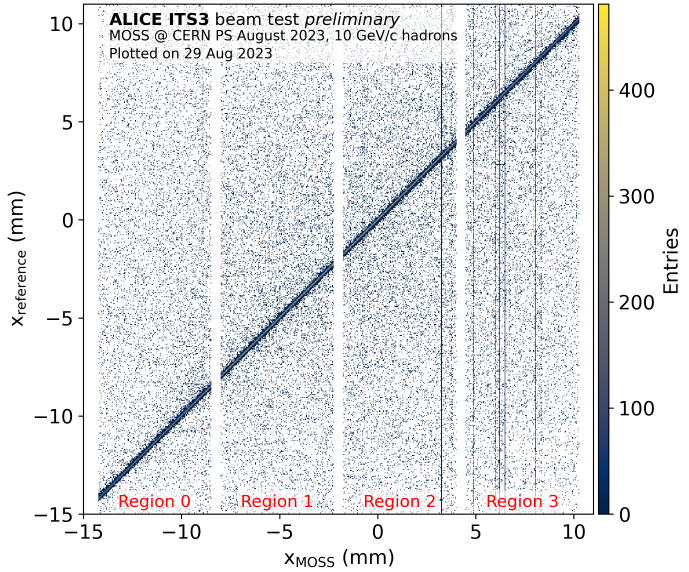






- Top half 22.5 µm pitch, bottom half 18 µm pitch
- Each half powered completely independently with 4 conservatively designed submatrices -> many power domains
- Synchronous readout





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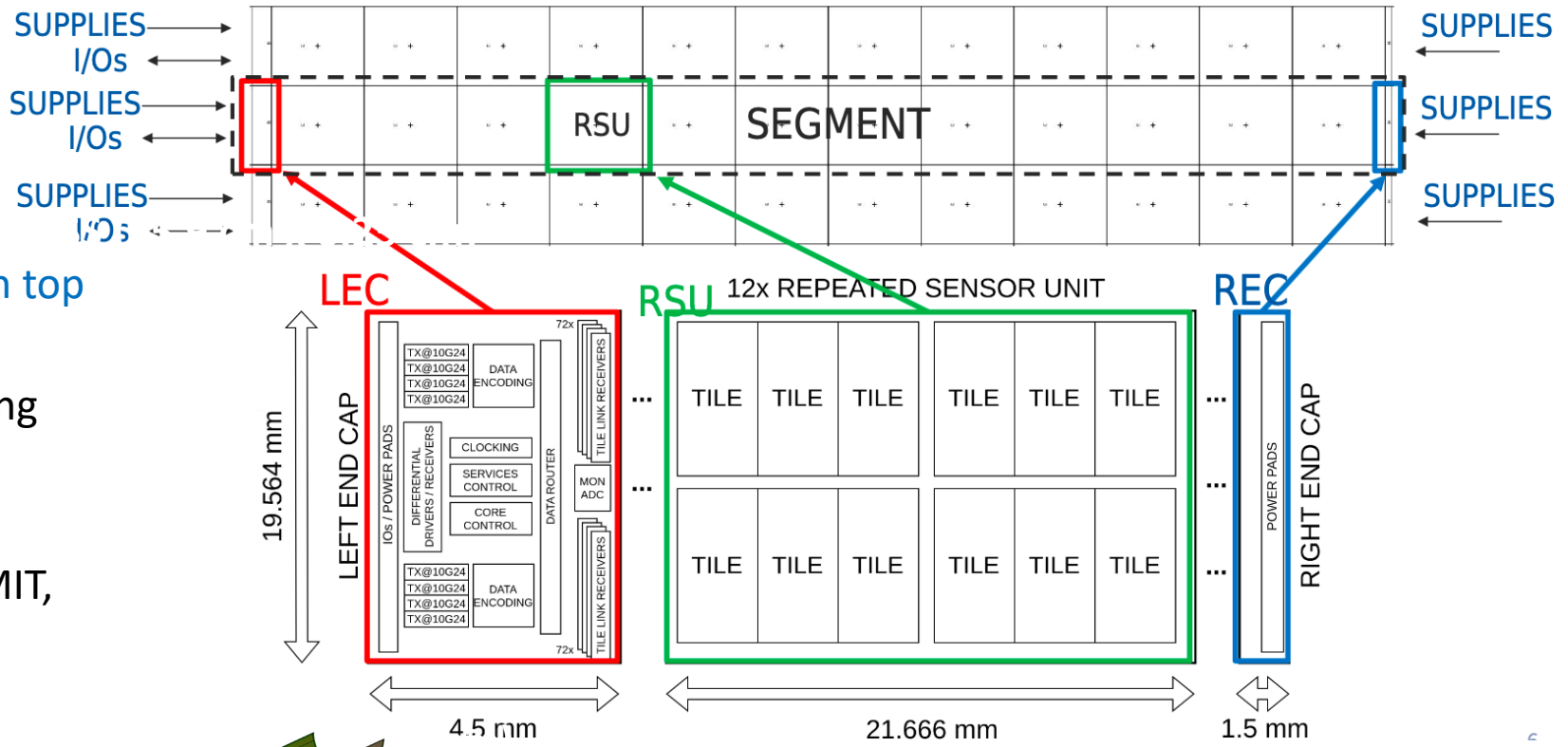
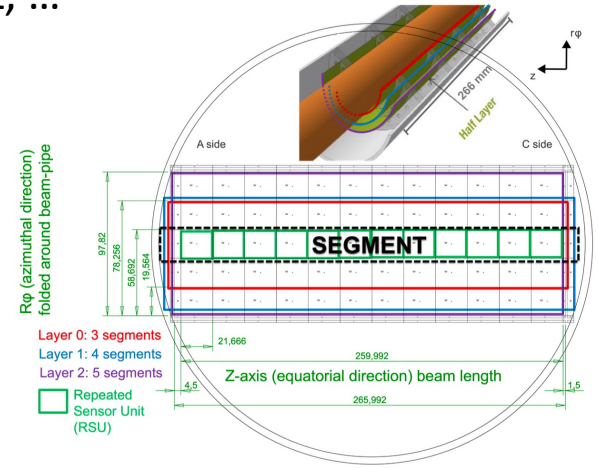
ER2: MOSAIX: Fall 2024:

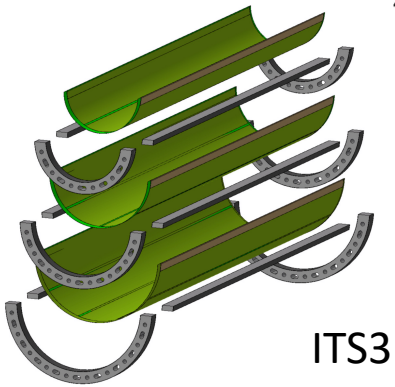
First full prototype for ALICE ITS3

Wafer-scale stitched sensor for inner 3 layers

- Initial study and specification complete, finalizing first version of the chip, digital on top design flow
- To do: port to the new metal stack, finalizing last blocks (target July), verification
- Goal is submission in the fall 2024
- Collective effort: CERN, BNL, INFN, IPHC, MIT, Nikheff, RAL, …







ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

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TPSCo 65 nm

- CERN engages to do the support and interface to the foundry
- Common Multi Project Runs (MPRs) foreseen ~Q4 2025 or early 2026 (MPR2), 2027 (MPR3), … with financial support at 50 % (excluding wafer stacking)
- Significant effort towards TPSCo design framework:
  - TPSCo offers Physical Design Kit (PDK) for analog designs, Digital Design Kit (DDK) for digital designs, IP (standard & I/O cells, SRAM/ROM compilers, eFuses)
  - CERN developed custom DRC rules, an RTL to GDS flow, more automated reticle assembly and sign-off (P. Leitao)
  - To be made available for MPRs, but early version accessible now
- Some IPs already developed in collaborative effort, including digital library for Design For Manufacturing. More are needed, with preparation for shared use.

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TPSCo 65 nm RTL to GDS flow consists of:

- Template scripts for digital on top implementation (using Cadence flowkit)
  Bookkeeping of tech and design files (tmake tool, https://cern.ch/tmake)
- Possibility to triplicate the design using the TMRG tool (https://cern.ch/tmrg)
- Versioning of Open-Access library via ClioSoft SOS
- Power analysis signoff
- Single Event Effect simulations for radiation hard designs
- Documentation

GOAL: empower the user with a workflow capable of rapid digital design prototyping, guiding the user from start to finish

Support to be deployed through CERN-ASIC-Support framework

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Tower Semiconductor 180nm

- >10 years of experience in the community
- Used for:
  - ALPIDE in ALICE ITS2 (10m^2), taking data in the experiment
  - for STREAM, Belle II, GSI… (see presentations earlier today)
- CERN has been interface to the foundry and carried out the support so far,
  intends to concentrate on TPSCo 65 nm
  for 180 nm discussions for help with IPHC and foundry
- Custom DRC rules
- Several IPs developed, need preparation for shared use
- Common runs to be scheduled, could be foreseen in 2025, 2026 and 2028.

Lfoundry LF11is 110nm technology features

- automotive-grade CMOS Image Sensor node
- 1.2V core and 3.3V IO devices
- 6 Aluminum BEOL stack and MiM capacitors
- MPW runs, MLM (Multi Layer Mask) and Full maskset SPW runs with a pilot lot starting 25 wafers
- 1D and 2D stitching options
- Development of LGADs
- use of custom high-resistivity substrates on FSI and/or BSI process flows, including hence the possibility to use a dedicated maskset for backside lithography on thick substrates.

Lfoundry LF11is 110nm FD-MAPS technology

- Sensor technology developed by INFN and LFoundry
- Extensively used in the framework of the INFN project ARCADIA
- Several INFN groups involved on ongoing and future activities employing the LF11is FDMAPS technology, working on sensor technology, CMOS IP design and chip integration, data acquisition systems and characterisation: Torino, Trento, Padova, Milano, Bologna, Perugia, Pavia and Pisa. The ARCADIA budget of ≈ 1.5 MCHF covered so far the cost of 3 full-maskset engineering runs (ER) and hardware for DAQ systems.
- Joint runs (INFN, PSI) so far on – ARCADIA ER-1, ER-2, ER-3 (50 wafers), ER-4 (12 wafers to be started), **support for future runs provided by INFN**
- More information: DRD7 workshop 25-26 September 2023: https://indico.cern.ch/event/1318635/

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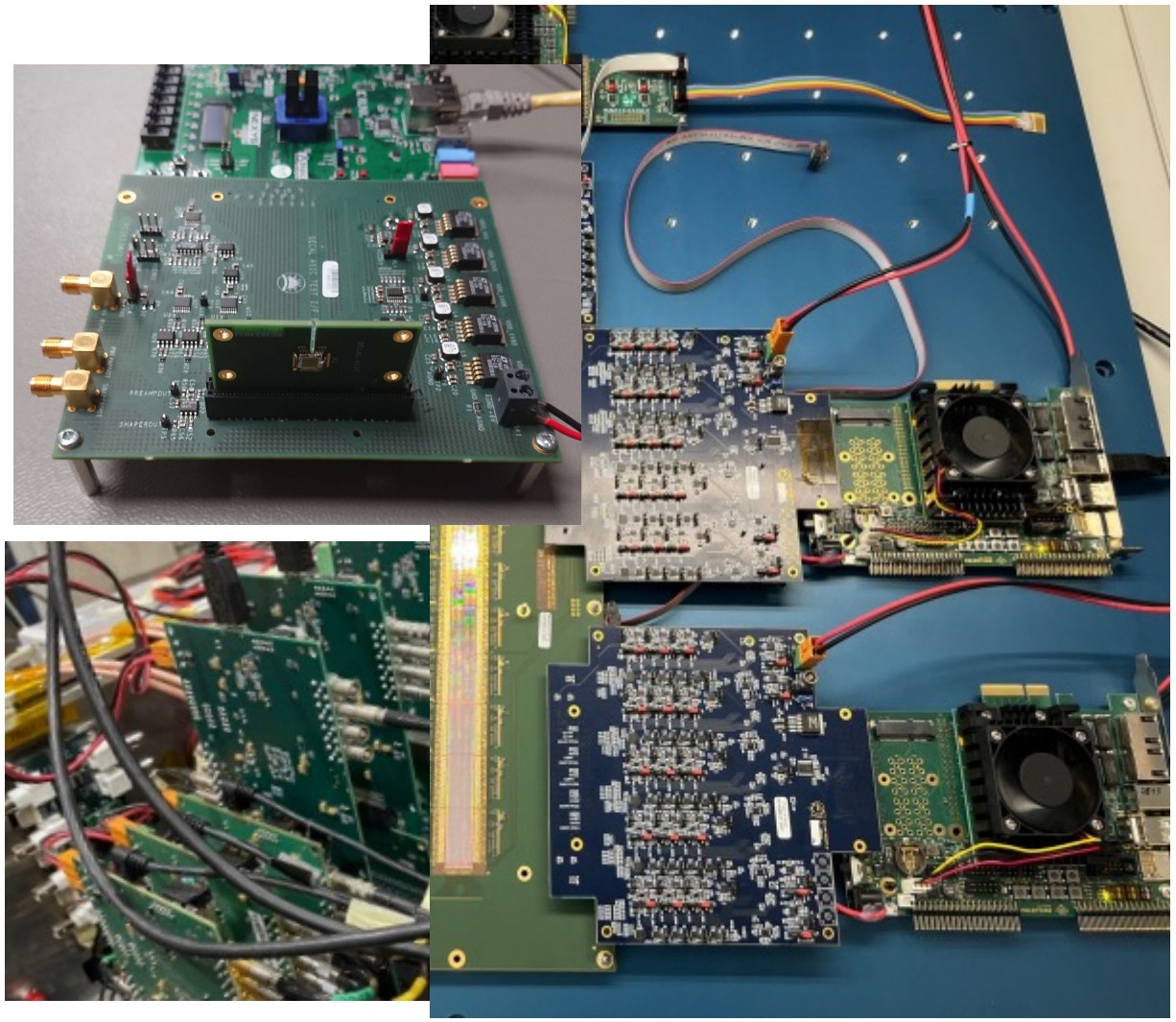
Shared Standardized Test Systems

- Desire to reduce duplication and development time of many test systems
- Render their support manageable (at present usually not sustainable)
- Standardise on chip interfaces
- Originally proposed as DRD7.6c
- Much interest, but no driving institute came forward
- If interested please get in touch – could include in future DRD7 calls



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- Institutes: *CERN, INFN, IN2P3 (CPPM, IPHC …), NIKHEF, NORWAY (UiB,UiO,USN), STFC, US DOE (SLAC…).*

- About 20 FTE and 400 kEuro/y available, mostly on TPSCo 65 ISC and LF110IS
- At least 6 FTE to be requested

- Additional resources for the runs to be financed by the participants in the run

- 3D stacking at the foundry not yet financed.

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Conclusions and outlook

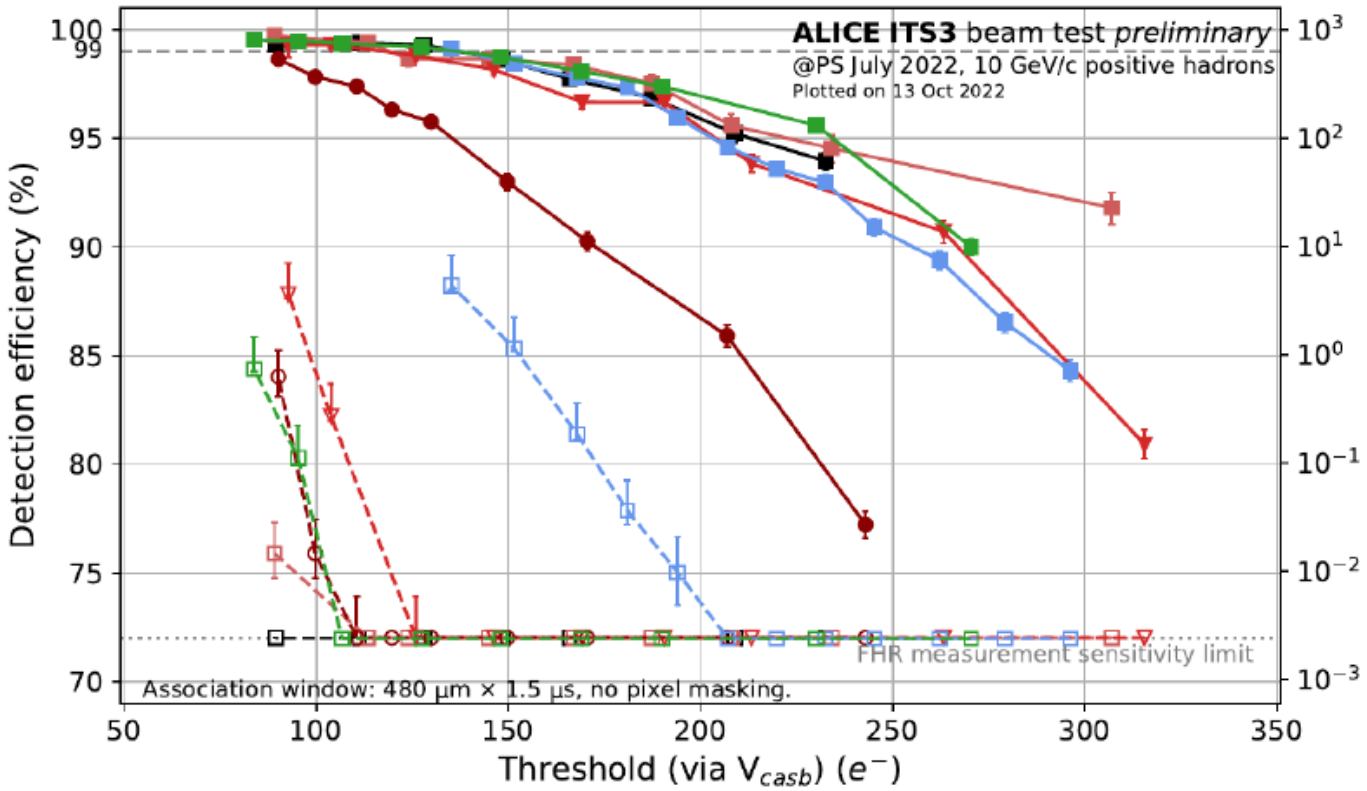
- Main aim: facilitate common access to selected imaging technologies (TPSCo 65nm ISC, Tower 180nm IS and LF110nm IS for projects, DRDs like DRD3, and experiments, to share and reduce cost and effort by concentrating resources, and to address the increased complexity of large chips. This includes:
    - *Interface to the foundry*
    - *Organization of shared runs*
    - *Development of shared design kits, automated design flows, etc., and IPs*
    - *Organize their support for the community*
- Shared test systems not (yet?) included
- In-foundry 3D stacking not yet financed, DRD7.6b proposes some mainly in-house 2.5 and 3D integration (contact M. Caselle)

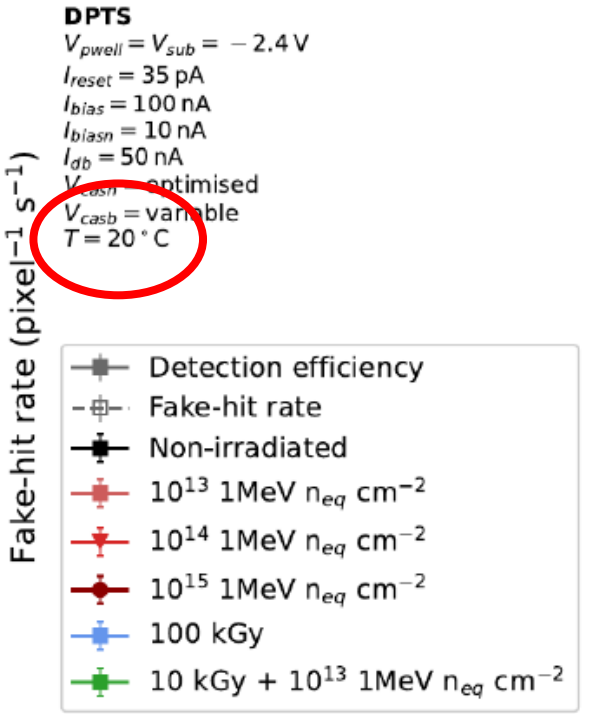
Questions?

Backup

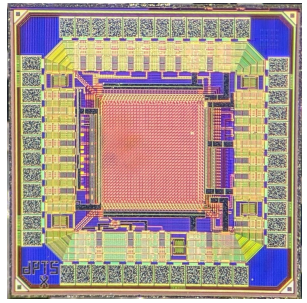
doi: 10.1016/j.nima.2023.168589

TPSCo 65nm : qualified for HEP (synergy between ALICE ITS3 and WP1.2)





DPTS



15 x 15 µm^2 pixel

- Fully efficient after 10^{15} 1MeV n_{eq} cm^{-2}… at room temperature
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- Many features not yet explored (wafer stacking, special imaging devices…)

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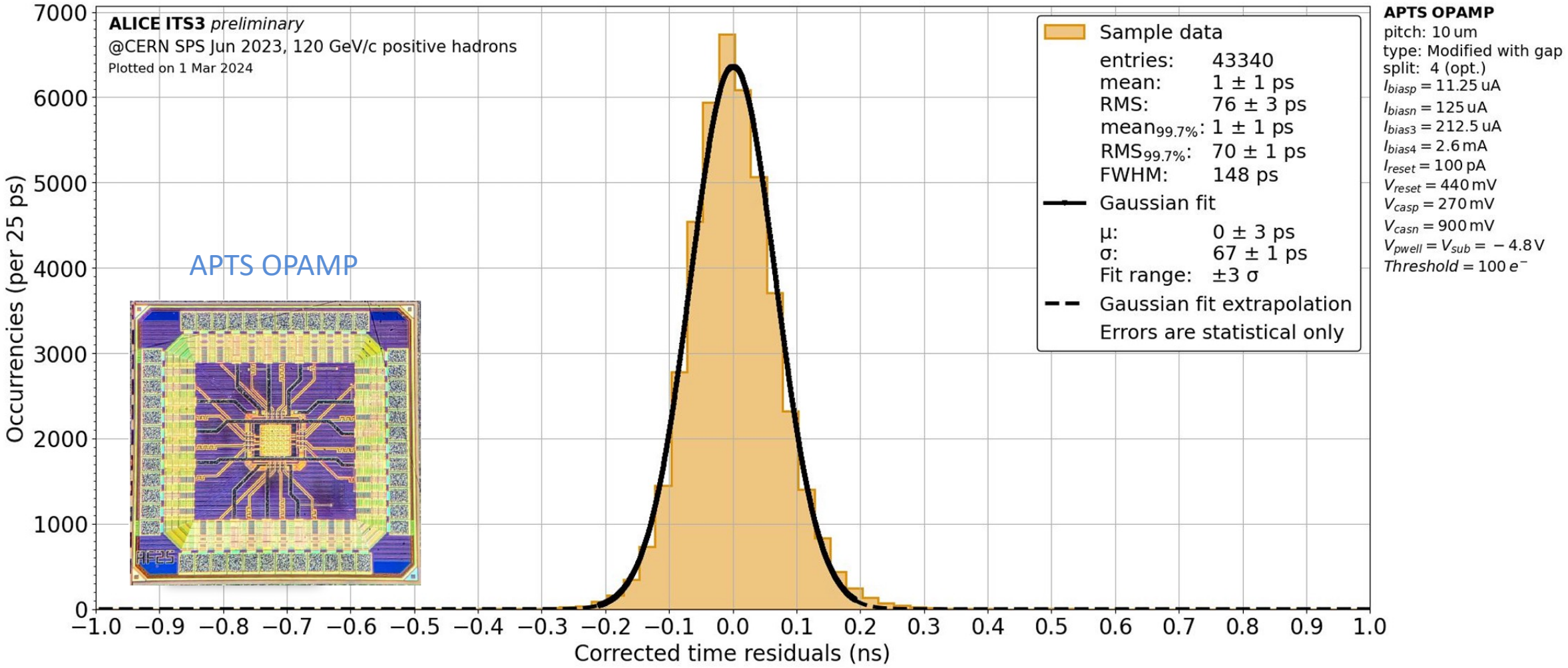

Bong-Hwi, U. Savino et al. ULITIMA 2023, L. Aglietta, 16th Pisa conference on advanced detectors.
(180nm FASTPIX ~100 ps with time walk and cluster size correction, J. Braach et al. https://doi.org/10.1016/j.nima.2023.168641)