Development of MAPS using 55nm HVCMOS Process for future tracking detectors

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On behalf of the COFFEE development team

- *IHEP, CAS, Beijing*
- *KIT, Karlsruhe*
- *Hunan U., Changsha*
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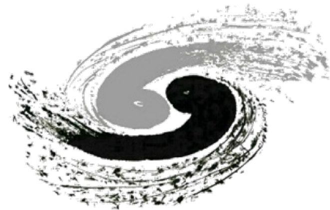
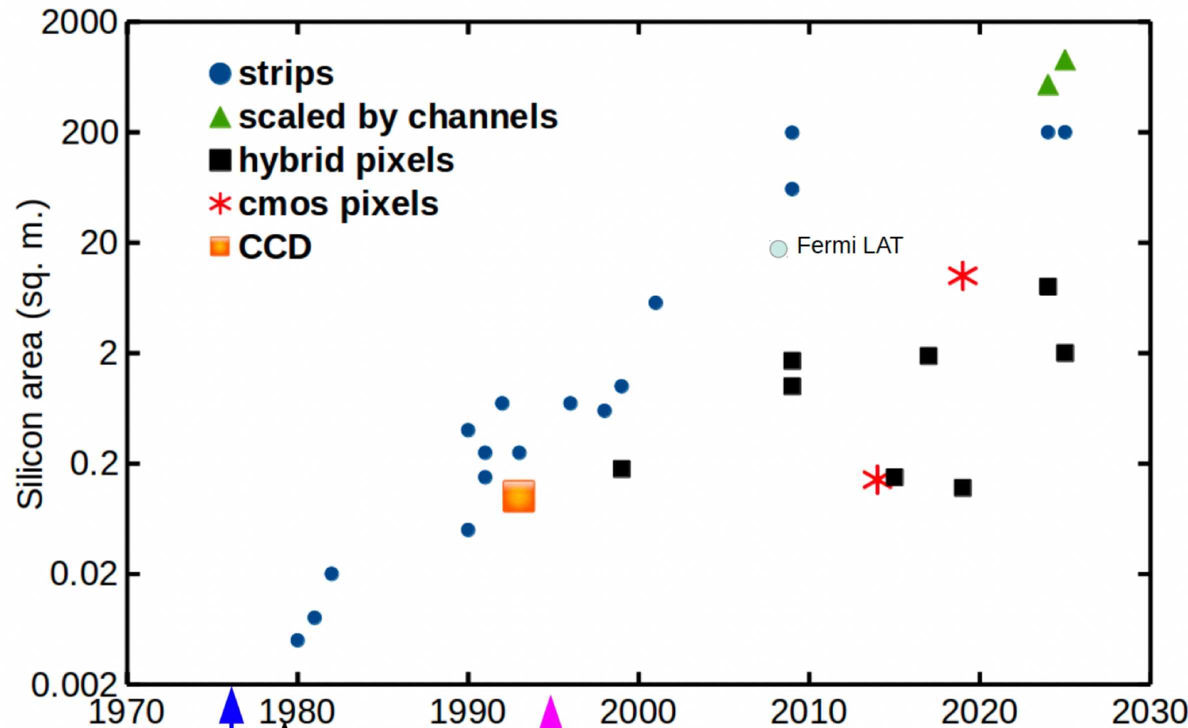
- *Shandong U., Qingdao*
- *CCNU, Wuhan*
- *NWPU, Xi'an*
- *DMU, Dalian*



1st DRD3 week on Solid State Detectors R&D
17 Jun 2024

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

Semiconductor tracking detectors in HEP: getting larger



Year of first data taking

First CCD digital cameras

Start of HEP IC design

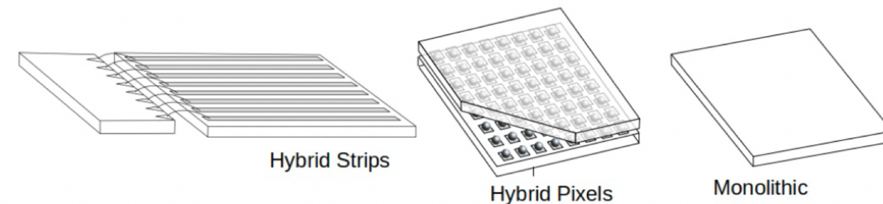
CMOS sensors used in webcams

Strip Detectors	
1980	NA1
1981	NA11
1982	NA14
1990	MarkII
1990	DELPHI
1991	ALEPH
1991	OPAL
1992	CDF SVX
1993	L3
1996	CDF SVX'
1998	CLEO III
1999	BaBar
2001	CDF SVXII+ISL
2009	ATLAS SCT
2009	CMS tracker
2025	ATLAS ITK
2025	CMS upgrade

Hybrid Pixels	
1999	Delphi
2009	ATLAS
2009	CMS
2015	ATLAS IBL
2017	CMS
2019	velopix
2025	ATLAS
2025	CMS

CMOS Pixels	
2014	STAR
2019	ALICE

CCDs	
1993	VXD



M. Garcia-Sciveres @ HSTD13, Dec 2023

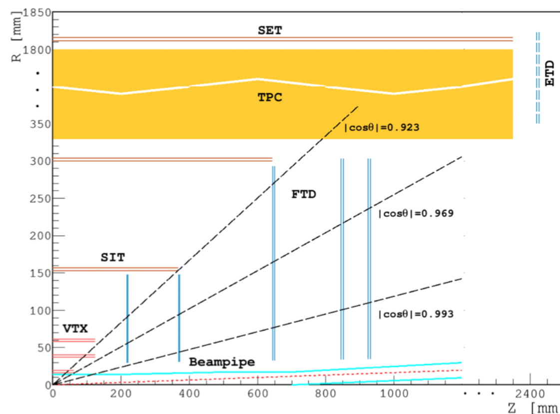
CEPC silicon tracker

- Large area silicon tracker planned
  - ~70 – 140 m² depending on detector concept
- Good spatial resolution
  - ~10 um resolution imposed by requirement on momentum resolution

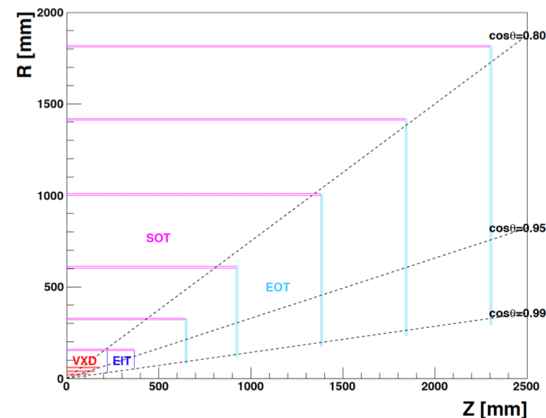
$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$a \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$

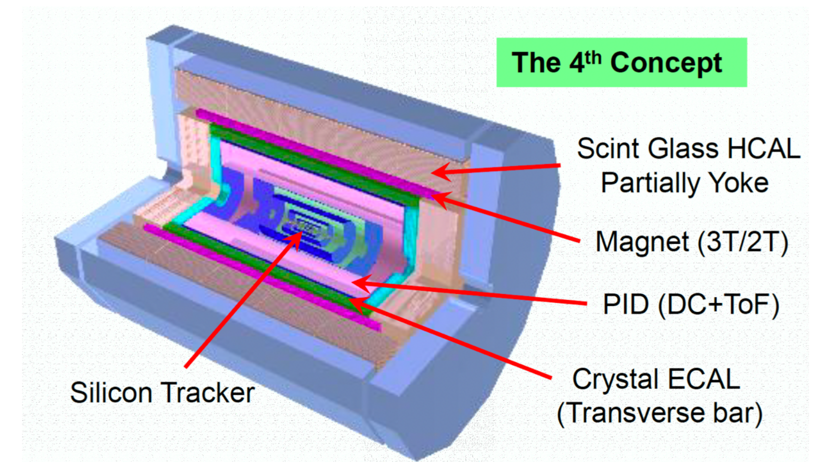
$b \sim 1 \times 10^{-3}$



Baseline concept

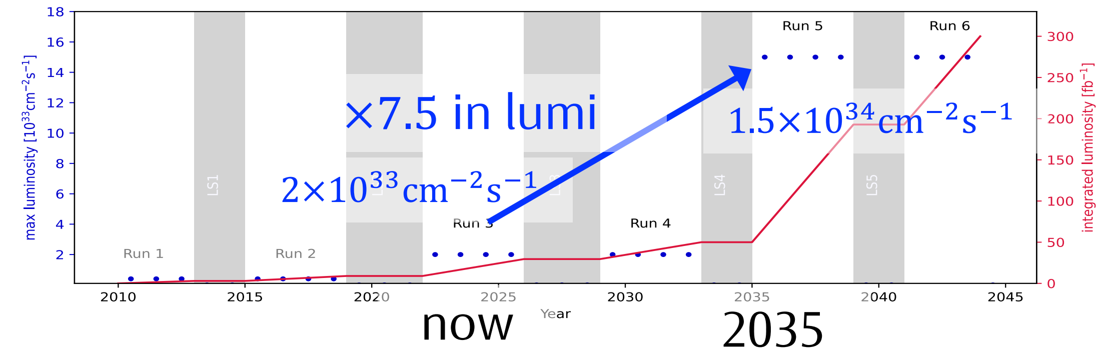


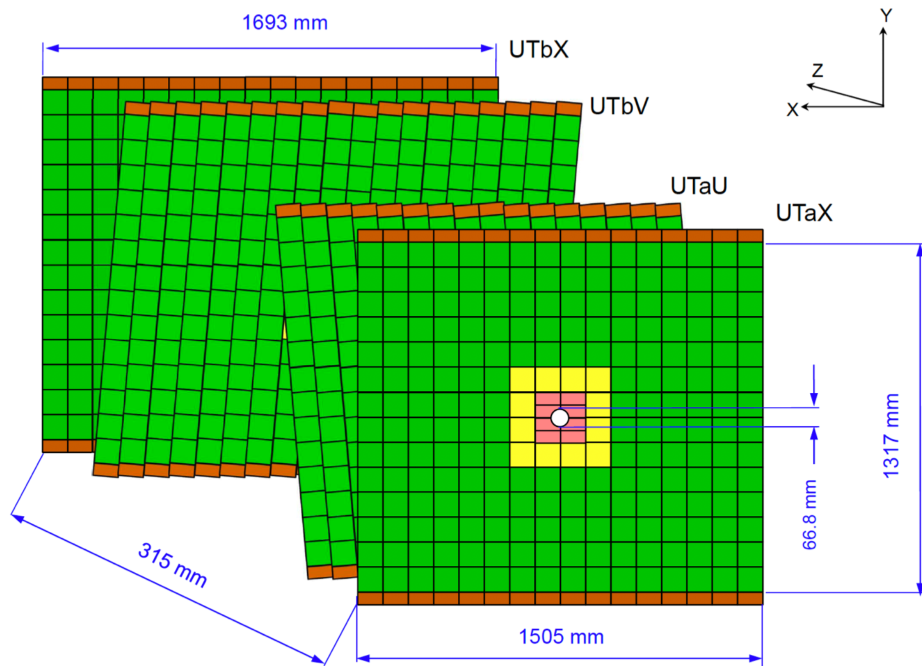
Full Silicon Tracker

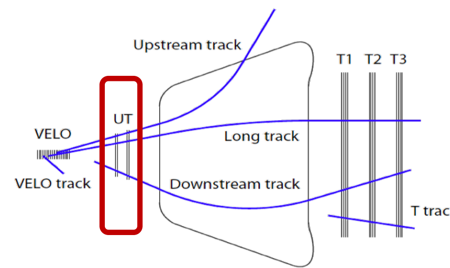


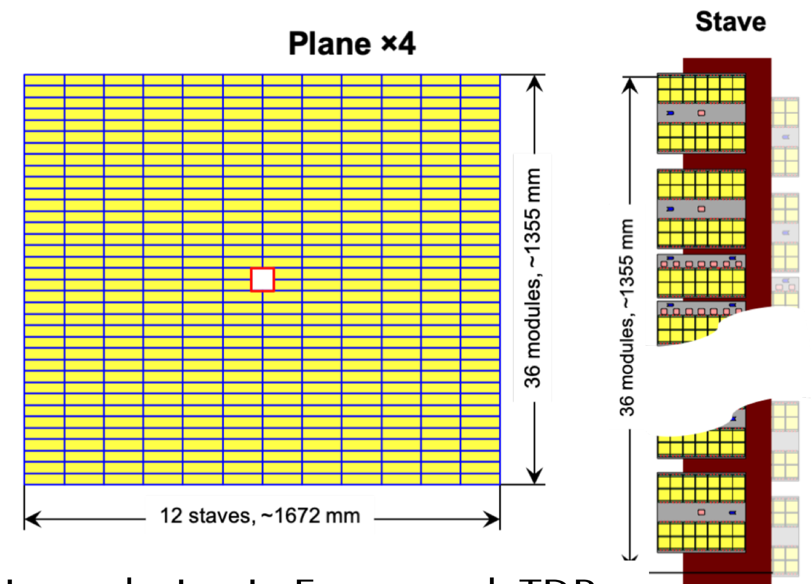
Upstream Tracker in LHCb Upgrade II

- LHCb Upgrade II planned in LS4 to enable luminosity increase by a factor of 7.5
- Silicon-strip-based Upstream Tracker will be replaced with a pixel detector with higher granularity and better radiation hardness
- HVCMOS is a promising technology option









Preliminary design in Framework TDR based on ATLASPix-like sensors

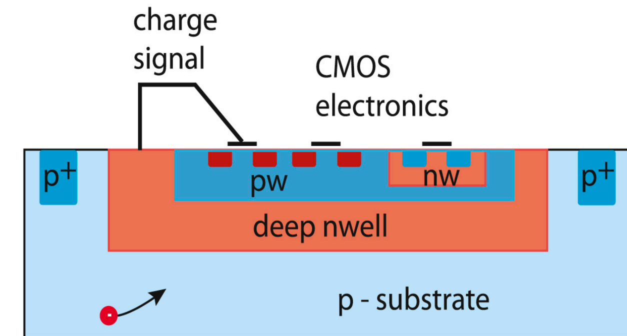
R&D goals

Parameter	CEPC tracker requirement	LHCb U2UT requirement
Pixel size	25 µm × 150µm (< 10 µm spatial resolution)	50 µm × 150µm
Timing resolution	<~ 10ns @ Z pole	<~ 5ns
Power consumption	< 150 mW/cm^2 The lower the better	< 150 mW/cm^2
Radiation tolerance	TBD (<< LHCb)	3×10^{15} n_{eq}/cm^2, 240 MRad
Readout speed	TBD (<< LHCb)	9 Gbps, compatible with lpGBT

HVCMOS as a promising technology

Chip	Pixel size [μm²]	Array size	Noise [e-]	Power density [mW/cm²]	Fluence [n_{eq}/cm²]
ATLASPix (AMS/TSI 180 nm)					
ATLASPix1	60 × 50	56 × 320	~200	170	1×10^{15}
ATLASPix3	50 × 150	372 × 132	~60	~150	1.5×10^{15}
MuPix10	80 × 80	256 × 250	75	190	
LF-Monopix (LFoundry 150 nm)					
LF-Monopix1	50 × 250	129 × 36	~200	~288	10^{15}
LF-Monopix2	50 × 150	340 × 56	~100	~400	
RD50 (LFoundry 150 nm)					
RD50-MPW1	50 × 50	40 × 78			2×10^{15}
RD50-MPW2	60 × 60	8 × 8	~50		2×10^{15}

* An incomplete compilation of HVCMOS sensors

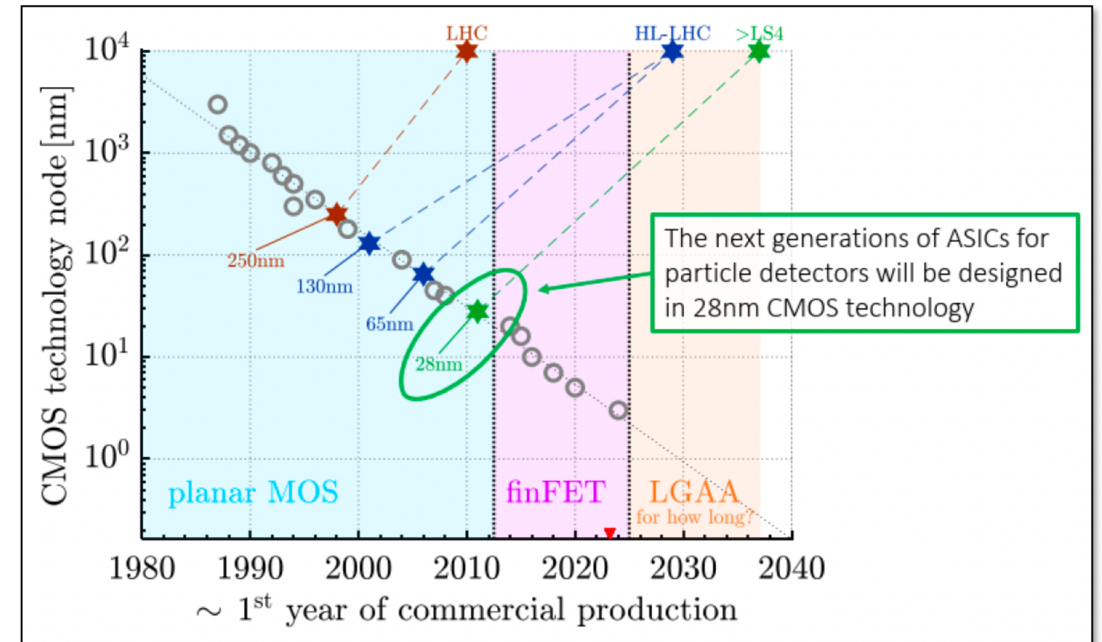


- High-Voltage CMOS
  - Full depletion possible due to large electrode
  - Intrinsically radiation hard
  - Fast charge collection
  - Relatively larger capacitance: noise, power
  - Based on commercially available process without modification -> cost-effective

- HVCMOS chips developed using 180nm or 150nm processes

Towards smaller feature size

- For better performance
  - Higher circuit density
  - More functionality in the same area
  - Less power consumption
- For higher reliability
  - R&D phase of HEP experiments are usually long (comparing to commercial world)
  - Will the process available for mass-production?
  - Example of TSI-180nm process
- Development for 65nm CMOS (in small electrode) has started
  - Key R&D theme in ECFA detector roadmap

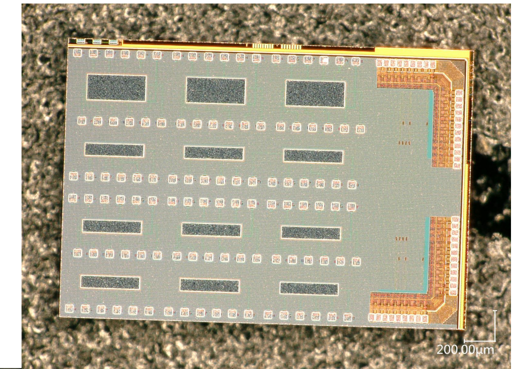


P. Moreira @ CEPC workshop, Oct 2023

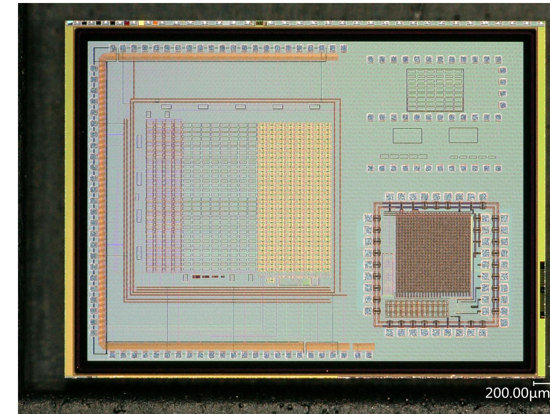
Development in small feature size HVCMOS

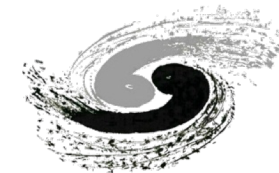
- HLMC 55nm HVCMOS process
  - Cancelled MPW plan in 2022
- SMIC 55nm Low-Leakage process
  - Not HV, yet with a similar deep n-well structure
  - MPW submitted in Oct 2022 in normal wafer
  - COFFEE1 received in Apr 2023
- SMIC 55nm HVCMOS process
  - HVCMOS process, with 1kΩ ·cm wafer
  - MPW submitted in Aug 2023
  - COFFEE2 received in Dec 2023

COFFEE1



COFFEE2





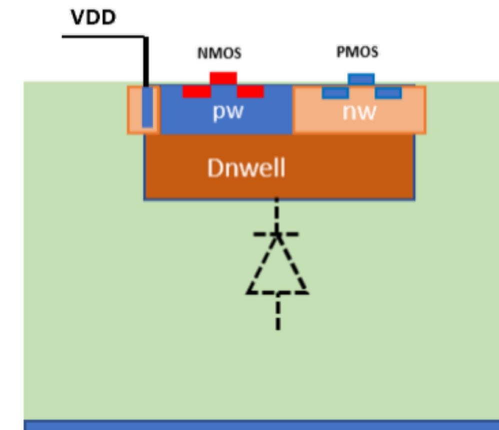
NB: All dimensions mentioned in 55nm process from now on always has a scale factor of 0.9.
As it is scaled down from 65nm masks

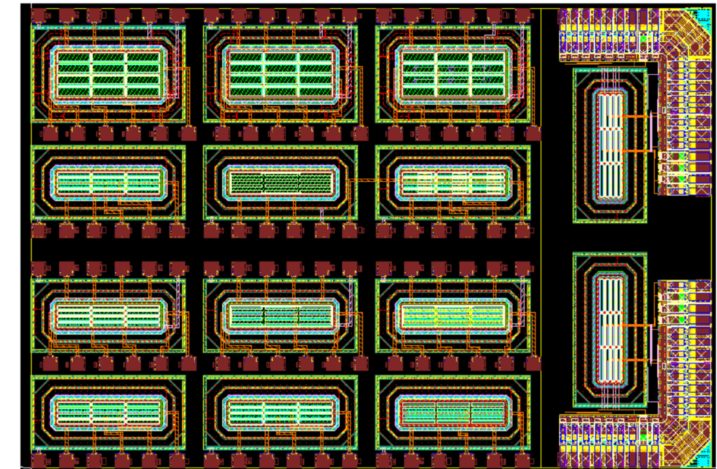
COFFEE1: MPW in LL process

- MPW submitted in Oct 2022 with SMIC 55nm Low Leakage process
  - NB: not an HV process! Yet it has similar deep N well separating the transistors and the sensor part
  - 3 × 2 mm^2 in area
  - Variation of passive diode arrays
  - Simple amplifiers added

- 40 chips received in end Apr 2023
  - Tests going on now

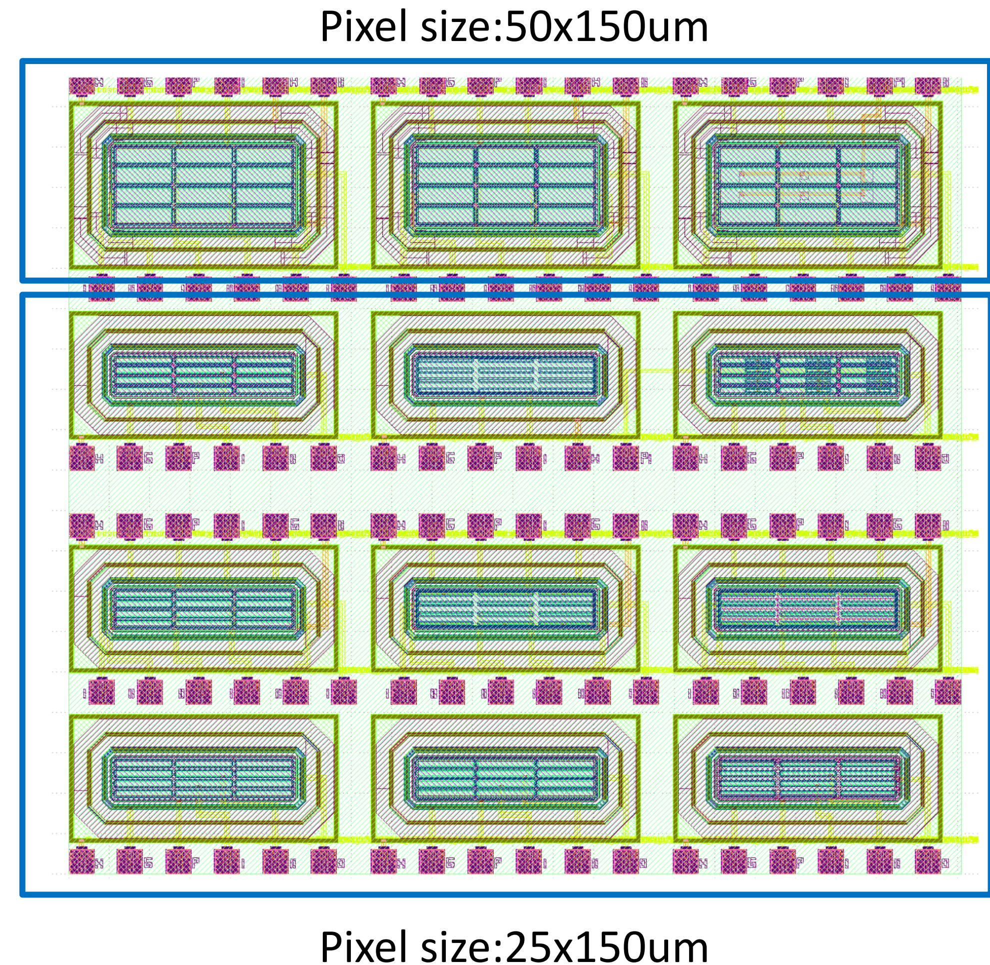
LL process





Passive sensor arrays

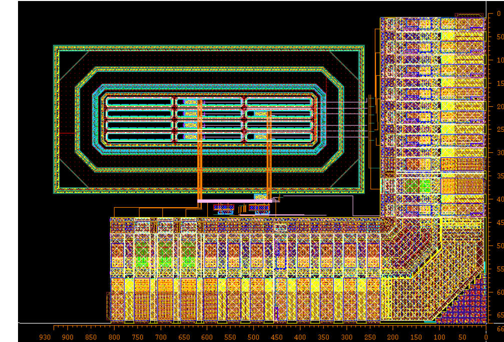
- NB: no HR substrate
  - Limited charge generation
- 12 layout design
- Pixel size：
  - $25x150um^2$, $50x150um^2$
  - Motivated by CEPC/LHCb requirements
- Pixel array： 3x4
  - For charge sharing study
- Different design:
  - With/without P stop between pixels:
  - Space between pixels: 5um, 10um, 15um
  - Connection method
  - Pwell area in Dnwell:
    - Capacitance affect



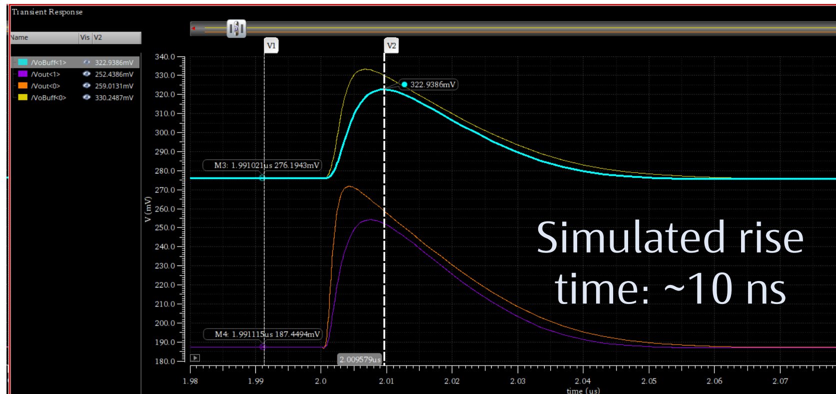
Mei Zhao

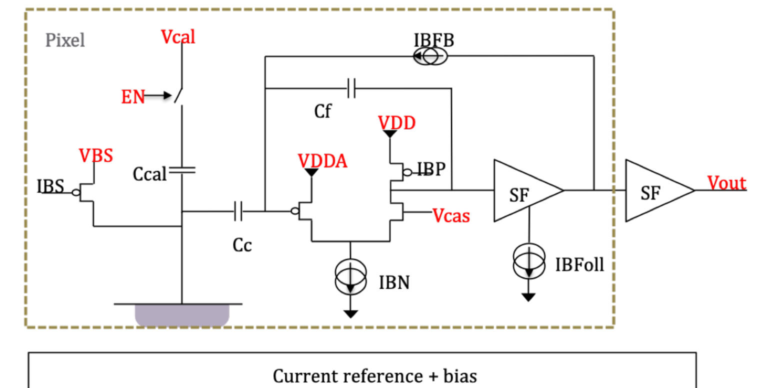
Schematic

- Sensor biased with active resistor
- Calibration capacitor integrated
- Charge Sensitive Amplifier structure
  - Two power supplies
  - Folded cascade amplification stage
  - Constant feedback current
- Two stage source follower used to drive the signal out



6 channels AC coupled to sensors

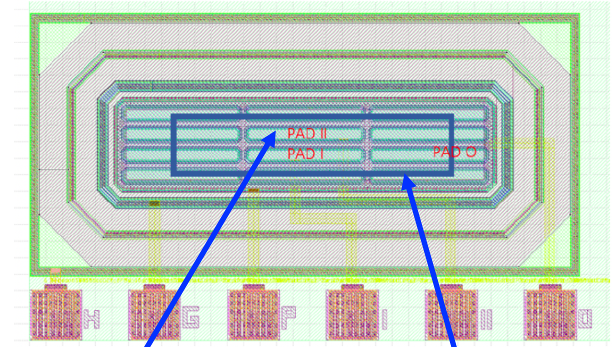




Weiguo Lu

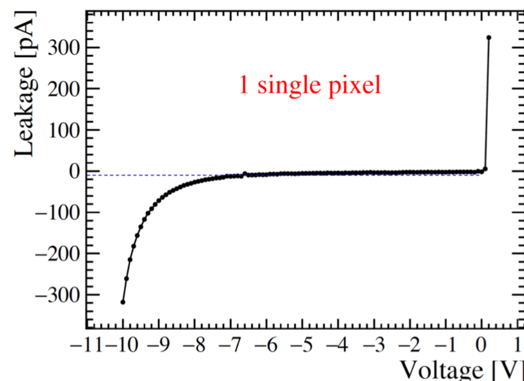
COFFEE1

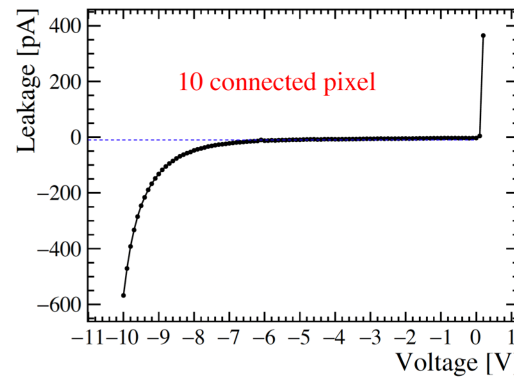
- IV curves show breakdown voltage ~ - 8V
  - Expected for low-resistance wafer
- CV curves measured for 1 pixel or 10 pixels connected
  - With offset subtracted the capacitance of a single pixel of $25\times150\ \mu m^2$ is 150~200 fF

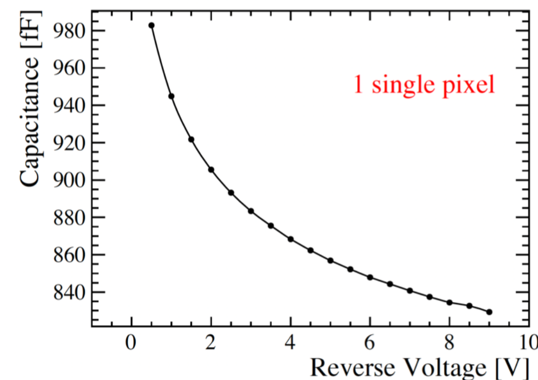


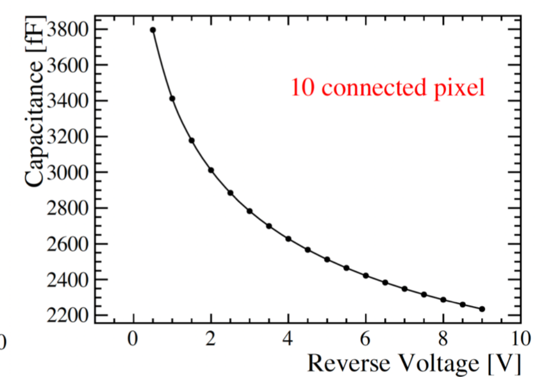
1 single pixel
$C \sim (180\times1 + 500)$ fF

10 pixels in parallel
$C \sim (180\times10 + 500)$ fF





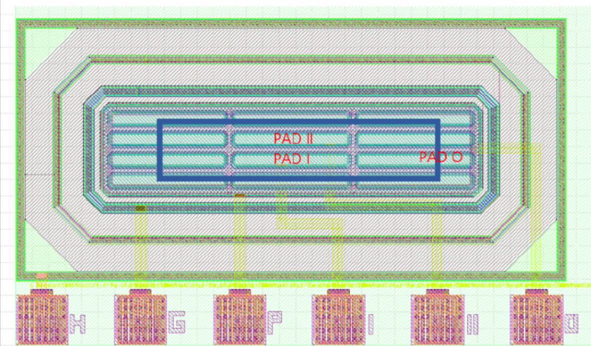


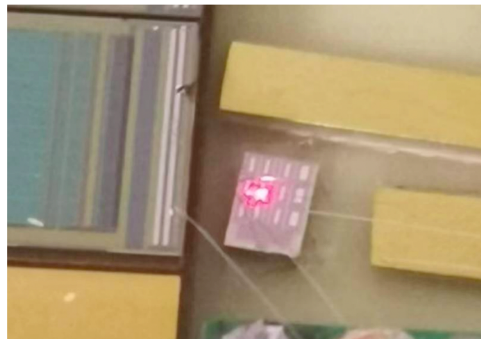


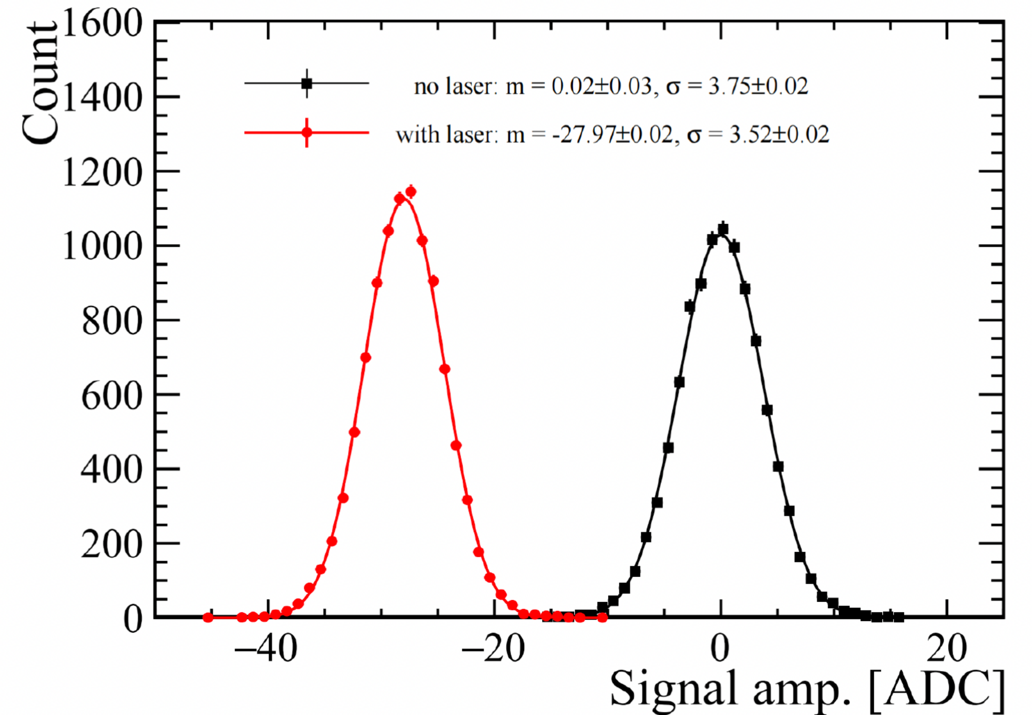
Zhiyu Xiang, Xiaoyu Zhu, Zijun Xu, YL

COFFEE1 laser test

- Ten pixel diode connected and a common output is read by an external ASIC (IDE1140)
- Red laser with beam spot ~0.5mm shines on top through opening above the sensor diodes
- Small yet clear signal response to laser
  - Corresponding to charge of ~2400 e-





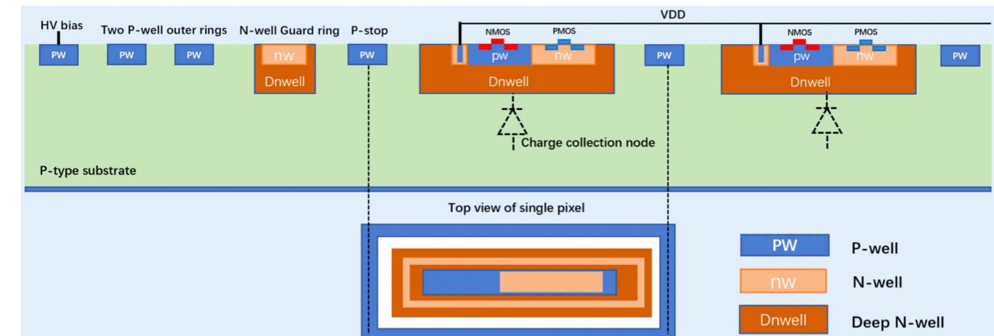


Zhiyu Xiang, Xiaoyu Zhu, Zijun Xu, YL

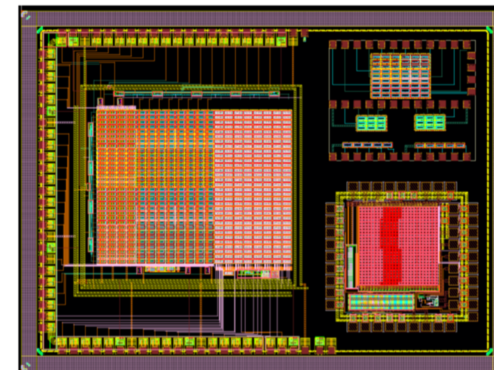
COFFEE2: MPW in HVCMOS process

- MPW with SMIC HV 55nm
  - High-res wafer of 2k or 1k Ωcm available
  - Real validation of the sensor
  - 4mm * 3mm in area
  - Passive arrays similar as COFFEE1
  - Two pixel arrays with in-pixel amplifier and more digital design
  - Submitted in Aug 2023
  - Received in Dec 2023

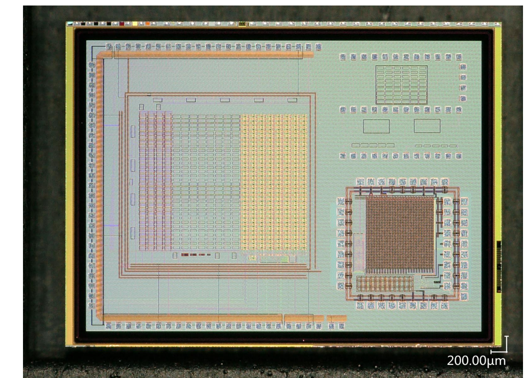
Cross-section of pixel strucure



COFFEE2 floorplan



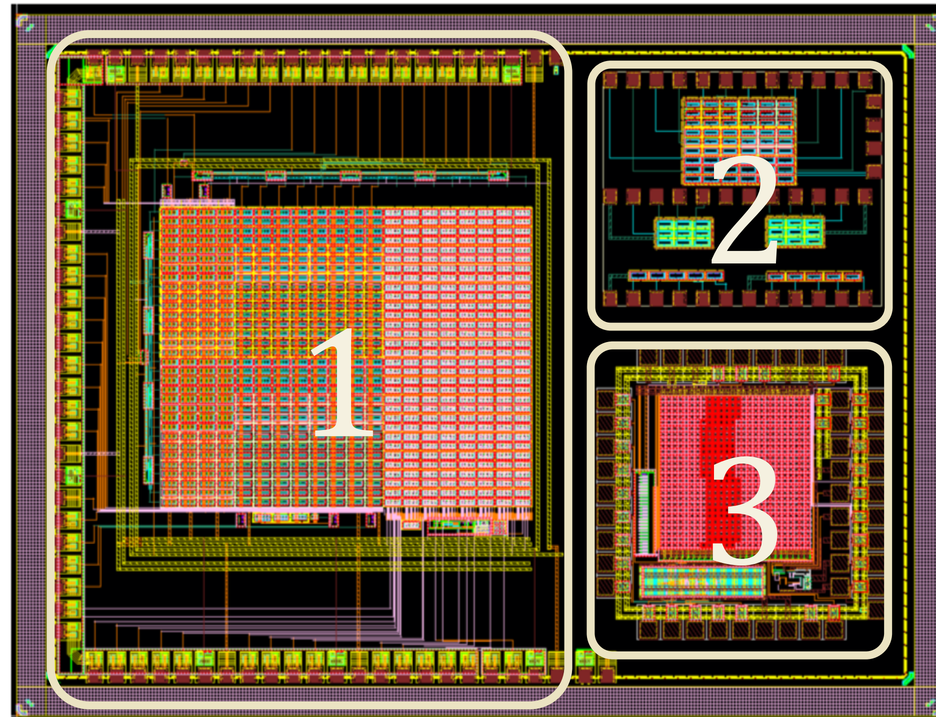
COFFEE2 photo



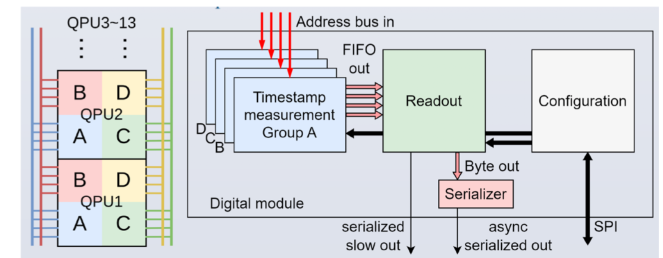
COFFEE2 design

1. 32 × 20 pixel matrix with various diodes and in-pixel amplifier or discriminator designs for process validation
   - $40 \times 80\ \mu m^2$
   - 5/10/15um gap btw pixels
   - With/ w.o. p-stops
   - 2 version in-pixel electronics

2. passive diode arrays, each has 3 × 4 pixels of size $40 \times 80\ \mu m^2$ for study on sensing diode and charge sharing



3. 26 × 26 pixel matrix of $25 \times 25\ \mu m^2$ pixels with digital readout periphery for novel electronics structure study



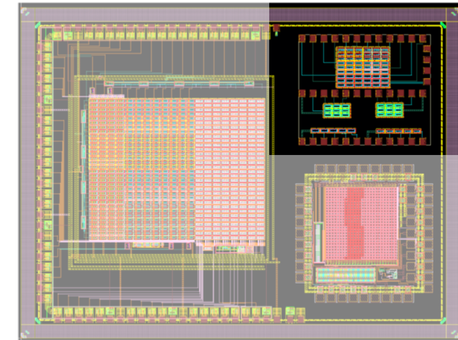
* Pixel size choice: similar area as $25 \times 150\ \mu m^2$ but less elongated

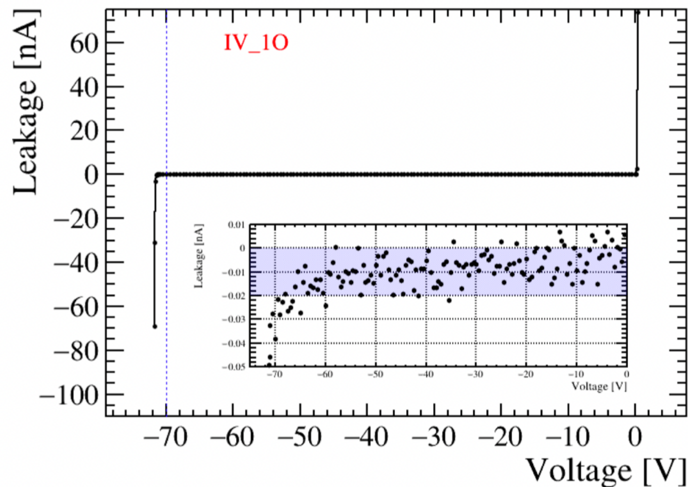
Yang Zhou, Mei Zhao, Weiguo Lu, Kunyu Xie, Leyi Li, Zhuojun Chen, Yunpeng Lu

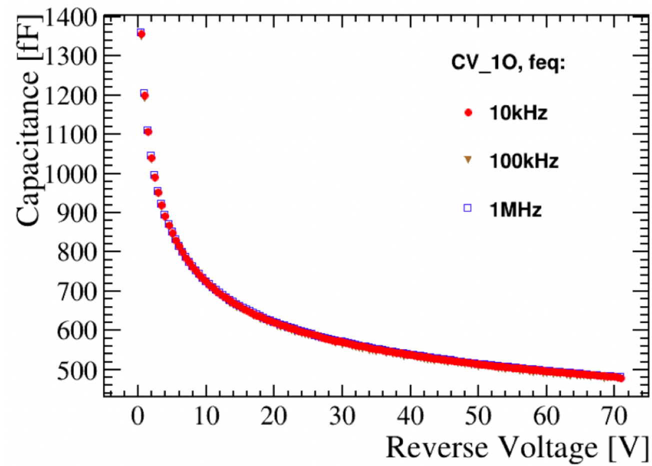
Ivan Peric, Hui Zhang, Ruoshi Dong

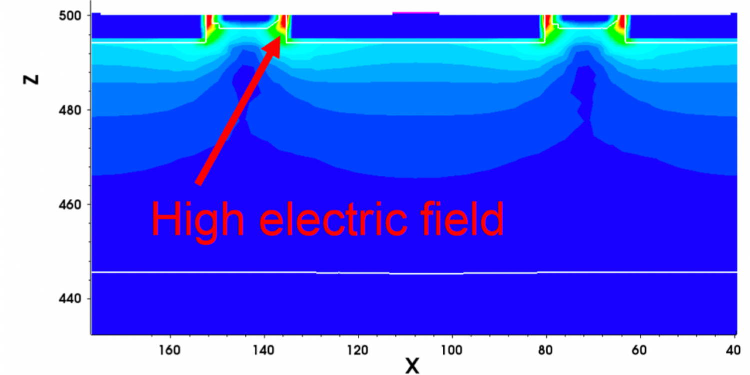
First tests of COFFEE2 sensors

- Breakdown voltage up to – 70V
- Full depletion not yet reached at breakdown
  - Confirmed by simulation
  - Due to p-well right next to the edge of deep n-well









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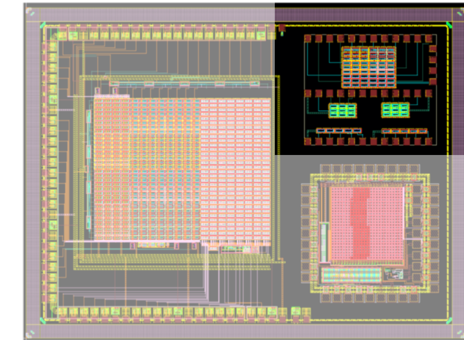
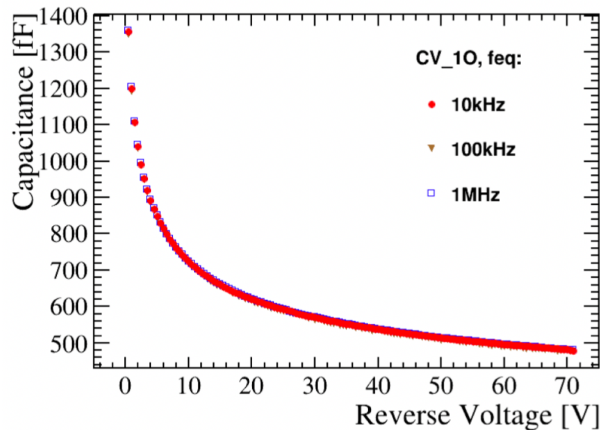
Jianpeng Deng, Hongbo Zhu

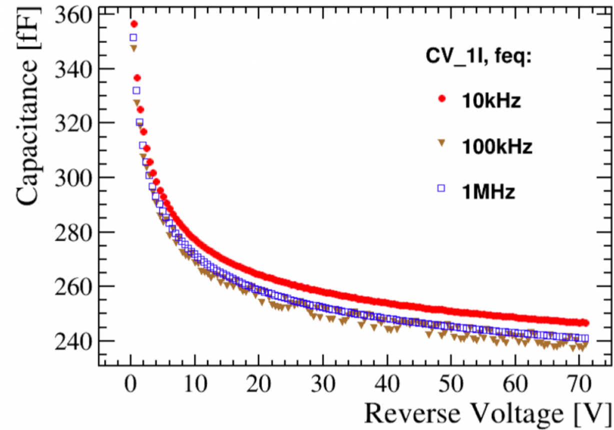
First tests of COFFEE2 sensors

- Breakdown voltage up to – 70V
- Full depletion not yet reached at breakdown
- Capacitance (with offset subtracted) scales with sensor area

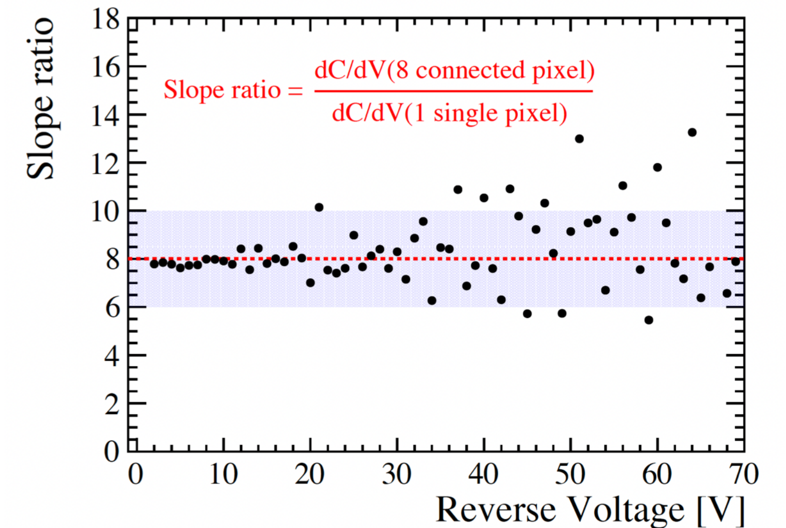




CV of 8-pixel connected
C(8) = 8*C0 + offset?



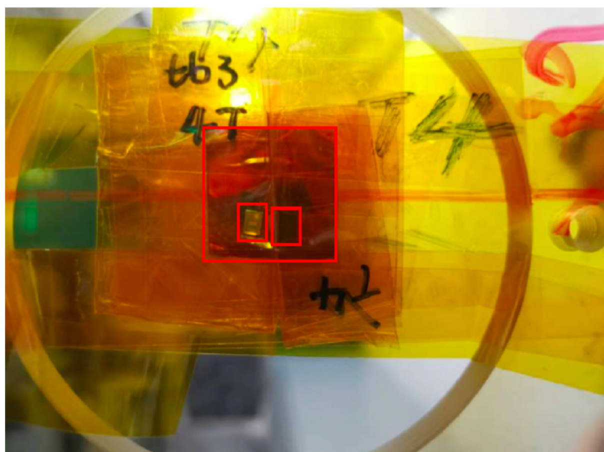
CV of a single pixel
C(1) =1*C0 + offset?

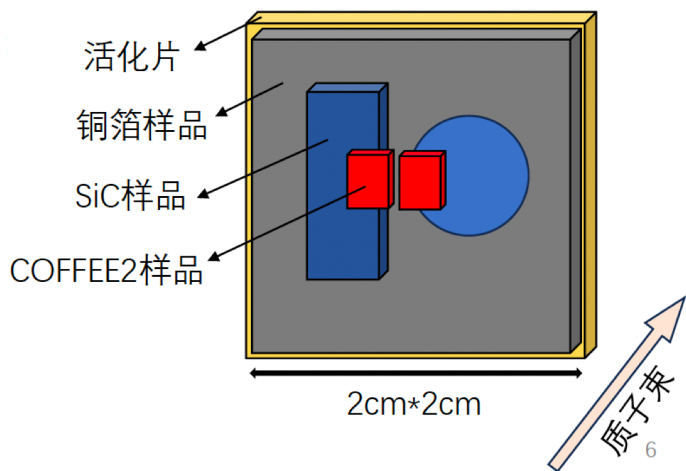


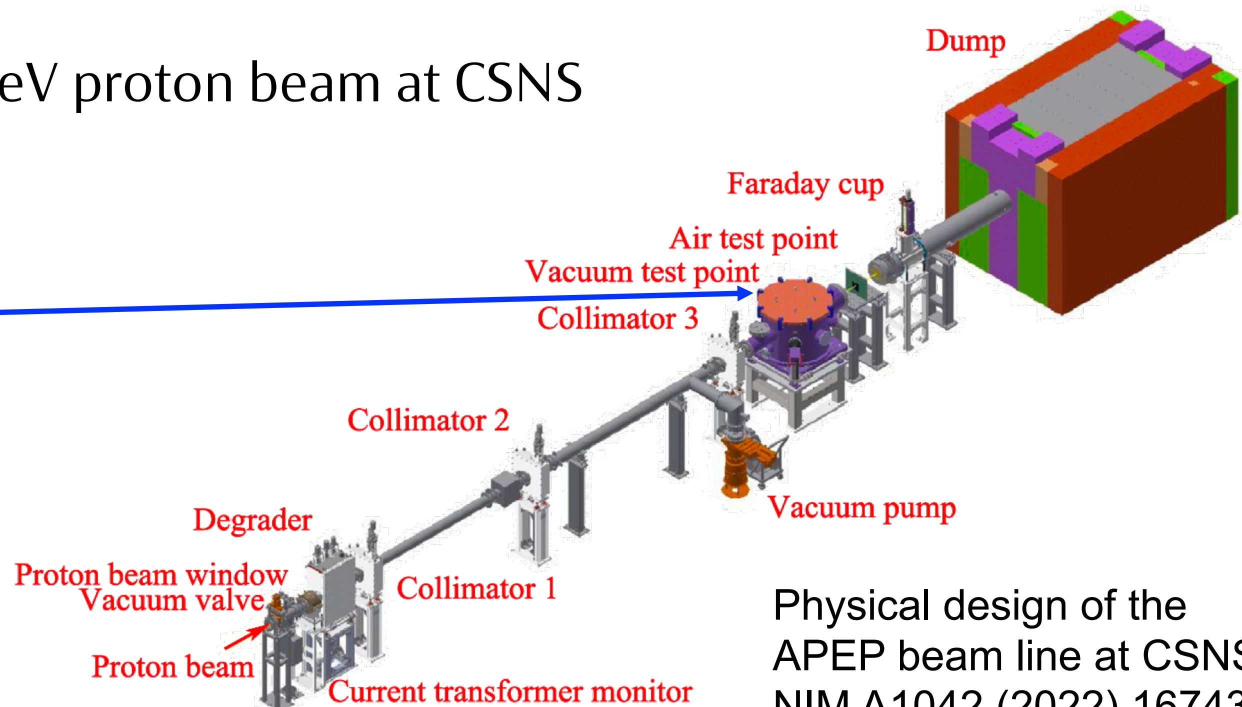
dC(8)/dV = 8* dC(1)/dV !

First tests of COFFEE2 sensors

- Sensors were recently irradiated in 80 MeV proton beam at CSNS







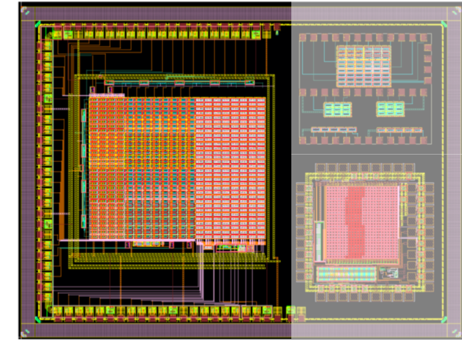
Physical design of the APEP beam line at CSNS, NIM A1042 (2022) 167431

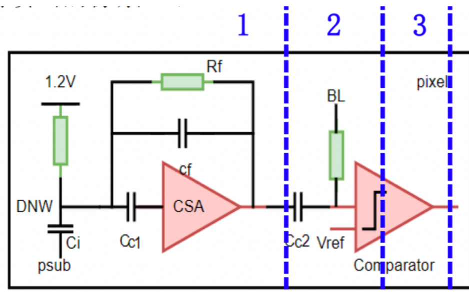
Fluence $[n_{eq} \cdot cm^{-2}]$	Condition
1.6×10^{15}	$-16^{\circ}C$
$2\times10^{11} \sim 1\times10^{14}$	Room temperature

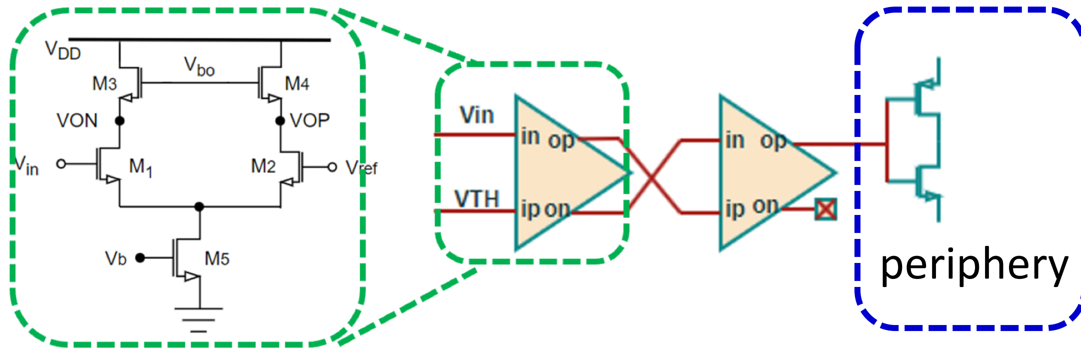
Zhiyu Xiang, Zijun Xu, Xiaojie Jiang, YL

Design and test of in-pixel circuit

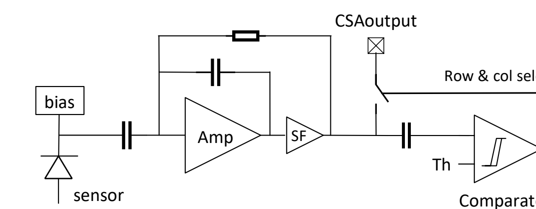
- Three types of in-pixel electronics
  - 1 – analog readout only
  - 2 – CSA + NMOS comparator -> ADC in periphery
  - 3 – CSA + CMOS comparator, digital output
  - A pixel is read out by row/column selector

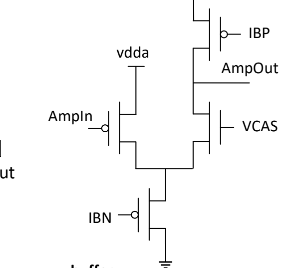


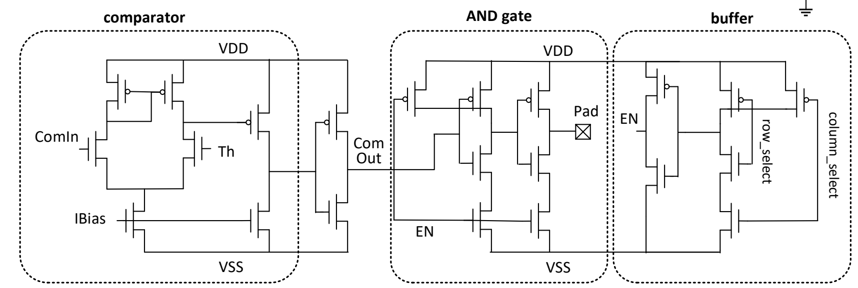




Kunyu Xie, Weiguo Lu



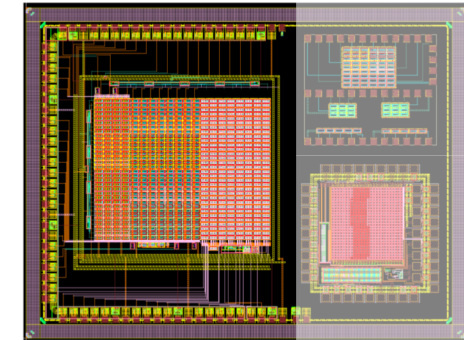


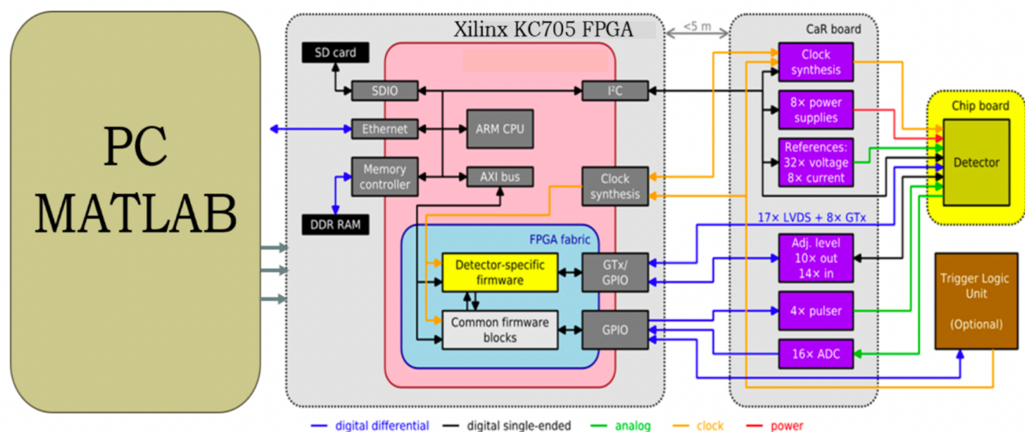


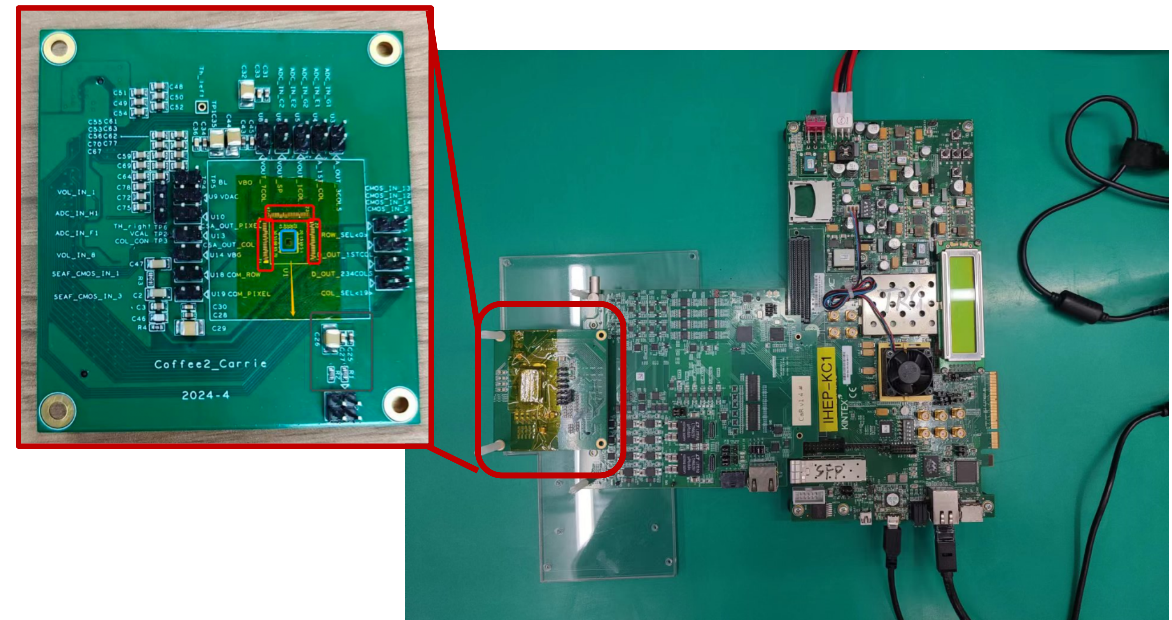
Leyi Li, Yang Zhou

Design and test of in-pixel circuit

- Test setup:
  - Carrier board → CaR test card → Xilinx KC705 FPGA → PC
- Carrier board designed and manufactured



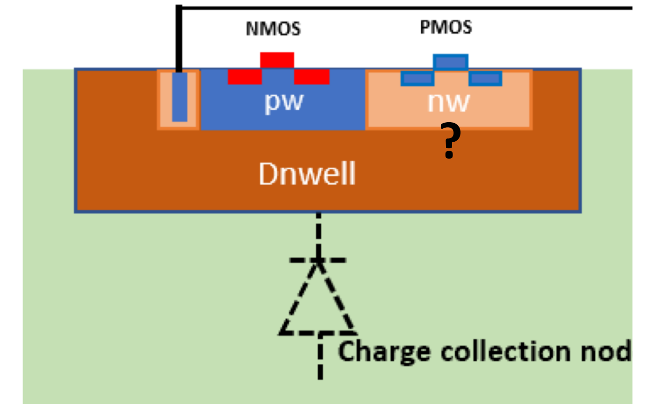


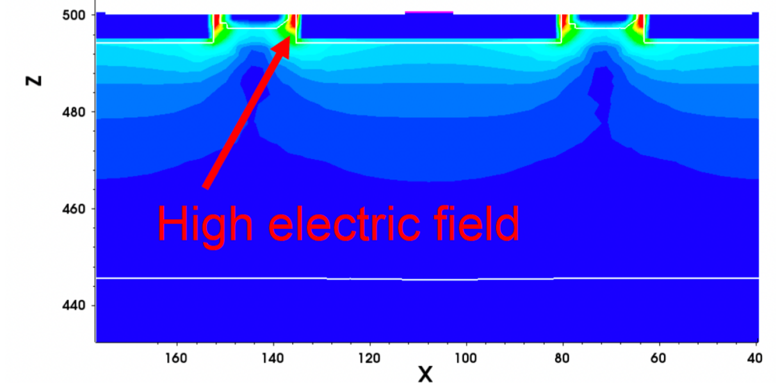


Kunyu Xie, Weiguo Lu

R&D plan

- Key issues to address in the process
  - Deep n-well and n-well connected (no deep p-well) -> Cross-coupling of digital circuit (especially PMOS) on collected signal charge?
  - How to increase biasing voltage? NB: breakdown occurs at the edge of DNW
  - Establishing modules of various functions
  - …
- Future R&D using 55nm planned
  - Thorough characterization of COFFEE2
  - MPW to implement small pixel array, with more in-pixel functions (eg. Timestamping)
  - Earliest MPW opportunity in Oct 2024
  - Eventually a prototype chip with larger array in 3-5 years





Conclusion

- HVCMOS is a promising technology for CEPC silicon tracker & LHCb UT upgrade among other possible application
- Search for alternative foundry of smaller feature size for the technical benefit and for risk reduction
- First results from MPW seems promising, test still ongoing
- More development foreseen in 55nm HVCMOS process