FPGA IRRADIATION @ NPTC-MGH (Round 2: SU vs Boston)

Ray Mountain, Bin Gui,

JC Wang, Marina Artuso

Syracuse University

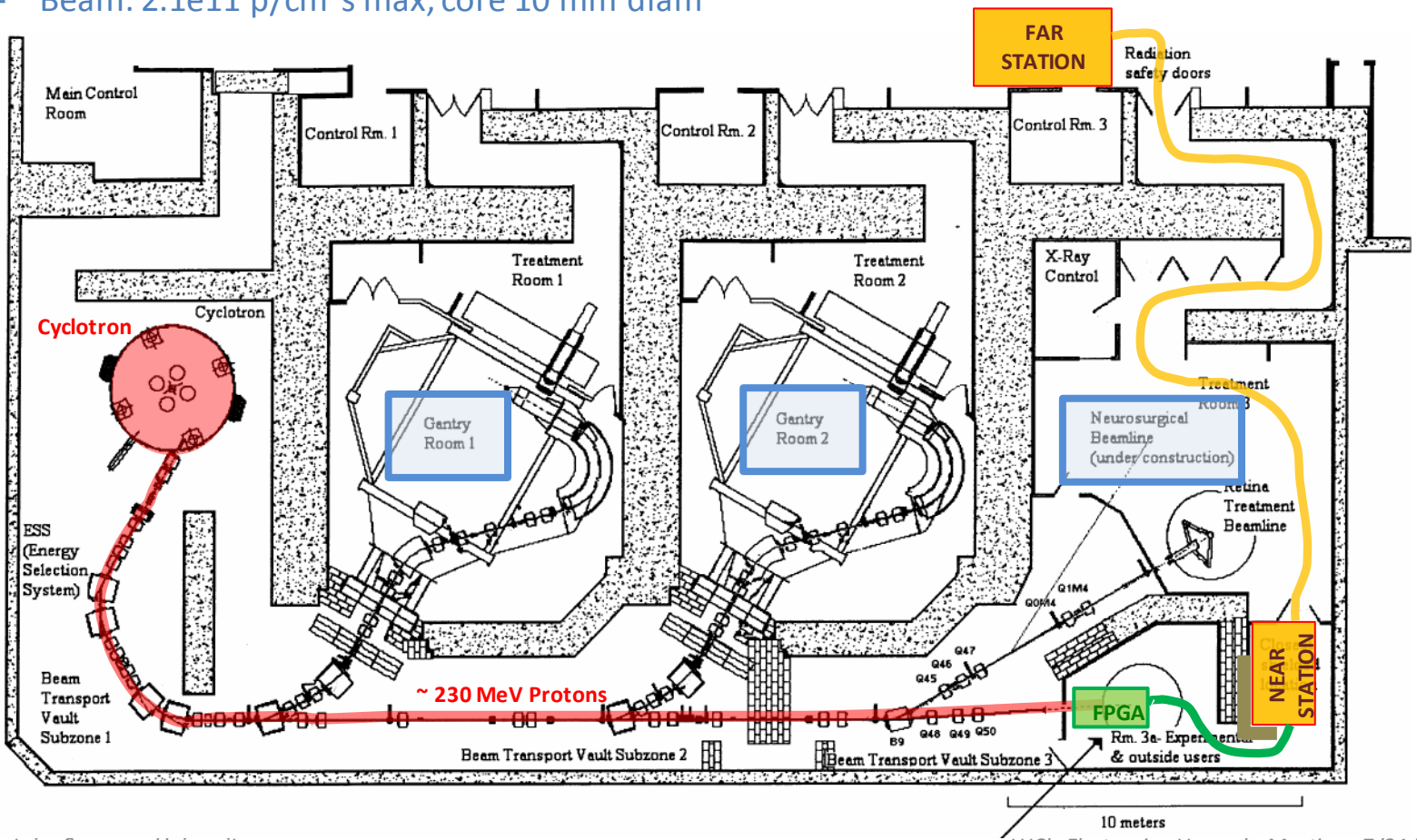
Outline

- **Irradiation Facility & Our Setup**
  - Quickie review
- **Irradiation**
  - Intensity and dose levels
- **Results: SEU test, RAM/ROM test, PLL**
  - Preliminary results
- **Radiation Damage Limits**
  - For logic, communications, configuration (program, verify)
- **FPGA Post-Mortem**
  - Characterization of current condition of our irradiated FPGAs
- **Annealing Results**
  - From previously irradiated device
- **Programmer Damage**
  - In-situ damage and recovery
- **Secrets from Actel (!)**
  - Tidbits from our discussions with Actel engineering
- **Summary / Work To Do**
  - Never done

THIS IS STILL WORK IN PROGRESS !

Irradiation Facility

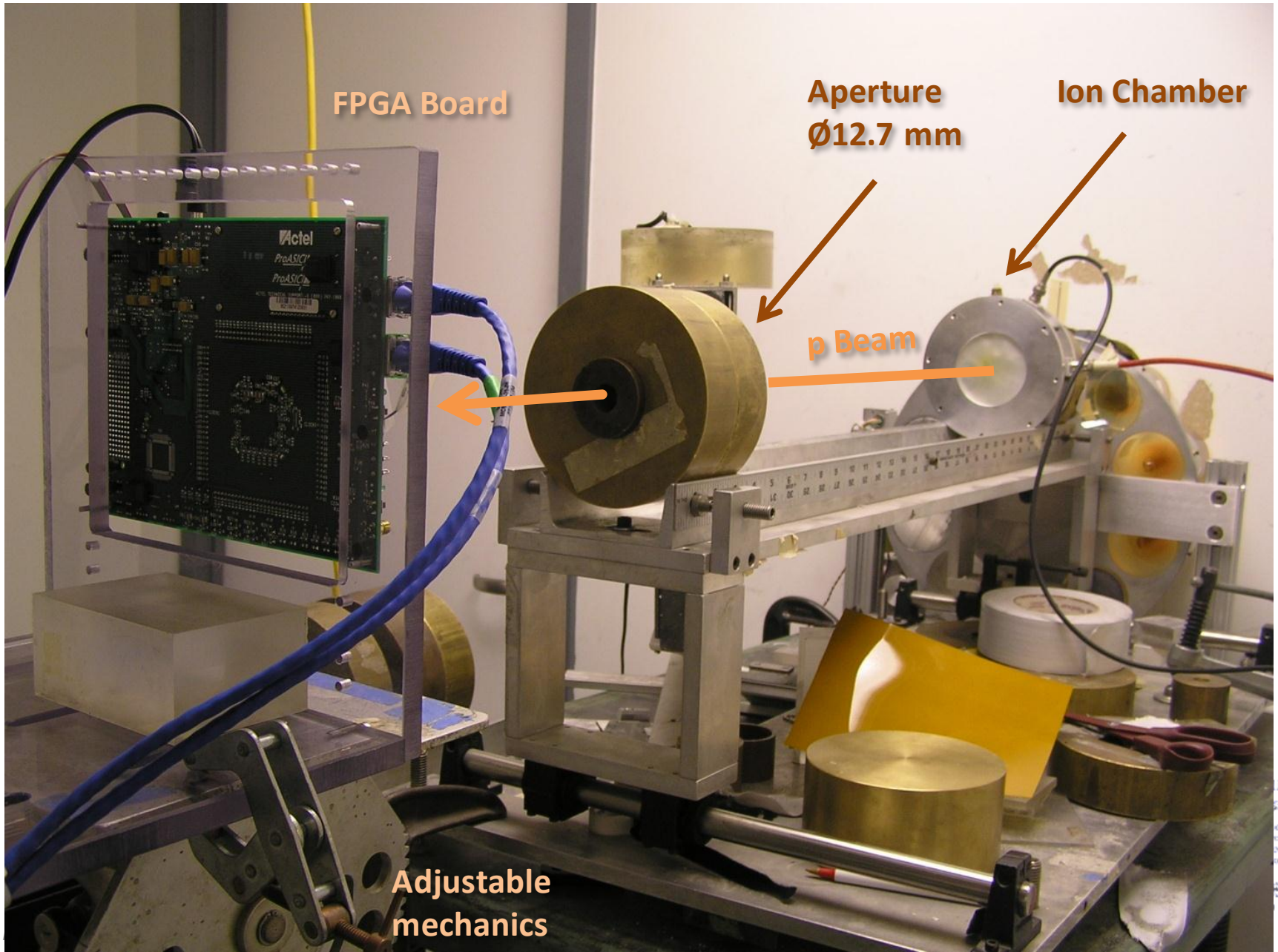
- **Northeast Proton Therapy Facility @ MGH**
  - Cancer facility, Mass General Hospital, Boston MA
- **Cyclotron:**
  - 230 MeV p primary beam, Pb foil scatterer, collimating aperture
  - Gives 226 MeV (~2 x MIP) on target, essentially monochromatic, E bite <1%
  - Dosimetry: Calibration w/ ion chamber, Faraday cup, <10% absolute, diode dosimeters
  - Beam: 2.1e11 p/cm^{2}s max, core 10 mm diam



FPGA Setup (1)

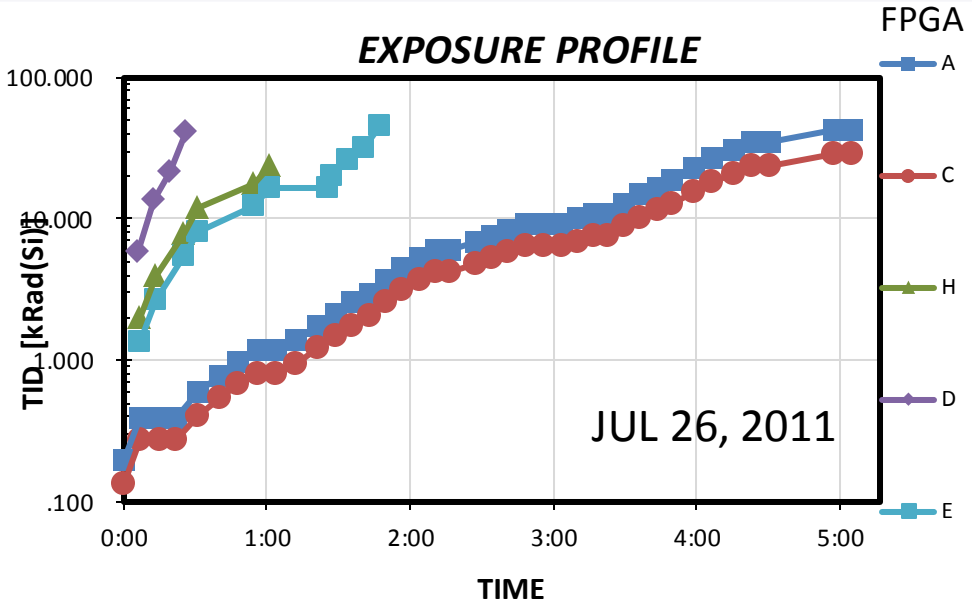
- **Actel ProASIC3 A3PE1500-PQ208**
- **Our Setup:**
  - FPGA on Eval PCB mounted in beamline, at 0 deg
  - Two stations now (front, back)
  - Tested 5 of 6 FPGAs this round
  - Programmers locally positioned (shielded, with shorter cable)
  - AC Power on remote relay (2 ch)
  - Near station: 2x(PC, TNG DIO, XBD, etc.)
    - Shielded, Borated PE (n_{th})
    - LabVIEW for comm and control (2 PCs)
    - Actel Libero for config (1 PC)
  - Far station: remote 2xLT connected to Near PCs
  - Current monitor circuits (2 ch)
  - Plus: Laser alignment, proton radiochromatography (proton "x-ray"), webcam

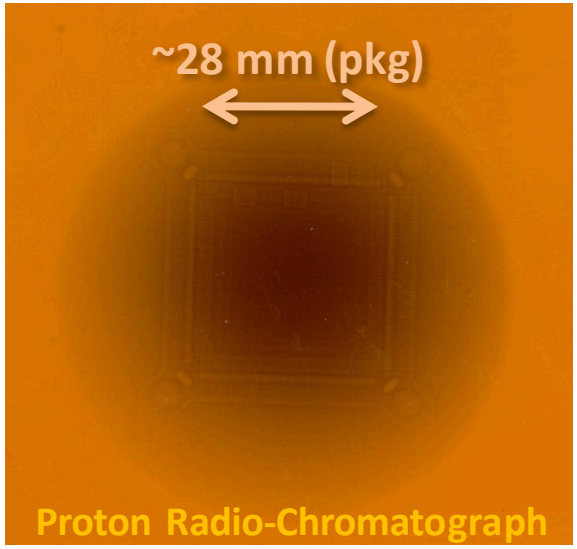
FPGA Setup (2)

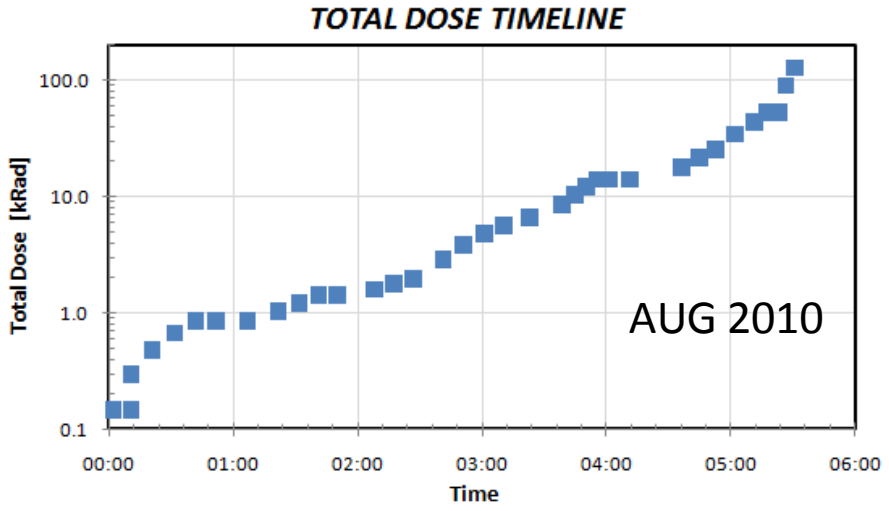

FPGA Board
Aperture
Ø12.7 mm
Ion Chamber
p Beam
Adjustable
mechanics

Irradiation

- **Irradiation**
  - Dose up to 127 kRad(Si)
  - Fluence up to 3.9E9 p/cm^{2}s @ 226.MeV
  - 226 MeV p = ~2 x MIP
  - Took lower/higher intensity runs
- **Beam location**
  - Centered on FPGAs
  - Laser aligned, checked with RCG image
- **Beam uniformity**
  - Adjust thin foil scatterer, 19 mm diam aperture
  - About 8% over central 8 mm
- **FPGA die: 7.9 x 7.7 mm2**

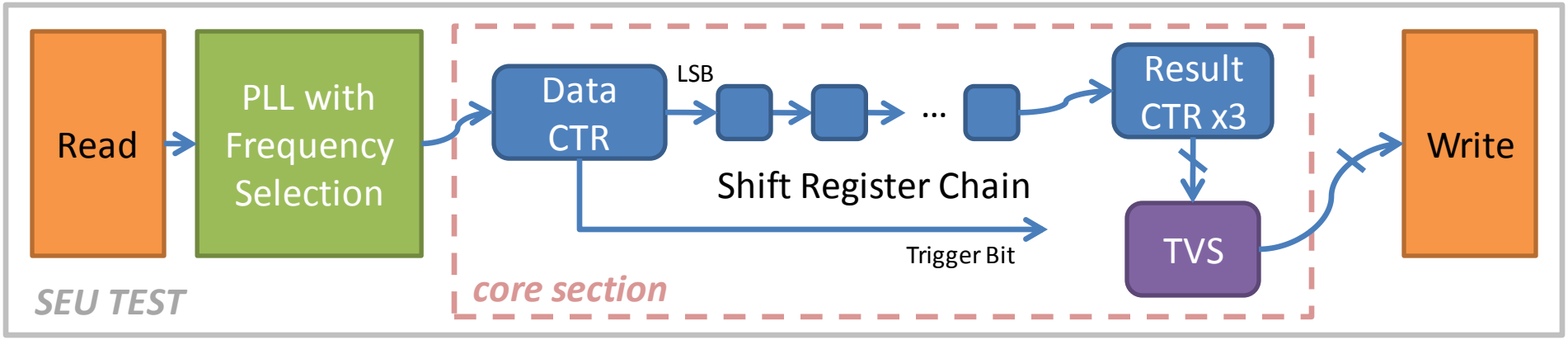






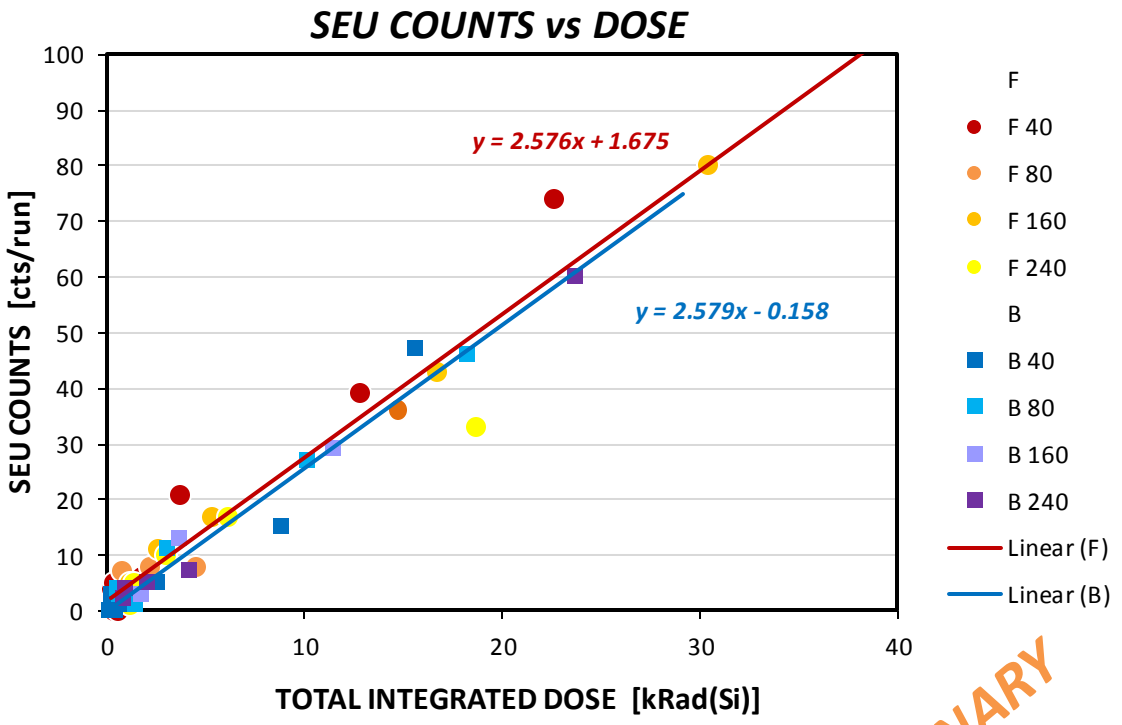
SEU Test (1)

- **SEU TEST re-coded**
  - Streamlined main algo and comm (less ambitious approach)
  - Incorporates new delay scheme
  - Modified to run for a fixed amount of time (~3.5 mins), uses trigger bit (e.g. 2^33 MSB tunable)
  - Select different frequencies: 40, 80, 160, 240 MHz
  - Data stream to SR is binary: 1010101…
  - Added triple voting into the design with 3 result counters
  - Bench tested for several weeks, various configurations
- **Physical constraint to place SR chain in central region of FPGA**
- **General Procedure for data runs**
  - Configure (if needed)
  - From LabVIEW: Set CLK freq, and Start (enable PLL CLK)
  - Irradiate (wait for fixed dose in a given run)
  - End (disable PLL CLK), after beam off
  - Read out results (write to LabVIEW)
- **Periodically**
  - Re-configure / verify configuration
  - Power cycle as necessary
- **Procedure same for RAM/ROM, with different core sections to code**



SEU Test (2)

- **Results**
  - See onset of SEU right away, even at very low doses
  - Linear increase with dose
- **Need to convert counts to a more physical quantity, etc.**
- **Seems understandable but expect threshold behavior?**
- **Still working on this**



PRELIMINARY

F = Front station (ROY)

B = Back station (BIV)

Different frequencies noted

Normalized to relative dose

(using diode calibration msrmts)

RAM/ROM Tests

- **SRAM core section**
  - Select PLL CLK frequency
  - Increment data counter and parallel write to 30 SRAMS (i.e., total that can fit in memory)
  - Compare SRAMs in pairs
  - Sum result of this comparison
  - TVS these 3 Adders
  - Repeat for each incremented values of data counter (until trigger bit asserted)
  - Run for fixed amount of time (~3.5 mins)
  - Output result (overall sum)
- **Results (first look)**
  - See a few counts in a few runs of a dozen total runs (expect zero in the case of no bit flips)
  - Difficult to interpret
  - Working on this

- **FROM core section**
  - Select PLL CLK frequency
  - FlashROM: 8 rows x 16 cols of 8-bit memory locations
  - During configuration, set FlashROM contents to pattern AA (10101010)
  - Read FlashROM contents once during beam (at end, controlled by trigger bit)
  - Compare bit-by-bit
  - Count the number of bits that are different than expected
  - Run for fixed amount of time (~3.5 mins)
  - Output result
  - (Alternately, could also choose to count number of memory locations with incorrect bits)
- **Results (first look)**
  - Also see a few counts in a few runs of a dozen total runs
  - However, also see verify fails associated with FlashROM memory locations (this is part of the verification procedure when the FROM is used)
  - Working on this

NIKHEF PLL

- **SORRY !**
- **By the time we solved all the problems in the weeks leading up to the beam test, we just ran out of time to get the PLL code fully integrated into the setup, so not included in this round**

Radiation Damage Limits (1)

FPGA	Logic	Communications	Configuration	Comment
A	30.5–34.4	> 42.2*	10.8–34.4 (CFG) *Code 24: Bad Device*	Lower intensity
B	—	89.9–127.0*	14.0–52.9 (VFY,CFG) *Code 24: Bad Device*	Irradiated previously
C	23.7–29.2	> 42.2*	7.5–23.7 (CFG) *Code 24: Bad Device*	Lower intensity
D	> 41.3* *(provisional)*	> 41.3*	< 41.3* (VFY,CFG) *Code 5: Programmer Fail*	Cfg upper limit unclear
E	> 44.7* *(provisional)*	> 44.7*	16.3–44.7* (VFY,CFG) *Code 5: Programmer Fail*	Cfg upper limit unclear
G	—	—	—	Not Irradiated
H	17.7–23.6*	> 23.6*	11.8–23.6* (VFY,CFG) *Code 24: Bad Device*	High-frequency "-2" device
	• Damage: Results become questionable. • Logic is constrained to central region of FPGA	• Damage: Basic communications and handshaking fails. • Communications resides in periphery of FPGA.	• Damage: Unable to erase, program or verify (JTAG) • Probably cause of configuration failure noted	

PRELIMINARY

Notes:

1. All devices are Actel A3PE1500 (except H, which is A3PE1500-2)
2. All units are kRad(Si) on target FPGA, indicating dose range or limit at which a FAIL occurs
3. (*) Indicates maximum irradiation for a given FPGA

Radiation Damage Limits (2)

- **Configuration:**
  - Damage: Unable to erase, program or verify (JTAG)
  - First to show signs of damage
  - Limits a bit unclear for FPGA D & E, due to interference of programmer failure
- **Logic**
  - Damage: Results become questionable (i.e., too large or too small, far away from trend)
  - Logic modules physically constrained to central region of FPGA tile area
  - Logic continues to work (as far as we can tell) until approximately the high end of configuration failure range
  - Logic range unclear again for FPGA D & E, still need to interpret RAM results
- **Communications**
  - Damage: Basic I/O communications and handshaking fails (i.e. doesn't respond)
  - Communications modules physically reside at periphery of FPGA tile area
  - Communications continue to work until maximum dose applied
  - Beam profile is about 10% down at periphery of device, so this is not simply explained by the physical position of the tiles (i.e., dose is not significantly reduced at periphery)
- **Other preliminary observations**
  - Does seem to explain last year's result:
    - FPGA B had its logic and configurability fail at ~1/2 its max dose
    - Logic not working properly due to timing issues
    - Communications continued to work until the bitter end, when the device was damaged beyond recovery
  - The high-frequency "-2" device, FPGA H, appears to fail earlier than the standard device
  - Rough goal was: Operational up to 30 kRad/100.fb^{-1}

FPGA Post-Mortem

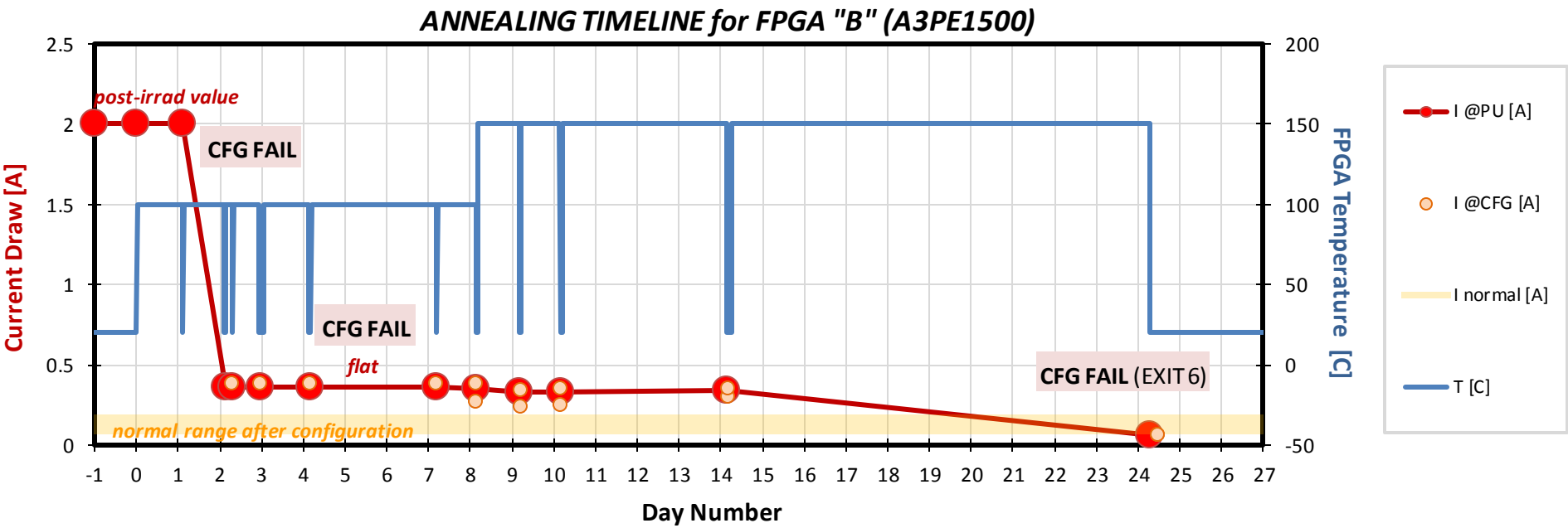
- **Current conditions of irradiated FPGAs**
  - As tested at Syracuse

FPGA	Can Verify?	Can Program?	Does it run?	Result of running	Comment
A	Failed	Failed	Yes	Wrong	
B	Failed	Failed	NO	—	Irradiated previously
C	Failed	Failed	Yes	Wrong	
D	Failed	TBD	Yes	Wrong	
E	Failed	TBD	Yes	Correct	
G	Passed	Passed	Yes	Correct	Not irradiated
H	Passed	TBD	Yes	Wrong	High-freq "-2" device, smallest max dose

- **Plan to try annealing and see if any can recover**
  - Some hope, since most of them run the program last cfg'd

Annealing

- **FPGA B (rad damaged last year)**



- **Results**
  - Never recovered from radiation damage
  - Cannot run program
  - Cannot configure (even a small program, confined to periphery of FPGA tiles)
  - Not just a low Vcc preventing it from functioning (provisional explanation)
  - Seems to be really most sincerely dead

Programmer Damage

- **In beam zone**
  - Had a large number of CFG fails
  - Recovered by reducing the cable length from programmer to board (141.cm to 16.cm)
  - But that puts the programmer closer to the beam (whereas 141.cm cable allows a shielded location)
  - As expected, it exhibited rad damage and eventually "died" (EXIT 5: Bad programming device)
  - Overall: saw ~75% CFG failures (program and verify) with 141.cm cable, and ~25% with 16.cm cable (before it died)

- **At Syracuse**
  - Checked programmers
  - All seemed to have recovered (!)
  - All three tested fine with 16.cm cable, but had >75% CFG fails (program only) with 141.cm cable and also with our original 7.m cable (used last year)
  - So short cable most reliable

- **Consequences for the upgrade design**
  - Need to retain short cable run from programmer to FPGA
  - This places programmer close to FPGA and in its rad field
  - Need to shield programmer (or equivalent circuit) very well
  - Need to have lots of spares

"Secrets" from Actel (1) – Rad Dam

- **Hierarchy of Failures**
  - Parametric failure: some spec from data sheet violated (e.g., Vcc too low)
  - Functional failure: device not behaving correctly (e.g., device dead)
- **Order of Radiation Damage effects**
  - *Level 1*: Icc increases
    - A "parametric" failure, behavior no longer guaranteed
  - *Level 2*: Device slows down
    - Total propagation delay for chain of combinational logic gets longer (e.g., a time for "execution" of 1000 chained AND gates increases)
  - *Level 3*: Functionality fails
    - A "functional" failure, device becomes unresponsive or appears dead
  - *Level 4*: Ultimate
    - Catastrophic failure, unspecified or unknown source of damage…it's baaaad
- **Annealing**
  - When annealing fails, device had been severely internally damaged, damage beyond Level 3; it is typically unrecoverable (our FPGA B)

"Secrets" from Actel (2) – Config

- **Programming procedure**
  - Transfer bitstream packet over JTAG line
  - Packet received by dedicated circuitry, then decoded and mapped to the proper flash switches
  - Separate circuitry, not a state machine
  - Sense amps are analog, addressing is digital
- **Verification procedure**
  - Same, but each packet now compared to respective switches
  - A single status bit is kept for verification pass/fail, and is returned to user
  - Cannot read back configuration: conscious design choice, for device security (absolutely cannot access program), NOT due to flash design
- **Radiation damage more severe when programming?**
  - No data on this, just "common sense" expectation – there may be a report
- **Other items**
  - Should select VJTAG 3.3 in GUI
  - Cable length issue: get reflections and failures, if pgm cable too long
  - EXIT-24 error: probably VPUMP out of spec (>5% parametric)

Summary / Work To Do

- **In Summary…**
  - Have tested 5 additional FPGAs in doses up to 45 kRad(Si) and have obtained results for SEU, RAM, ROM tests
  - Have extracted rad damage limits for exposures with an ad-hoc behavioral model
  - Have characterized some programmer behavior

- **Continue data reduction**
  - Interpret SEU in terms of physical quantity
  - Extract RAM/ROM limits
  - Integrate current measurements (readout somewhat intermittent in beam zone, but see increased current with dose)
- **Post-Mortem work**
  - Characterize FPGA conditions, investigate failure modes
  - Including annealing
- **Extract bottom-line rates, mitigation schemes, etc.**

- **Next irradiation test: ?**
  - Resources now exhausted for this project