GLIB, Gigabit Link Interface Board

Paschalis VICHOUDIS
PH-ESE-BE

on behalf of the GLIB team
(S. Baron, M. Barros Marin, V. Bobillier, S. Haas, M. Hansen, M. Joos, F. Vasey, P. Vichoudis)

LHCb UPGRADE ELECTRONICS 21 JULY 2011

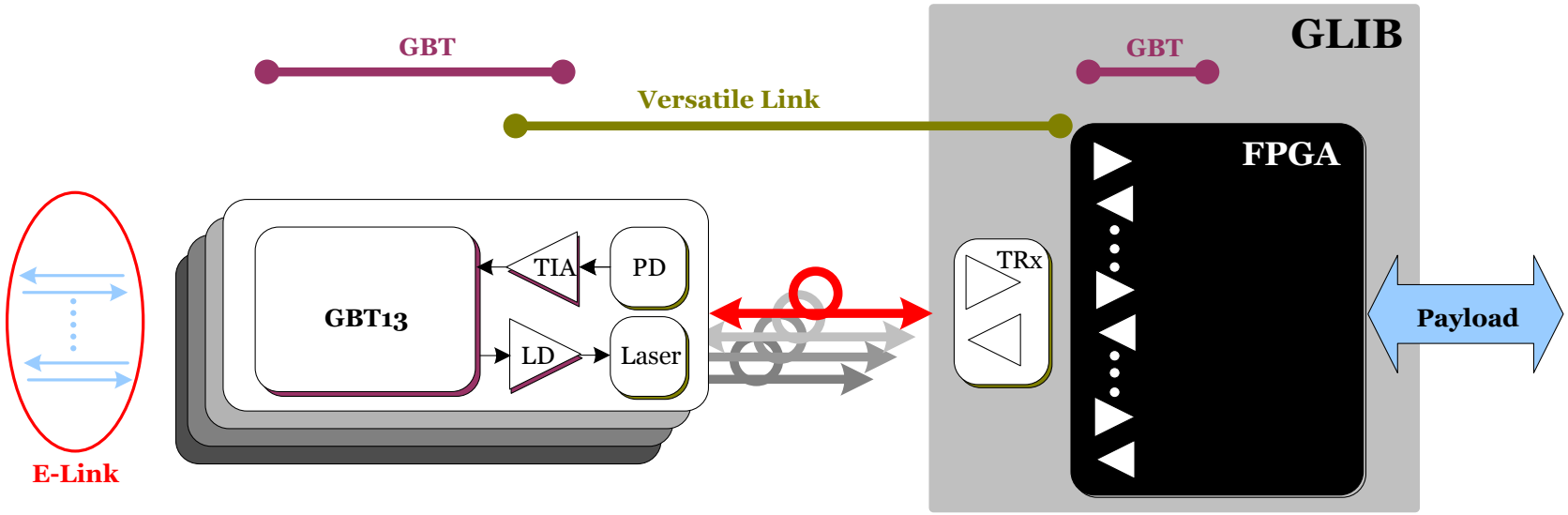
Introduction

CONCEPT

THE GLIB IS: an evaluation platform and an easy entry point for users of high speed optical links

THE GLIB IS TARGETED FOR:

- optical link evaluation in the laboratory
- control, triggering and data acquisition from remote modules in beam or irradiation tests



Introduction

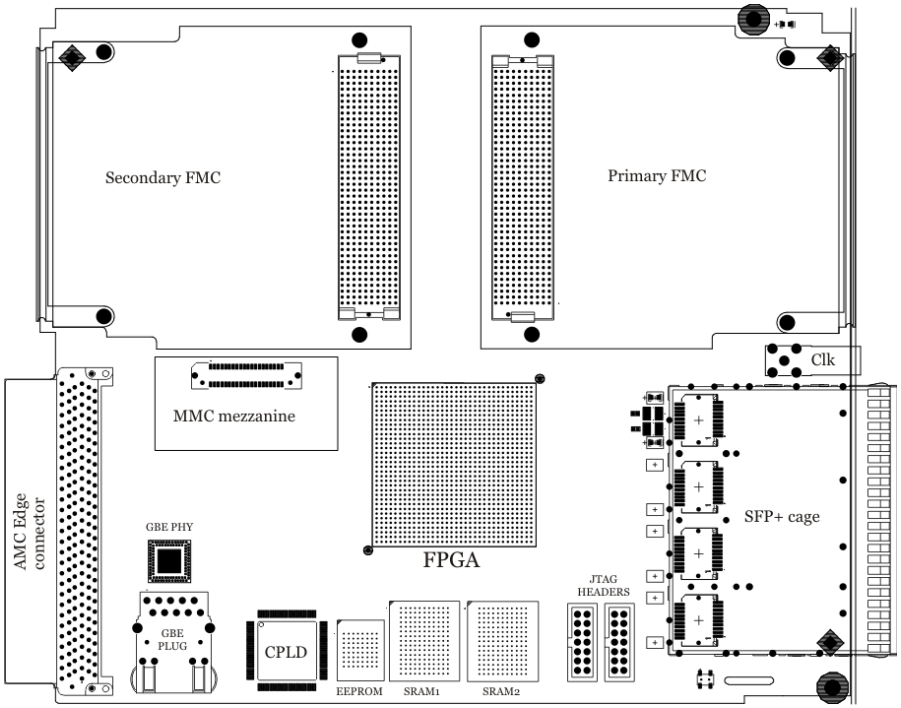
GUIDELINES

- ✓ Rapid development (first prototype spring 2011)
- ✓ "Low" cost (capacity limited to four GBT lanes)
- ✓ Long lifetime (distribution and support of a small set of variants over several years)
- ✓ User-driven evolution potential
  (via mezzanine cards, FPGA pin compatible upgrades, different firmware versions)

Introduction

OVERVIEW

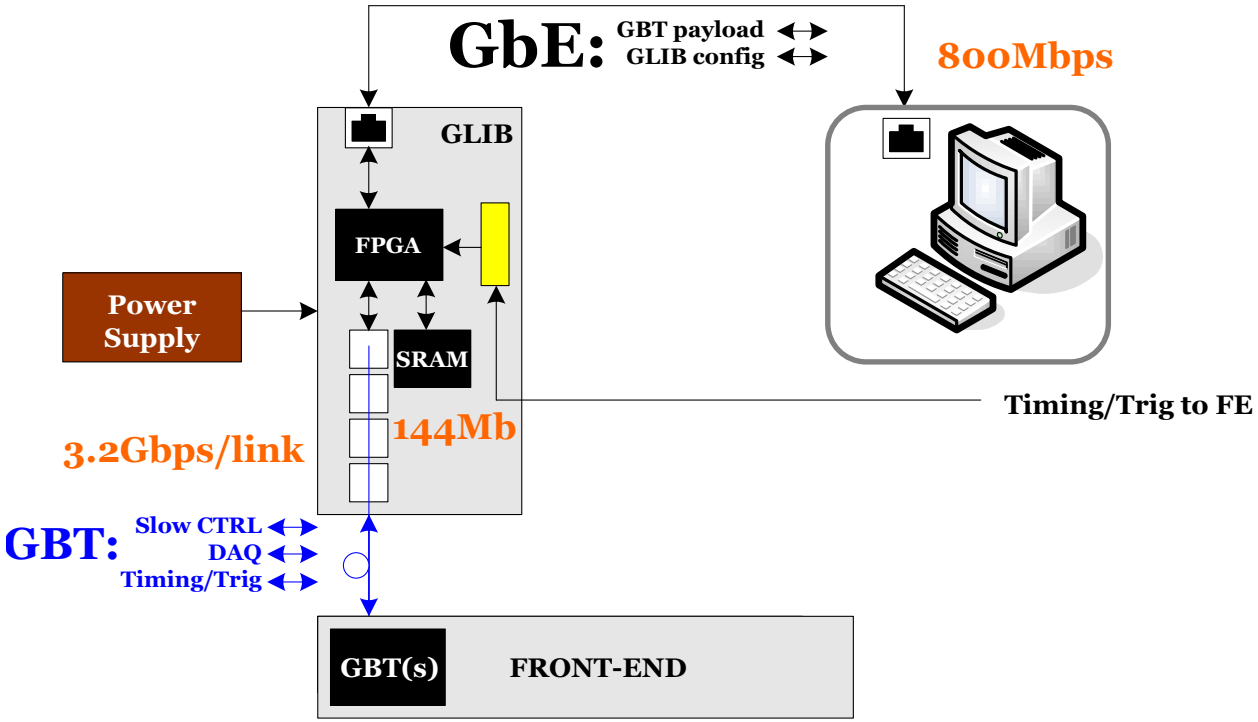
- ✓ Double width AdvancedMC (AMC) module for µTCA environment or bench-top use.
- ✓ Based on a high-performance Virtex-6 FPGA with Multi-Gigabit Transceivers (MGTs) up to 6.5Gbps.
- ✓ Sockets for up to four pluggable 10Gbps optical transceiver modules (SFP+).
- ✓ Sockets for two expansion FPGA Mezzanine Cards (FMCs) for user-specific I/Os and up to four additional MGTs (optional).
- ✓ On-board memory



Introduction

TYPICAL USE CASES (1/6)

BENCH-TOP: beam test setup

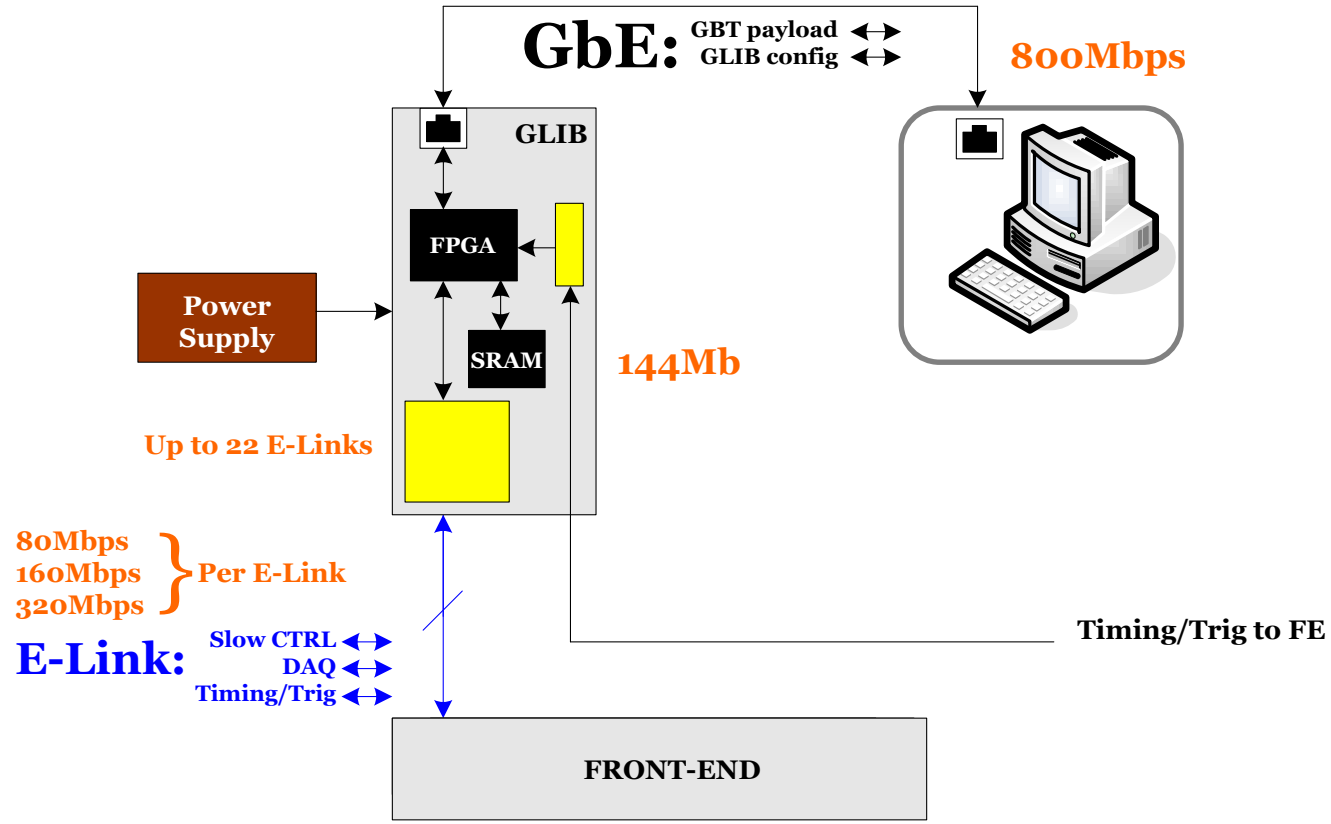


= TTC FMC = SFP+

Introduction

TYPICAL USE CASES (2/6)

BENCH-TOP: front-end module test setup

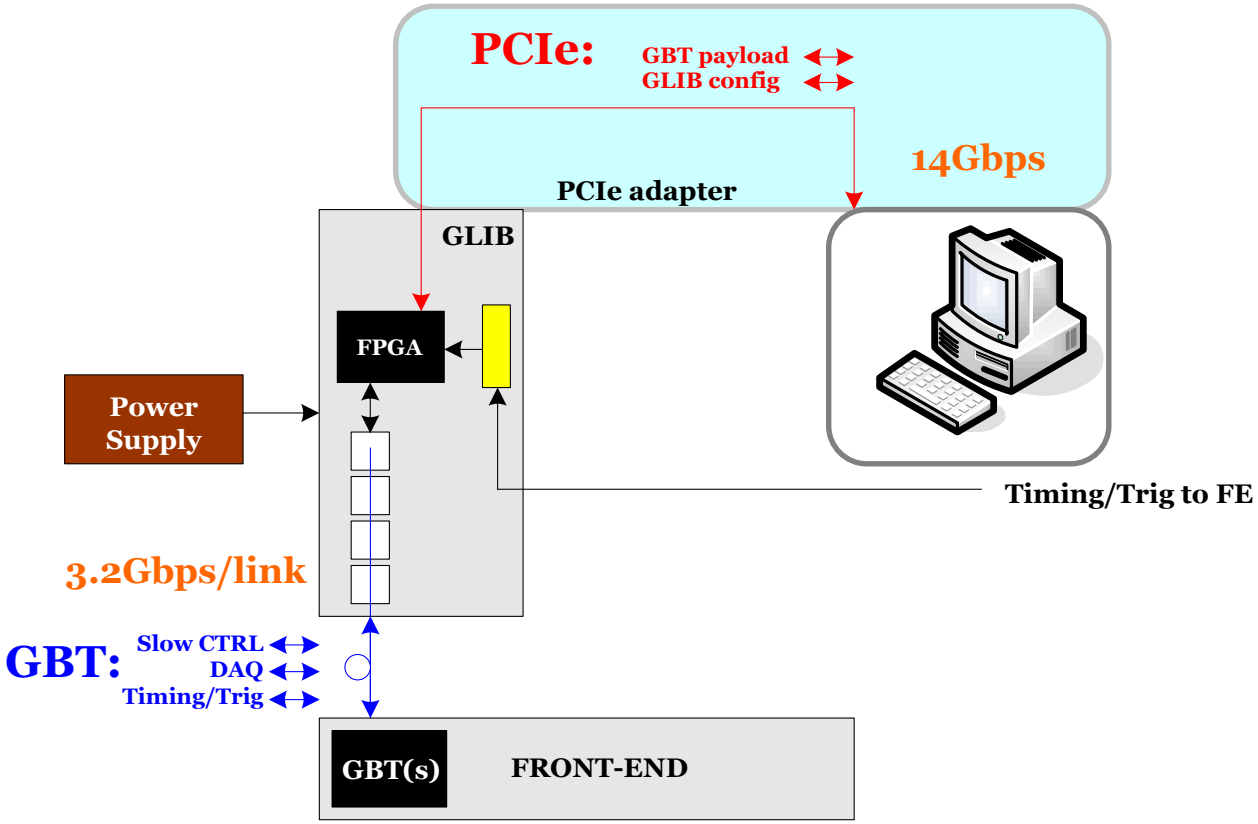


= E-LINK FMC = TTC FMC = SFP+

Introduction

TYPICAL USE CASES (3/6)

BENCH-TOP: system test setup

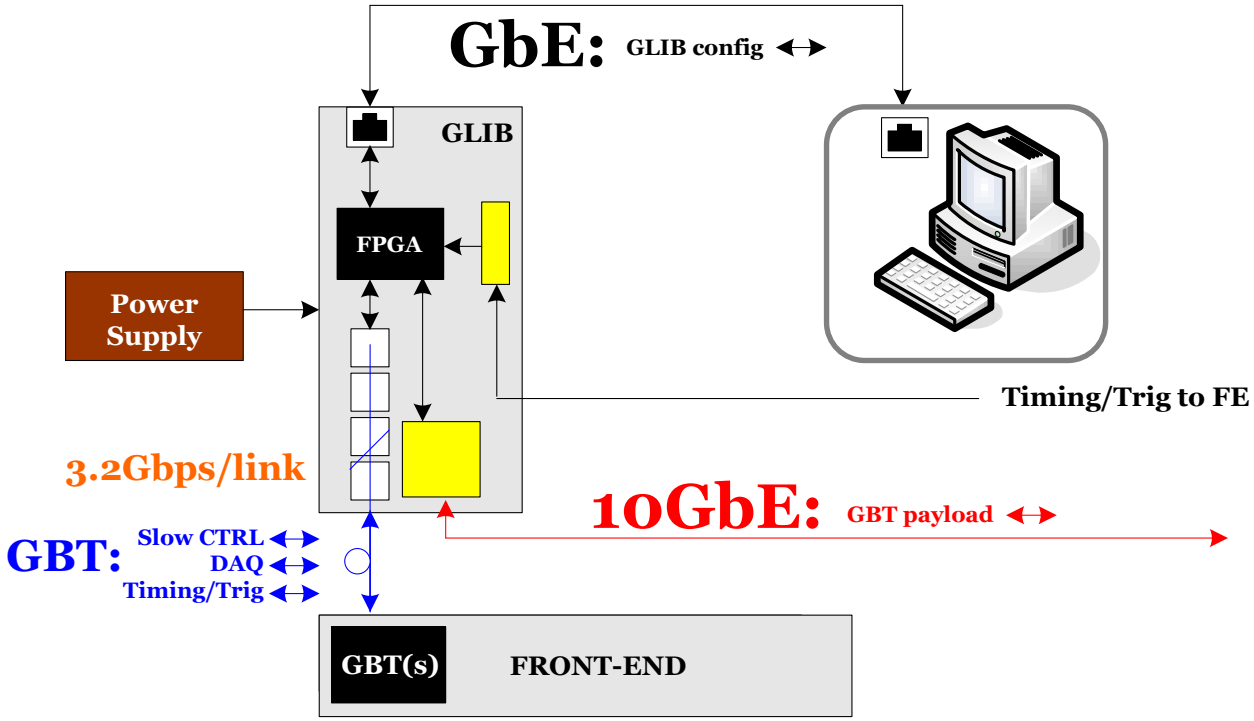


= TTC FMC = SFP+

Introduction

TYPICAL USE CASES (4/6)

BENCH-TOP: system test setup [remote control/readout]

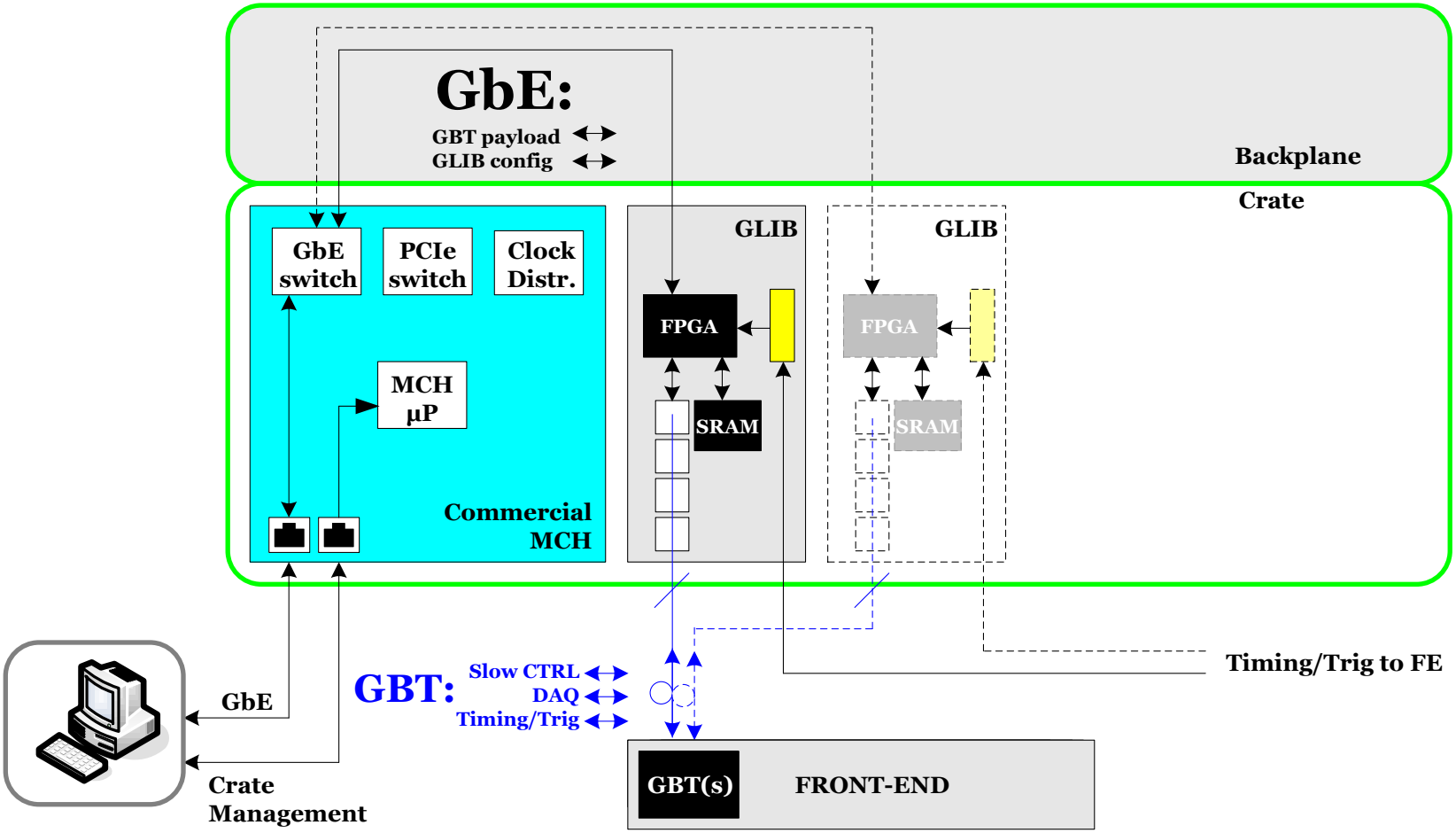


= 10GbE FMC = TTC FMC = SFP+

Introduction

TYPICAL USE CASES (5/6)

CRATE: beam test setup

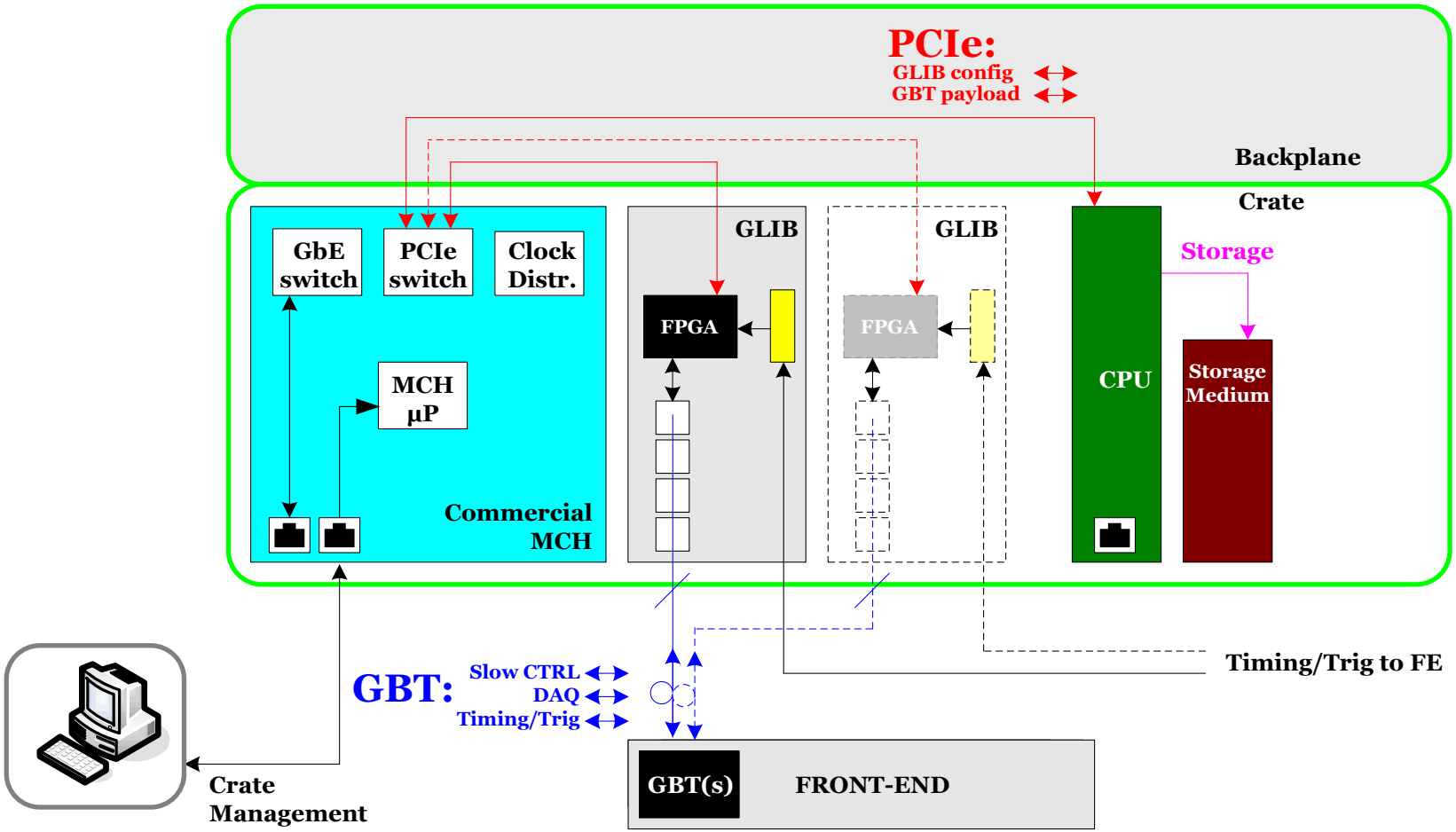


= TTC FMC = SFP+

Introduction

TYPICAL USE CASES (6/6)

CRATE: system test setup



= TTC FMC = SFP+

Introduction

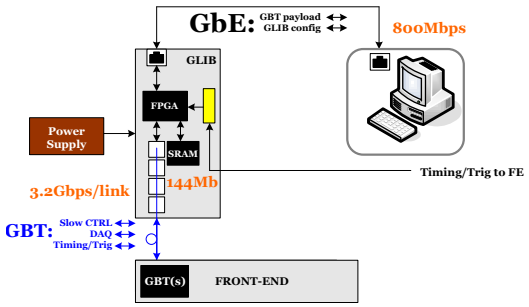
DELIVERABLES

The GLIB team envisages to deliver and support software, firmware and hardware for the following 3 setups:

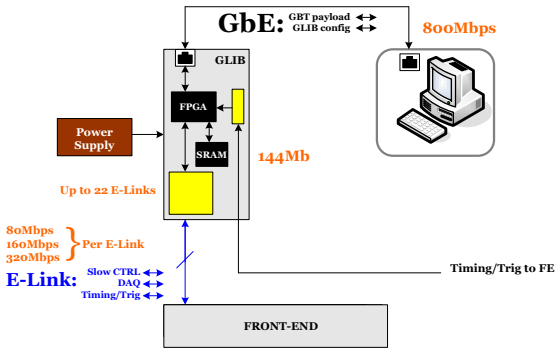
- **Bench-top beam test setup**
- **Bench-top front-end module test setup**
- **Crate system test setup**

The required FMCs (TTC & E-Link) will also be delivered and supported.

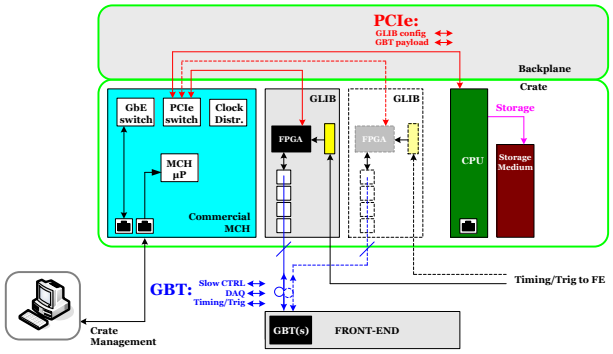
Bench-top beam test setup



Bench-top front-end module test setup



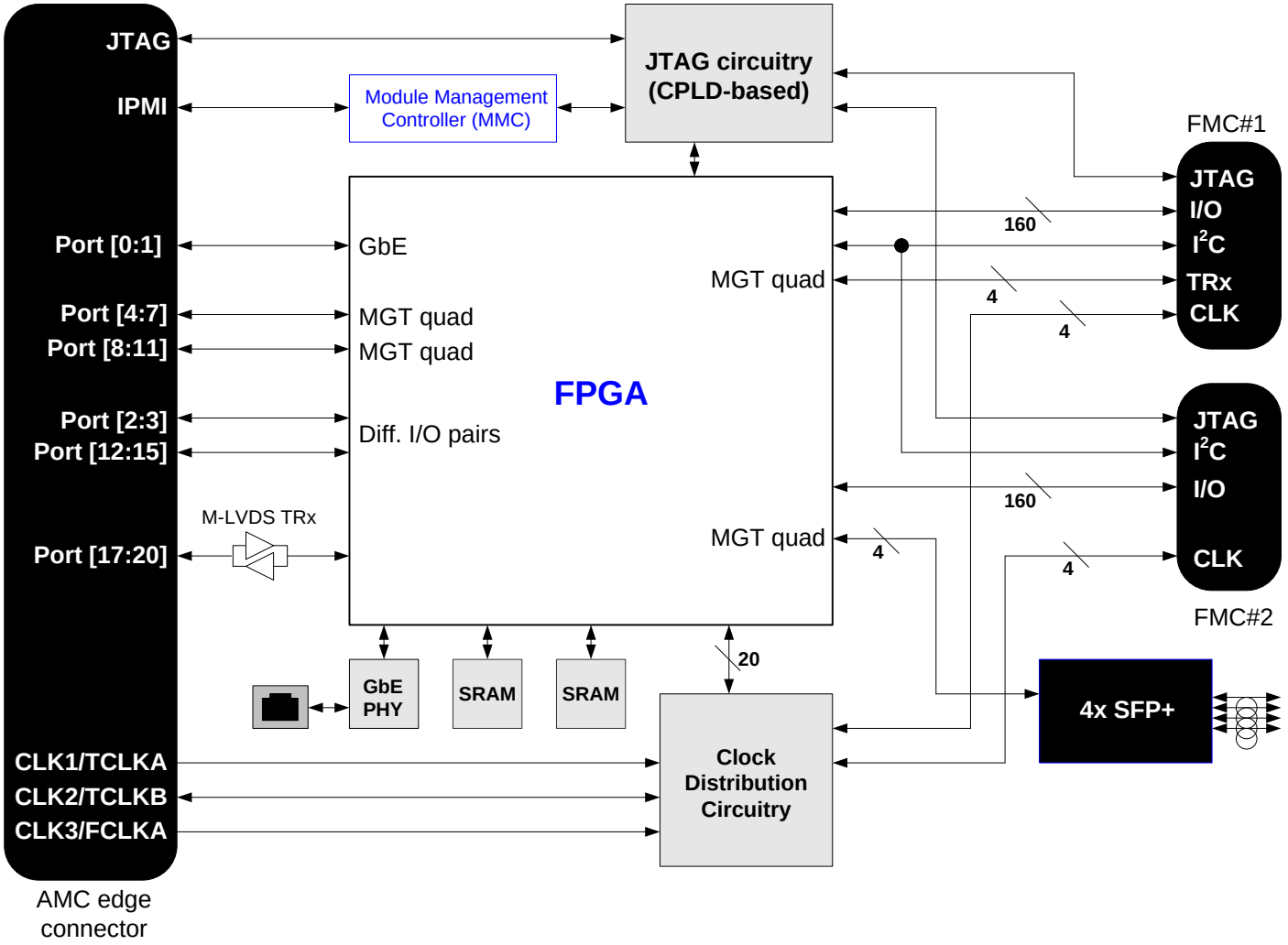
Crate system test setup



= E-LINK FMC = TTC FMC = SFP+

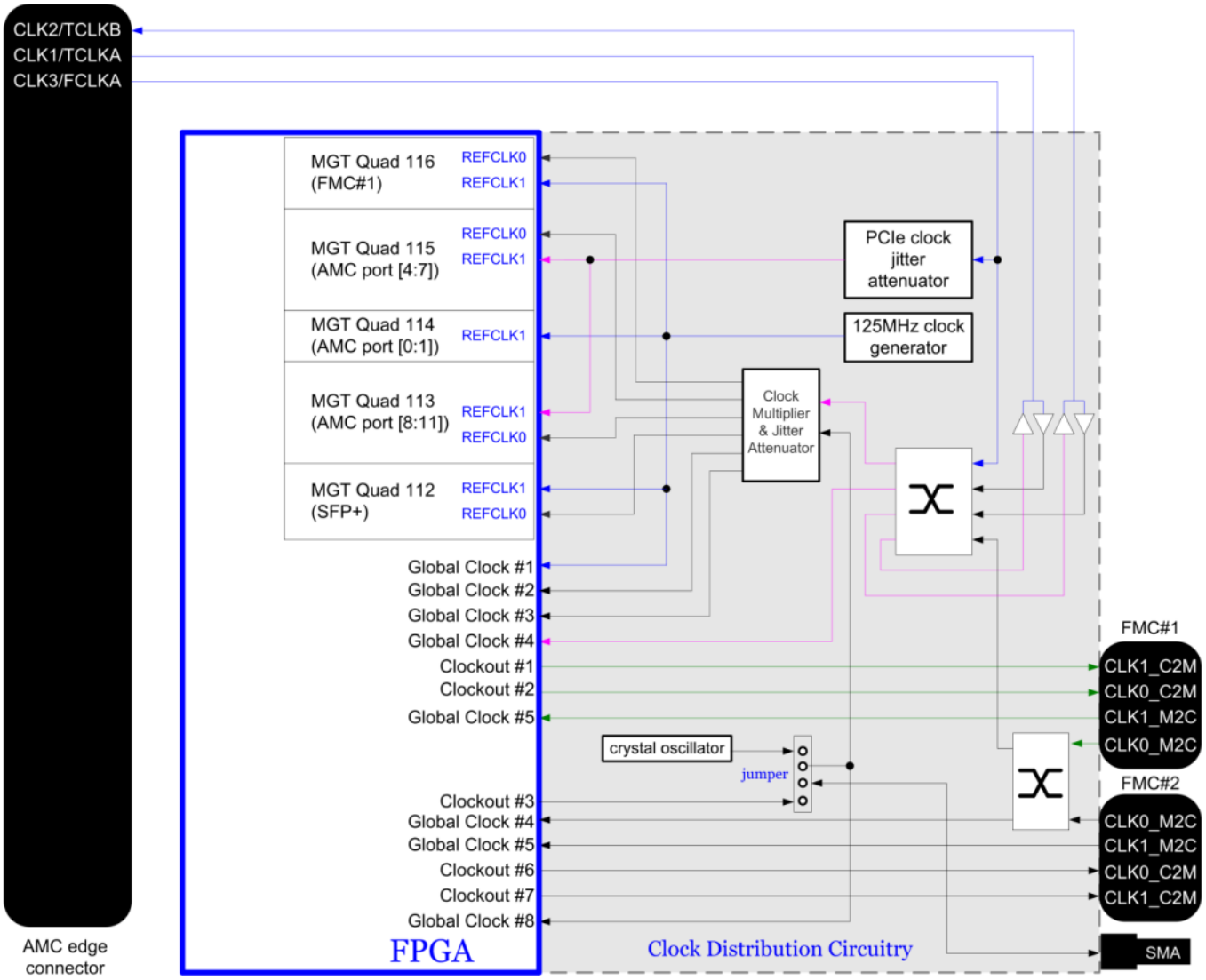
Hardware

ARCHITECTURE (1/2)



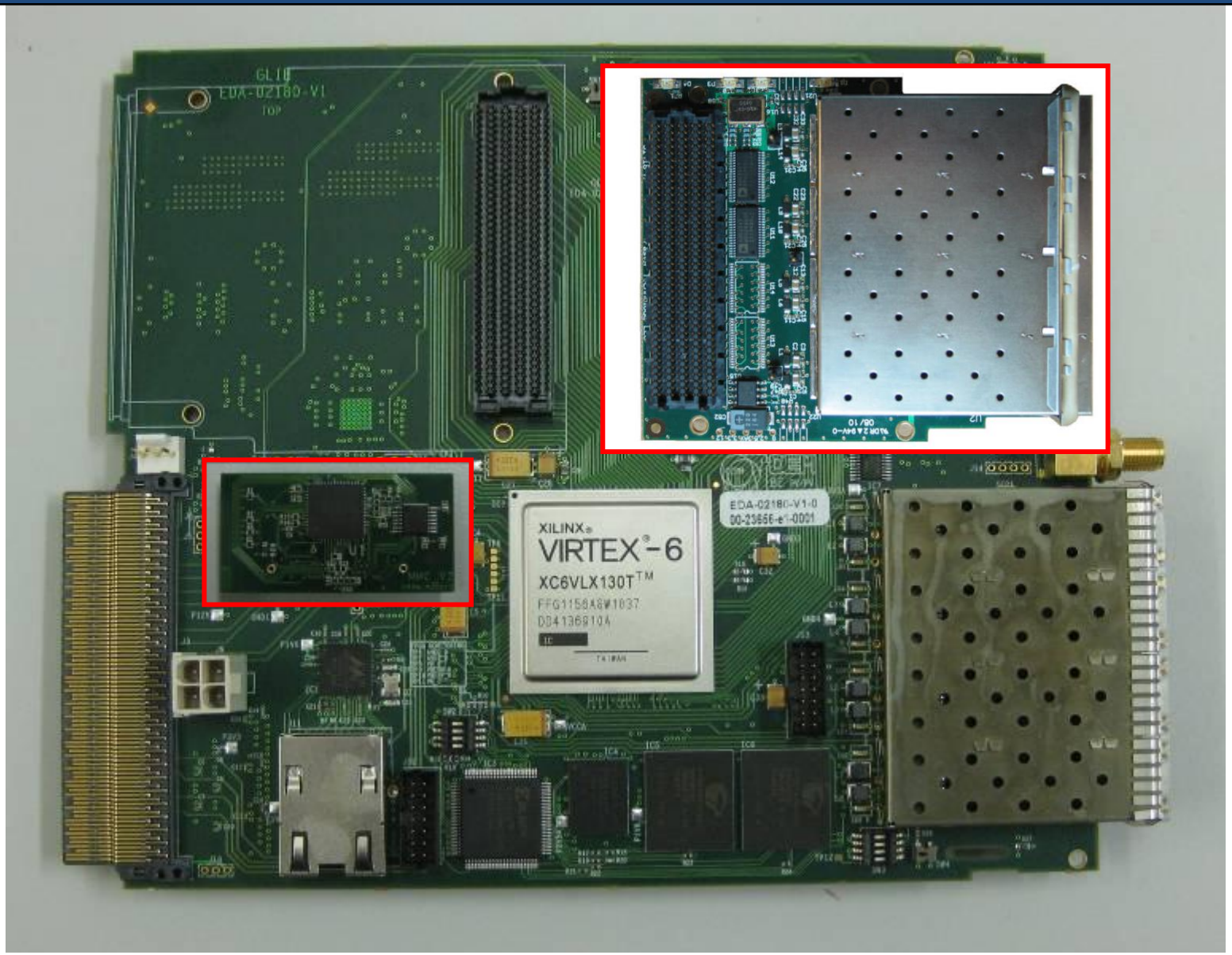
Hardware

ARCHITECTURE (2/2)



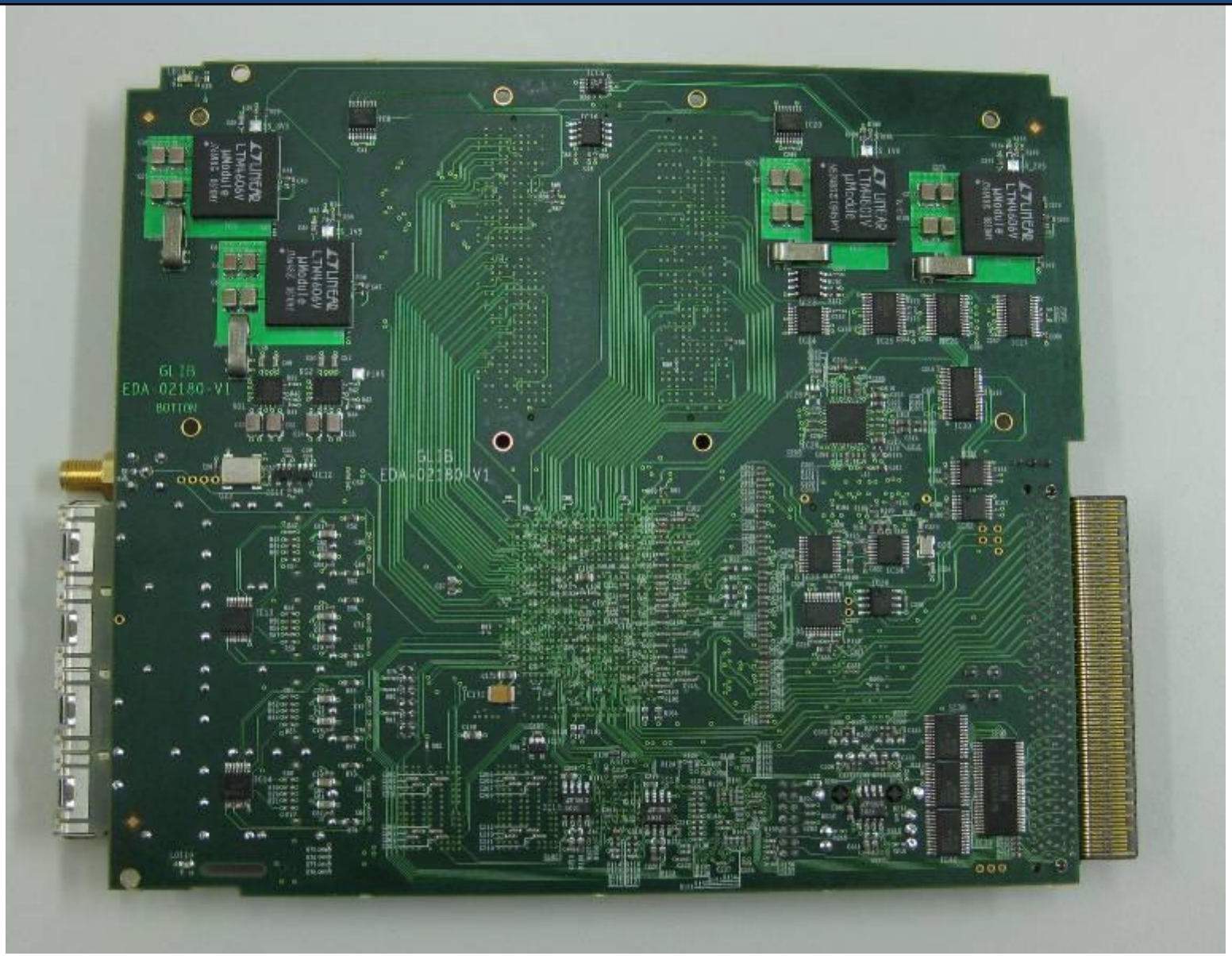
Hardware

FIRST PROTOTYPE (TOP VIEW)



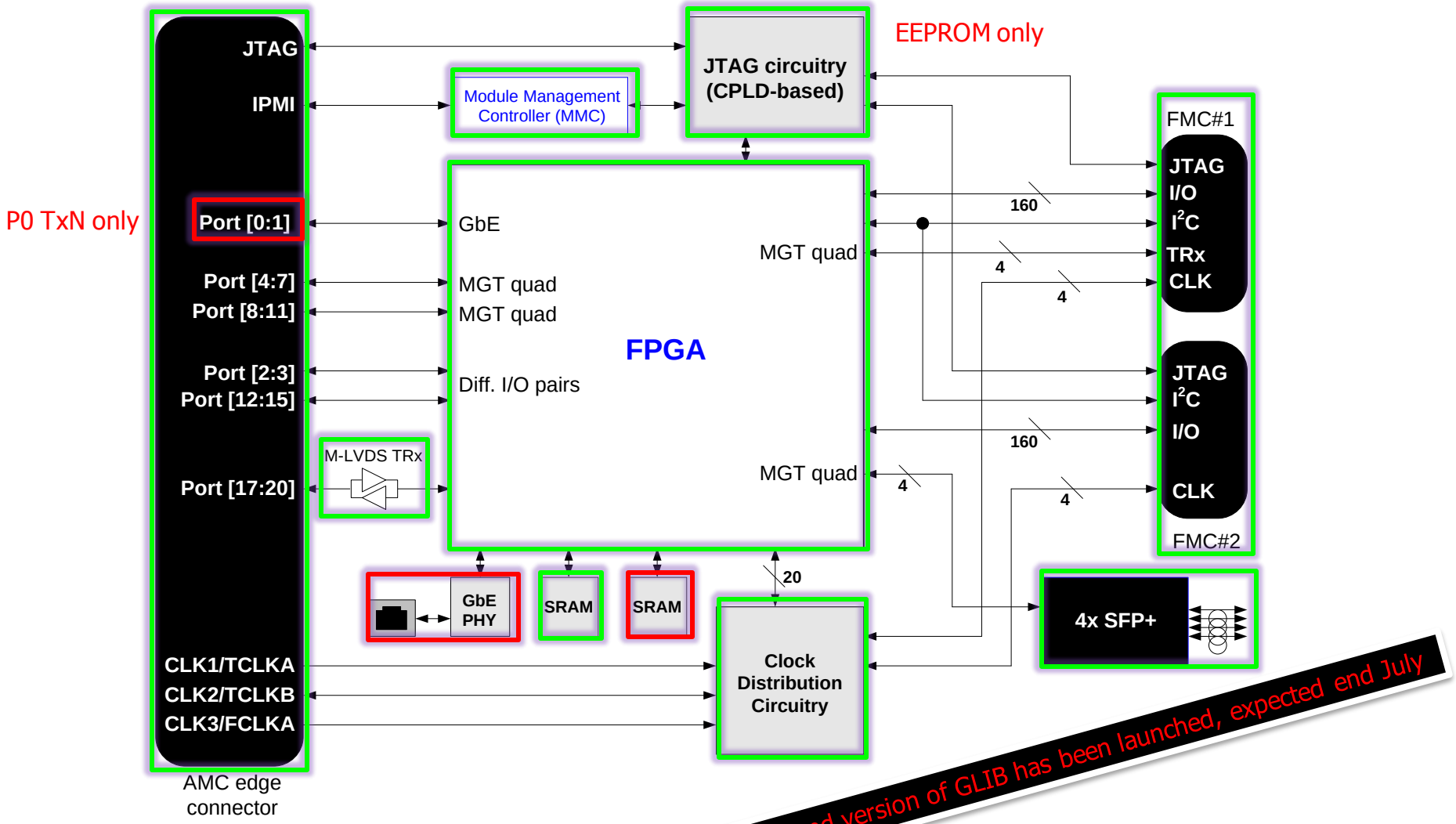
Hardware

FIRST PROTOTYPE (BOTTOM VIEW)



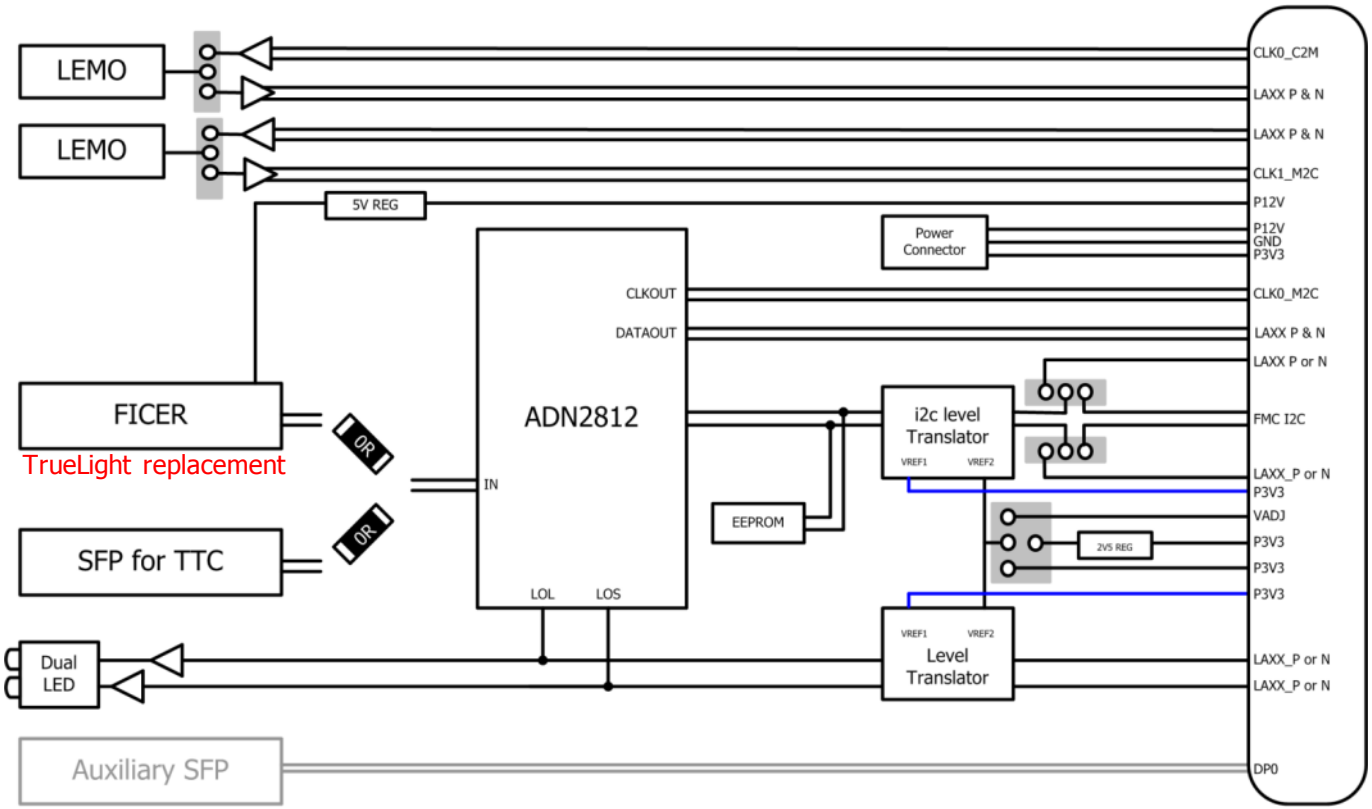
Hardware

FIRST PROTOTYPE TEST RESULTS

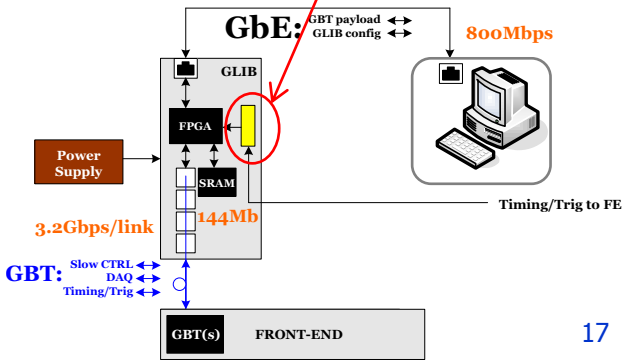


Mezzanine cards

TTC FMC ARCHITECTURE

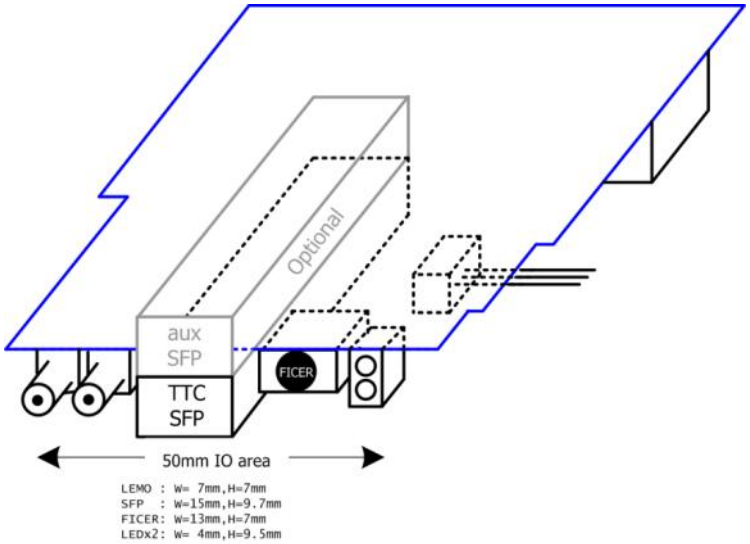


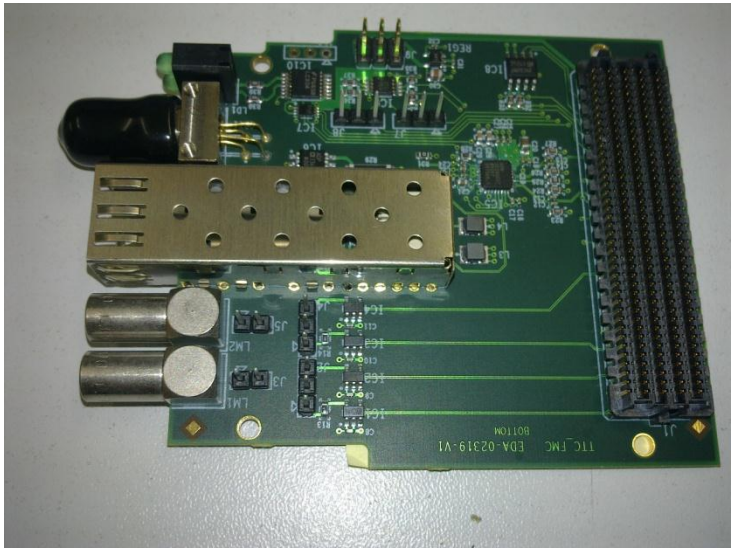
TTC FMC in bench-top beam test setup (Deliverable #1)



Mezzanine cards

TTC FMC IMPLEMENTATION





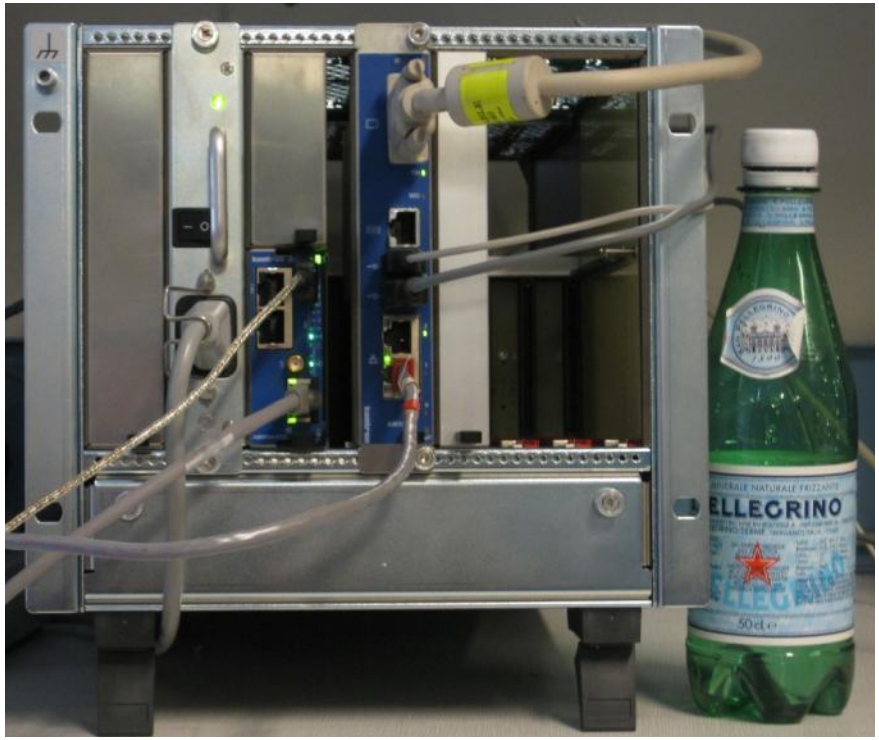
uTCA environment

INFRASTRUCTURE

Two different setups are available.

The setups include:

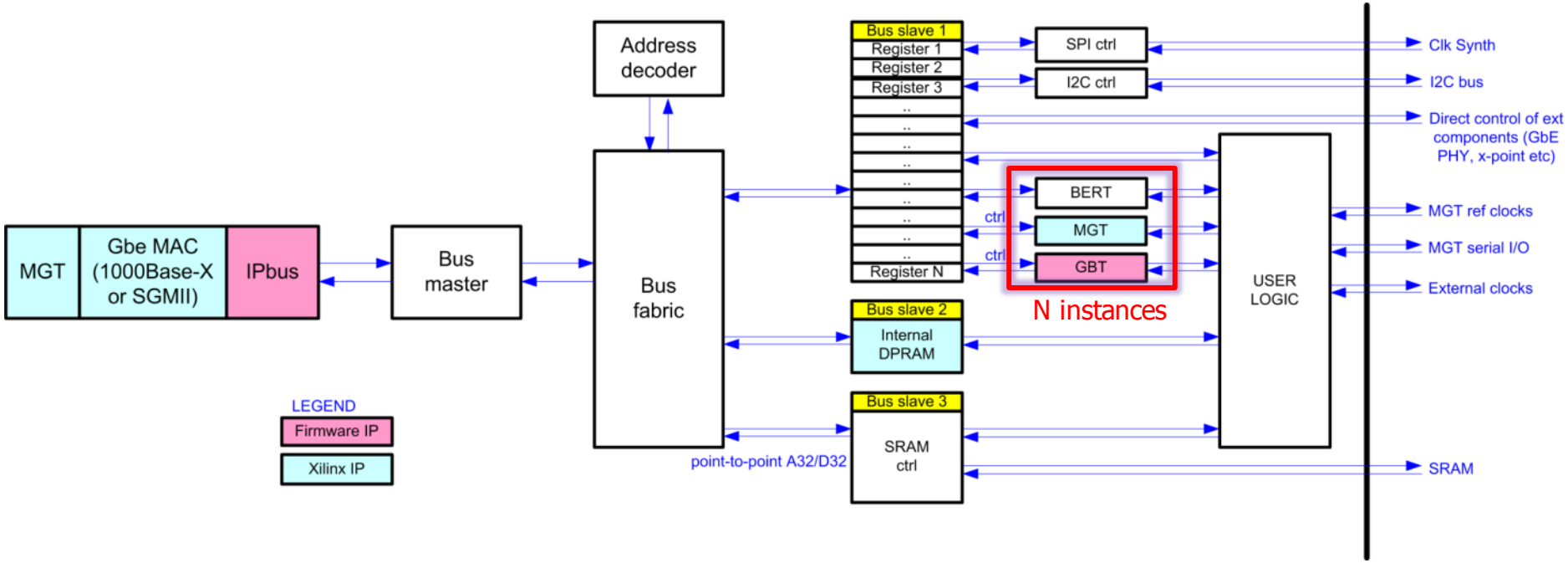
- Crate
- MCH
- Power supply
- CPU
- Commercial cards



The TCA infrastructure study became a different project "xTCA Evaluation Project" led by M. Joos

Firmware

TOP LEVEL



IPBUS firmware reference: Jeremiah Mans, "Ethernet HAL: firmware + Minnesota development status"
http://indico.cern.ch/getFile.py/access?contribId=5&sessionId=1&resId=0&materialId=slides&confId=90024

Software

STATUS

- Using the IPBUS software (Linux, C++, text mode)

  IPBUS software reference: Robert Frazier, "IP Bus (Ethernet HAL) Software"
  http://indico.cern.ch/getFile.py/access?contribId=6&sessionId=1&resId=0&materialId=slides&confId=90024

- Planning to develop a Graphical Users Interface (GUI) for the IPBUS
  - Based on Java
  - A draft specification is available
  - A technical student will work on it starting for July (under the supervision of M. Joos)
  - Already some progress

SUMMARY

- GLIB v1 available, GLIB v2 expected end July.
- Selected advanced users will possibly get a GLIB v2 before end 2011 to help with development
  - Planning to deliver GLIB cards to other users sometime in 2012
- Firmware for Bench-top test beam setup (Deliverable #1) is good state – still to test with GBT
  - Huge effort by M. Barros Marin (technical student) in GLIB firmware
  - Excellent collaboration with the GBT-FPGA team
- Software development on going
  - Excellent collaboration with Bristol University
  - Starting from July, a technical student will work with Markus for the IPBUS Graphical Users interface in Java
- TTC FMC first prototype ready (part of the Deliverable #1), firmware based on E. Hazen (Boston)
- TCA infrastructure available
  - Thanks to M. Joos, V. Bobillier & J.P. Cachemiche (CPPM)
- Detailed results will be presented in TWEPP 2011
- Development of the Deliverables #2 & #3 will follow

GLIB LINKS

https://edms.cern.ch/nav/EDA-02180-V2-0

specs from GLIB website

GLIB at OHR

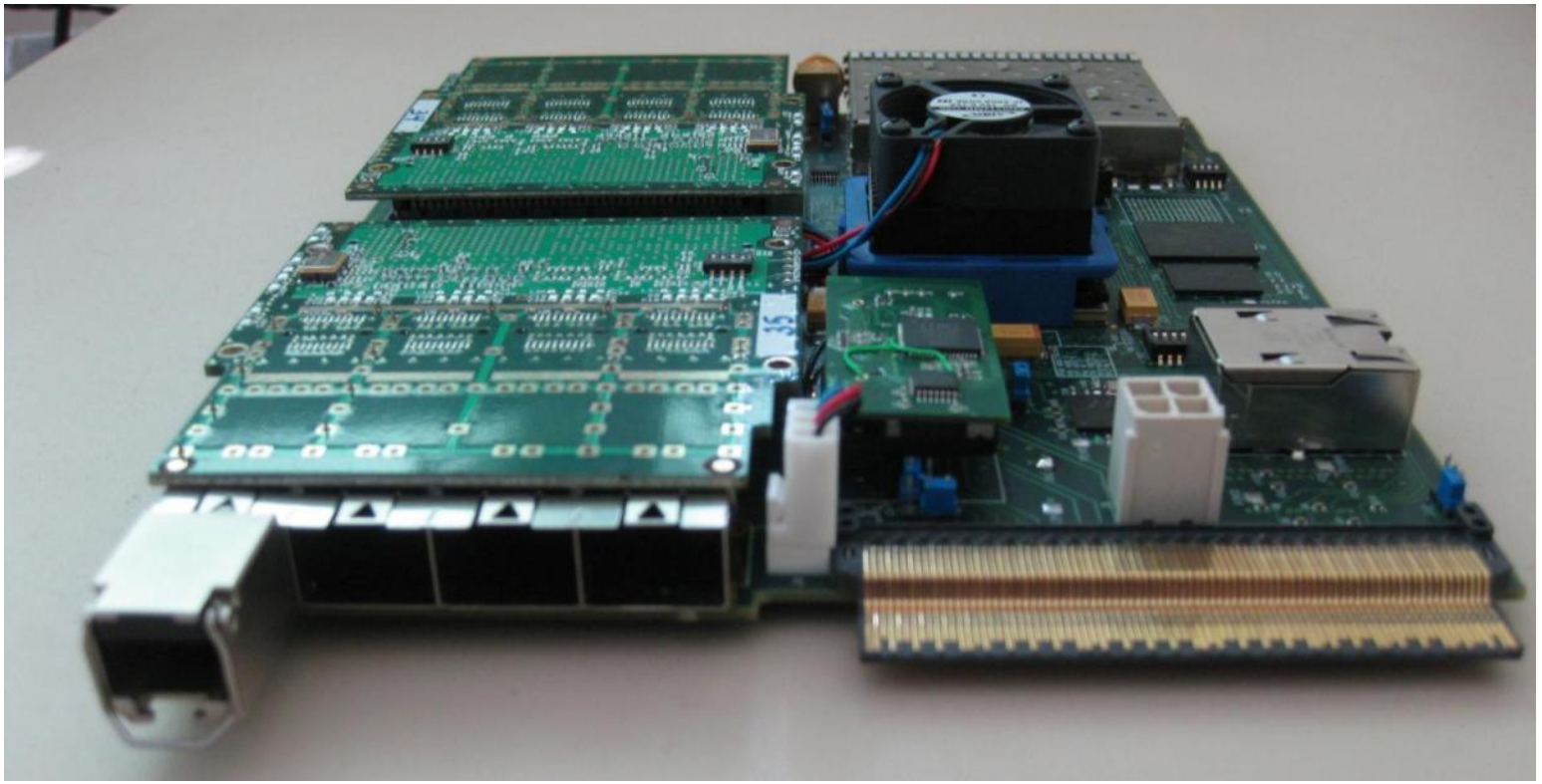

END

BACKUP SLIDES

Firmware

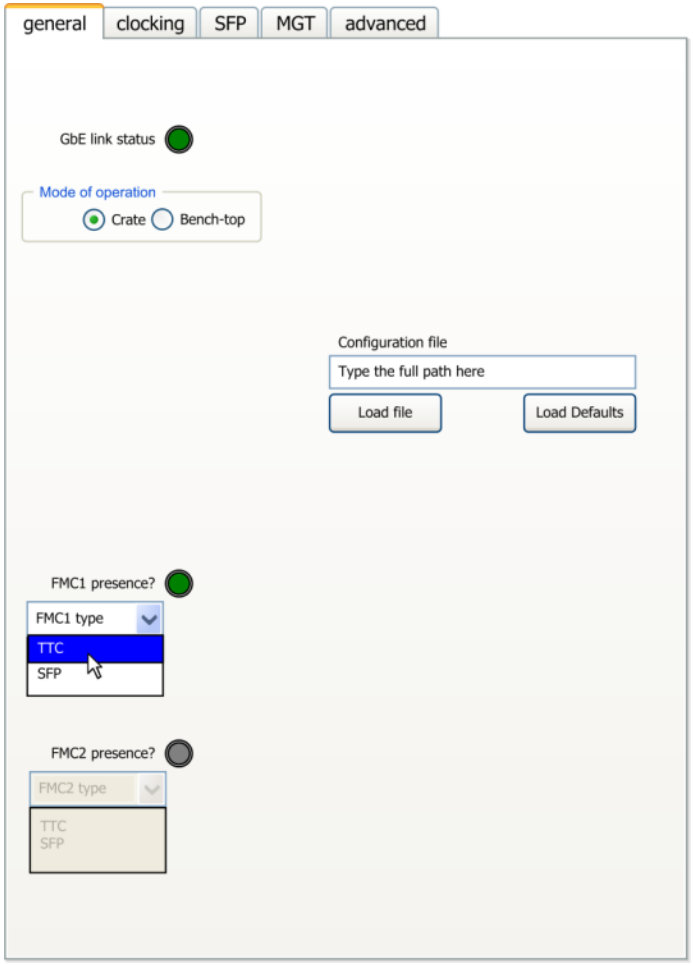
TEST OF FIRMWARE EXAMPLE#1

A reserved MGT channel in FMC#2 is used as the GbE link (since the PHY of GLIB v1 fails)



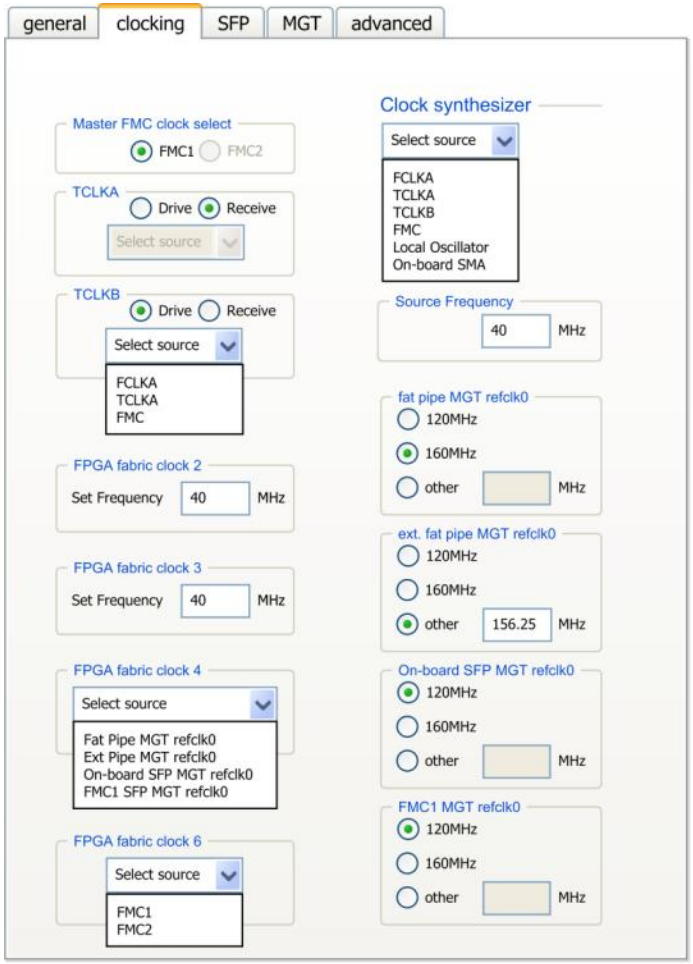
Software

Graphical Users Interface concept (1/3)



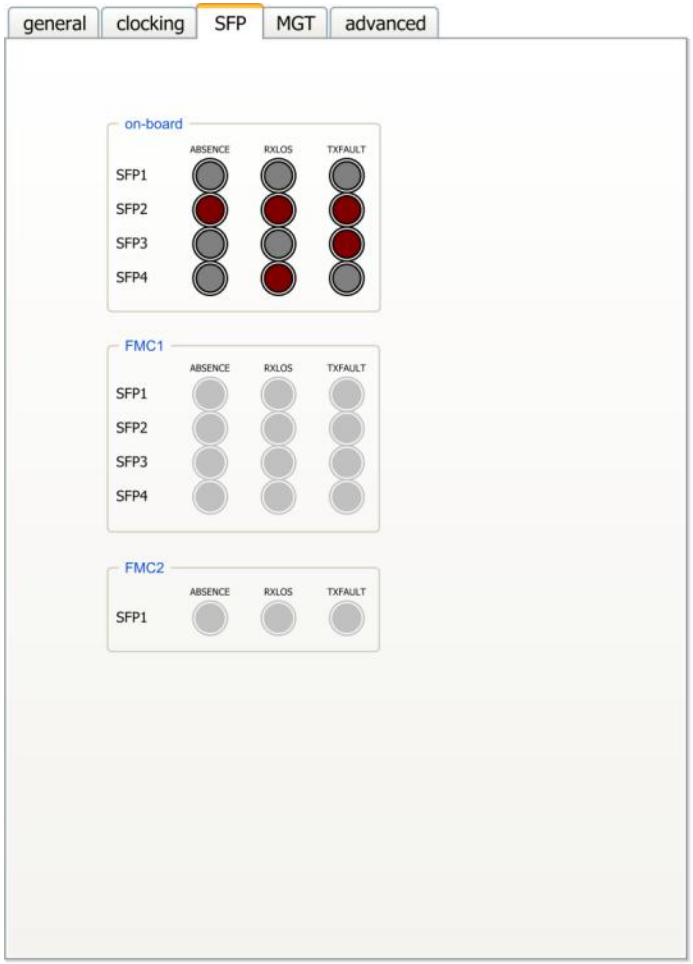
Software

Graphical Users Interface concept (2/3)



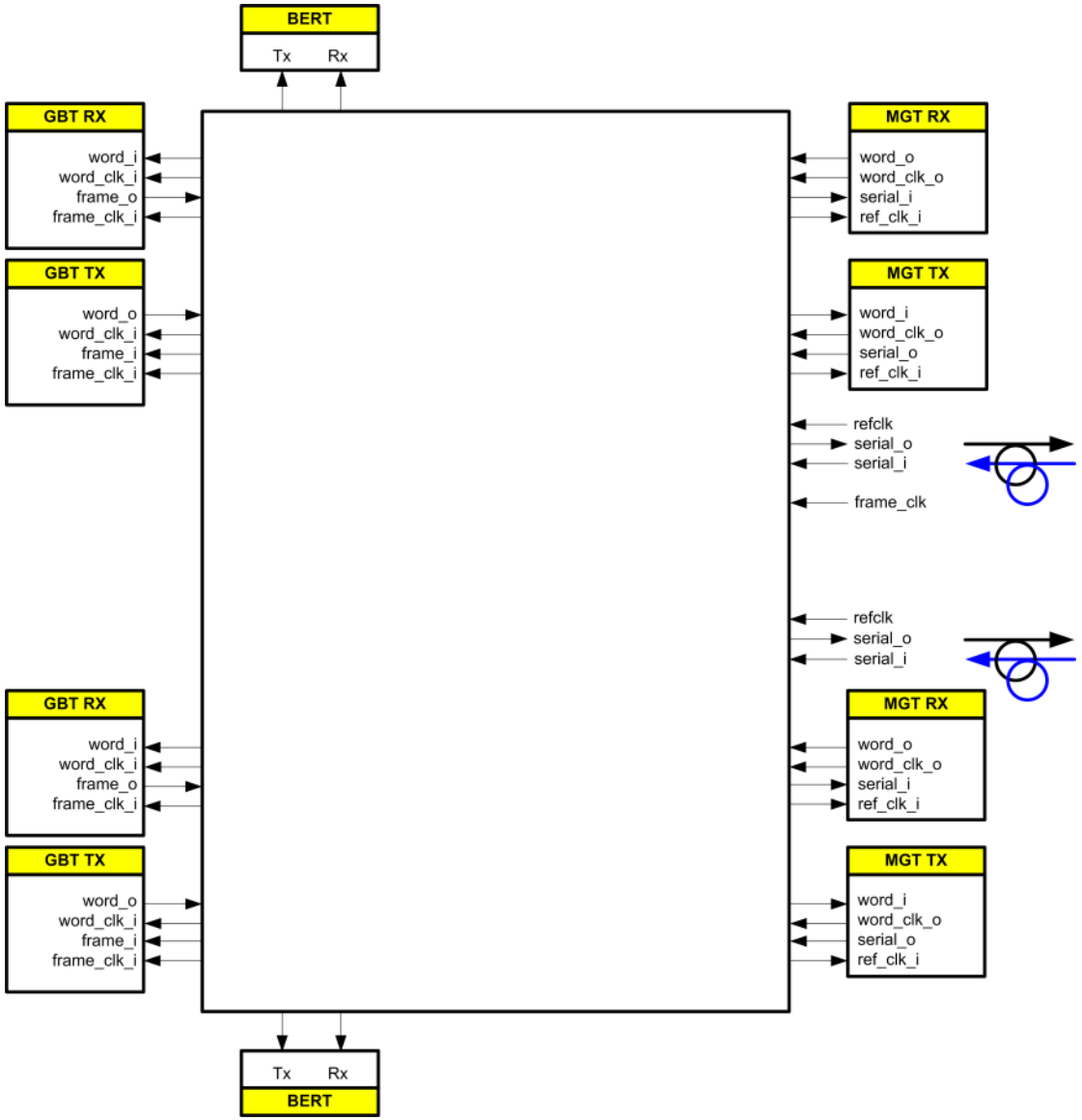
Software

Graphical Users Interface concept (3/3)



Firmware

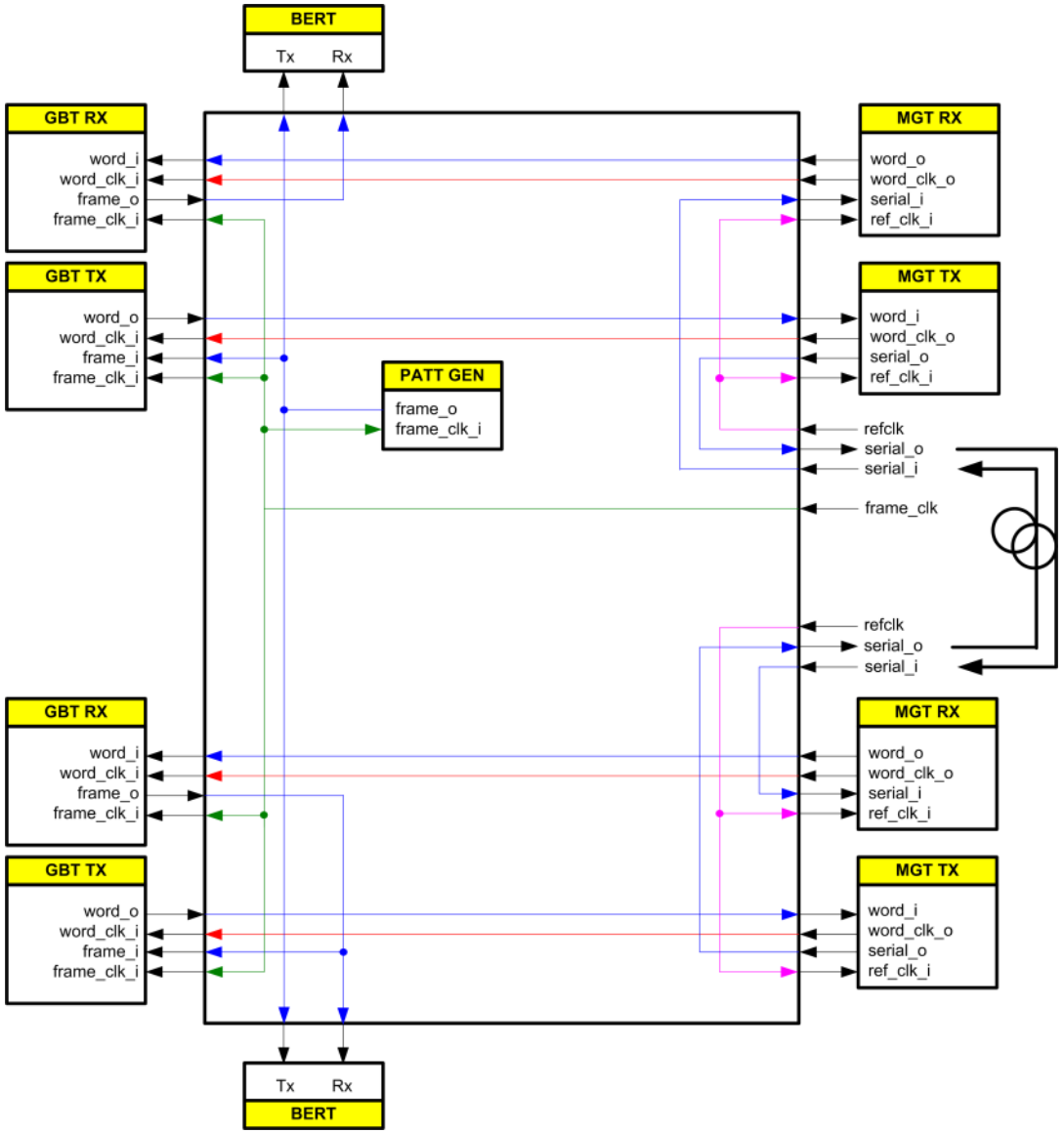
USER LOGIC ARCHITECTURE (for N=2)



LEGEND
Frame = 84bit
word = 40bit

Firmware

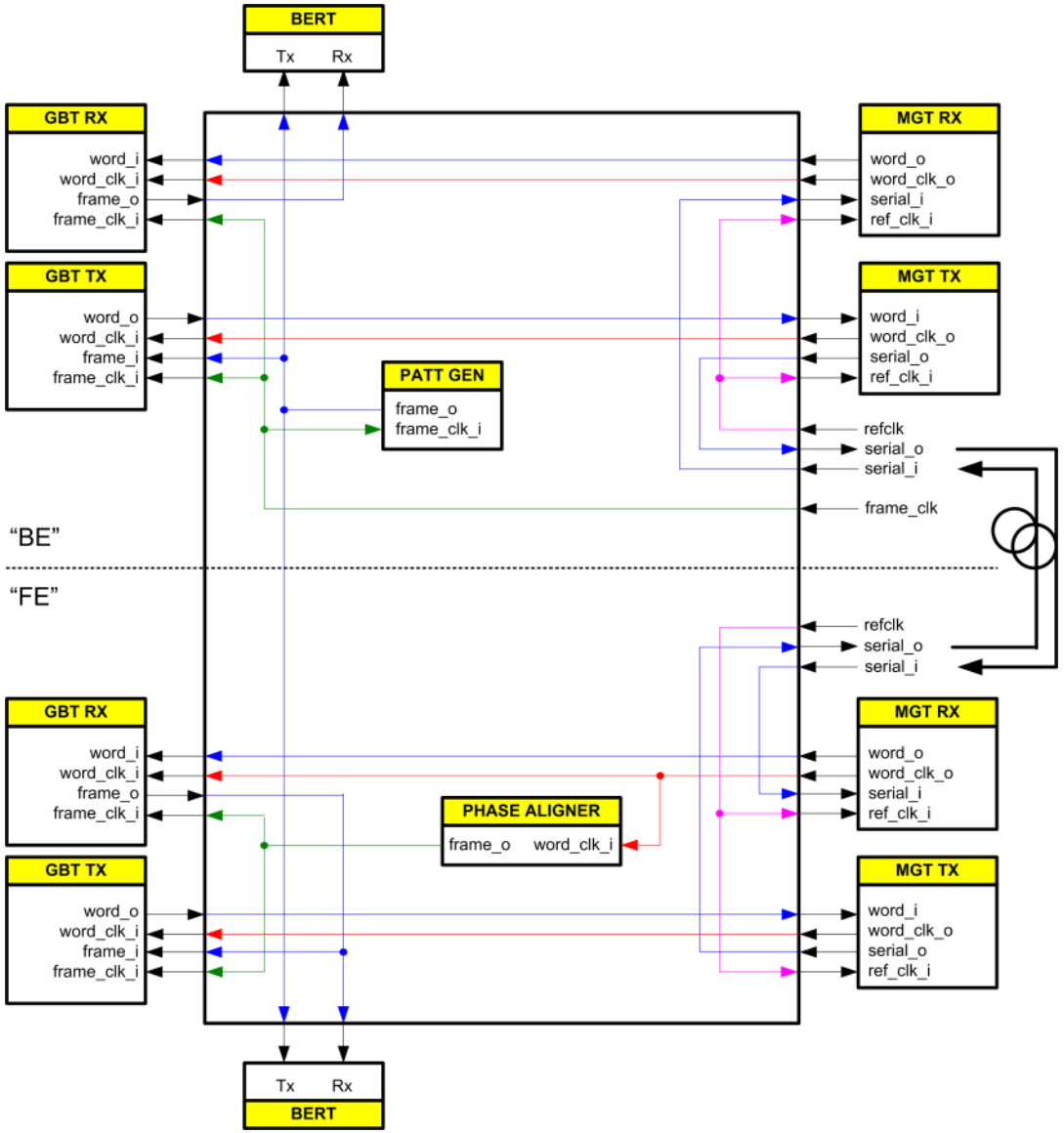
USER LOGIC EXAMPLE #1



LEGEND
Frame = 84bit
word = 40bit

Firmware

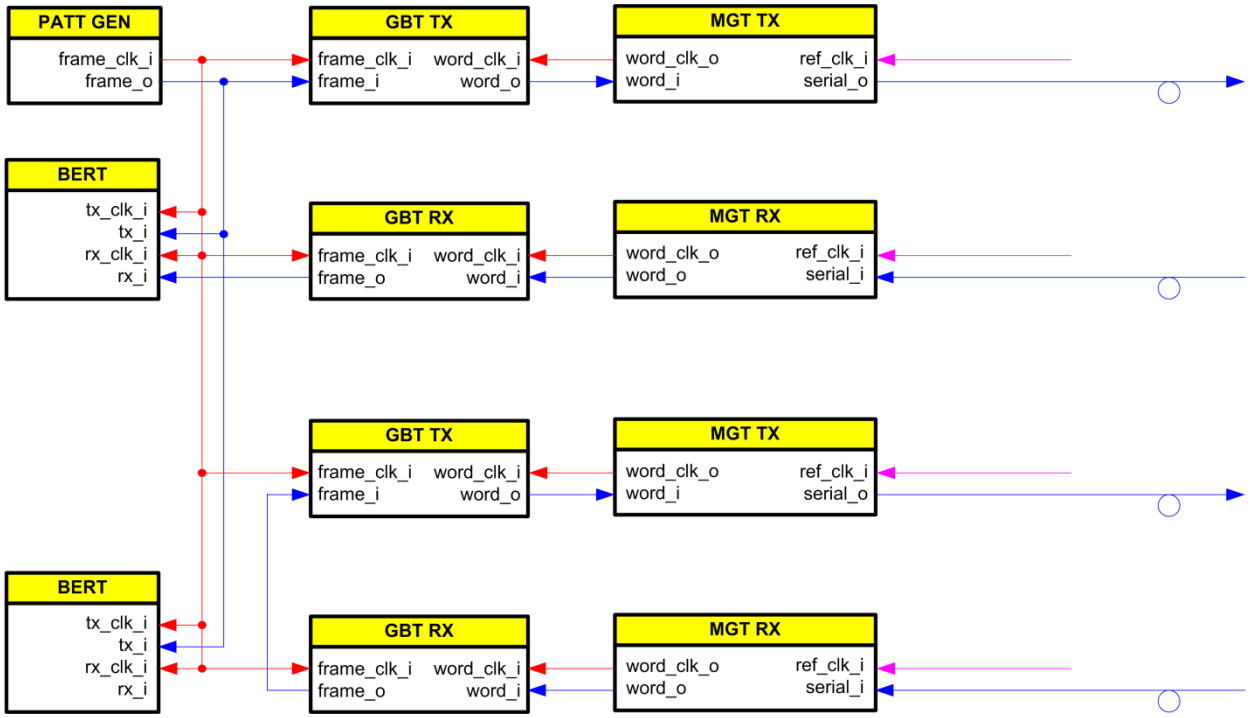
USER LOGIC EXAMPLE #2



LEGEND
Frame = 84bit
word = 40bit

Firmware

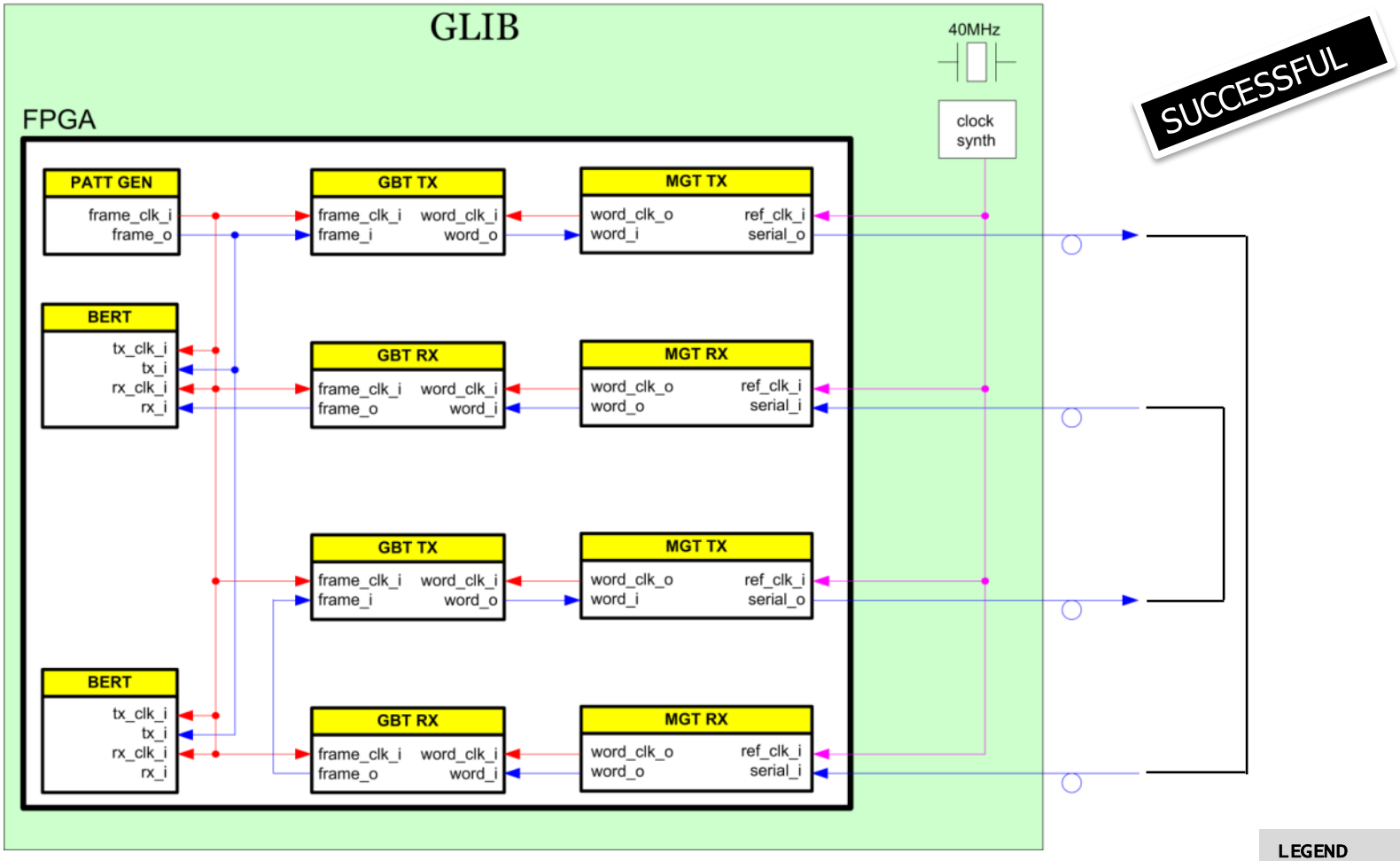
USER LOGIC EXAMPLE #1 (SIMPLIFIED)



LEGEND
Frame = 84bit
word = 40bit

Firmware

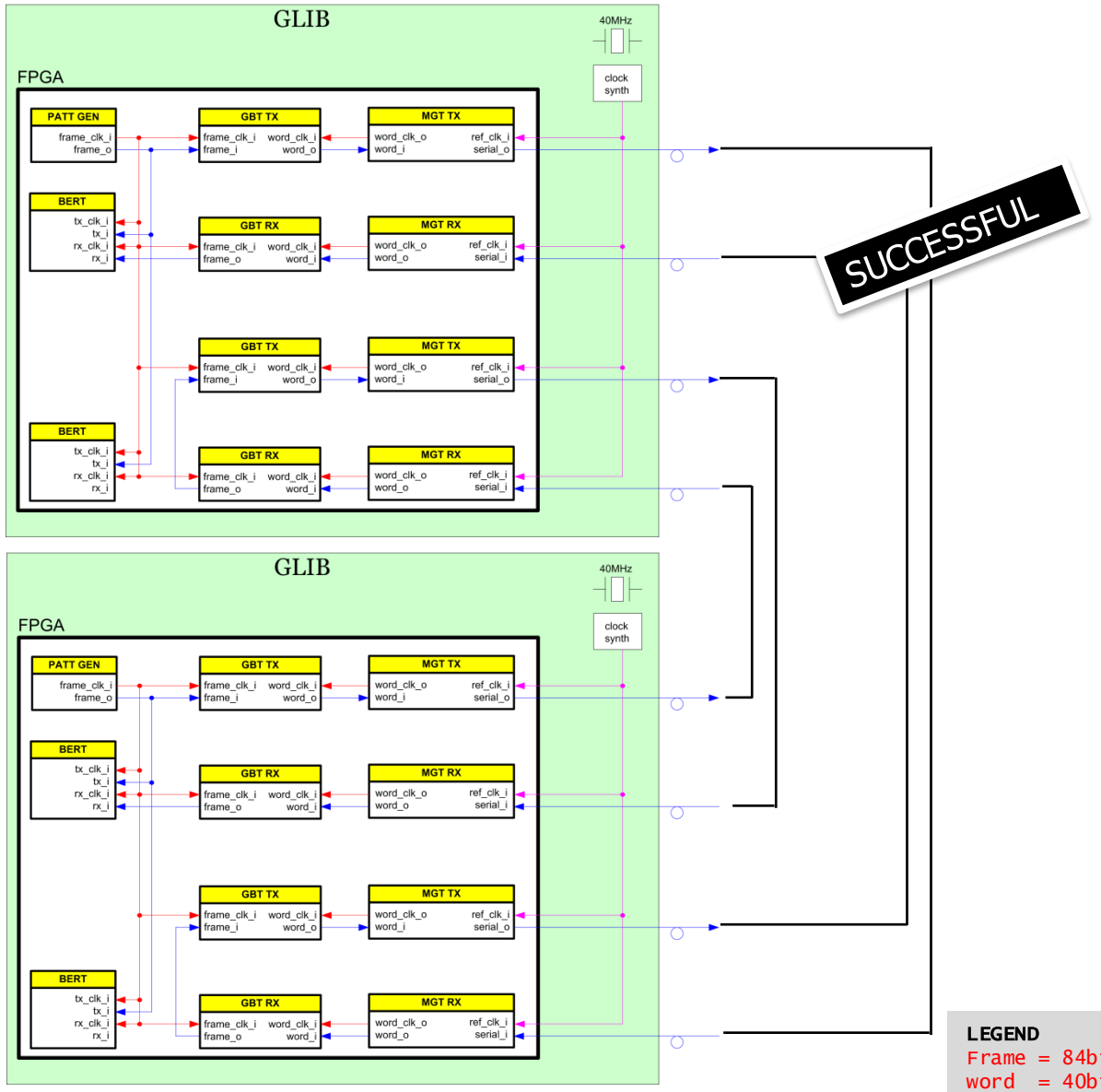
TEST OF FIRMWARE EXAMPLE#1 (1/2)



LEGEND
Frame = 84bit
word = 40bit

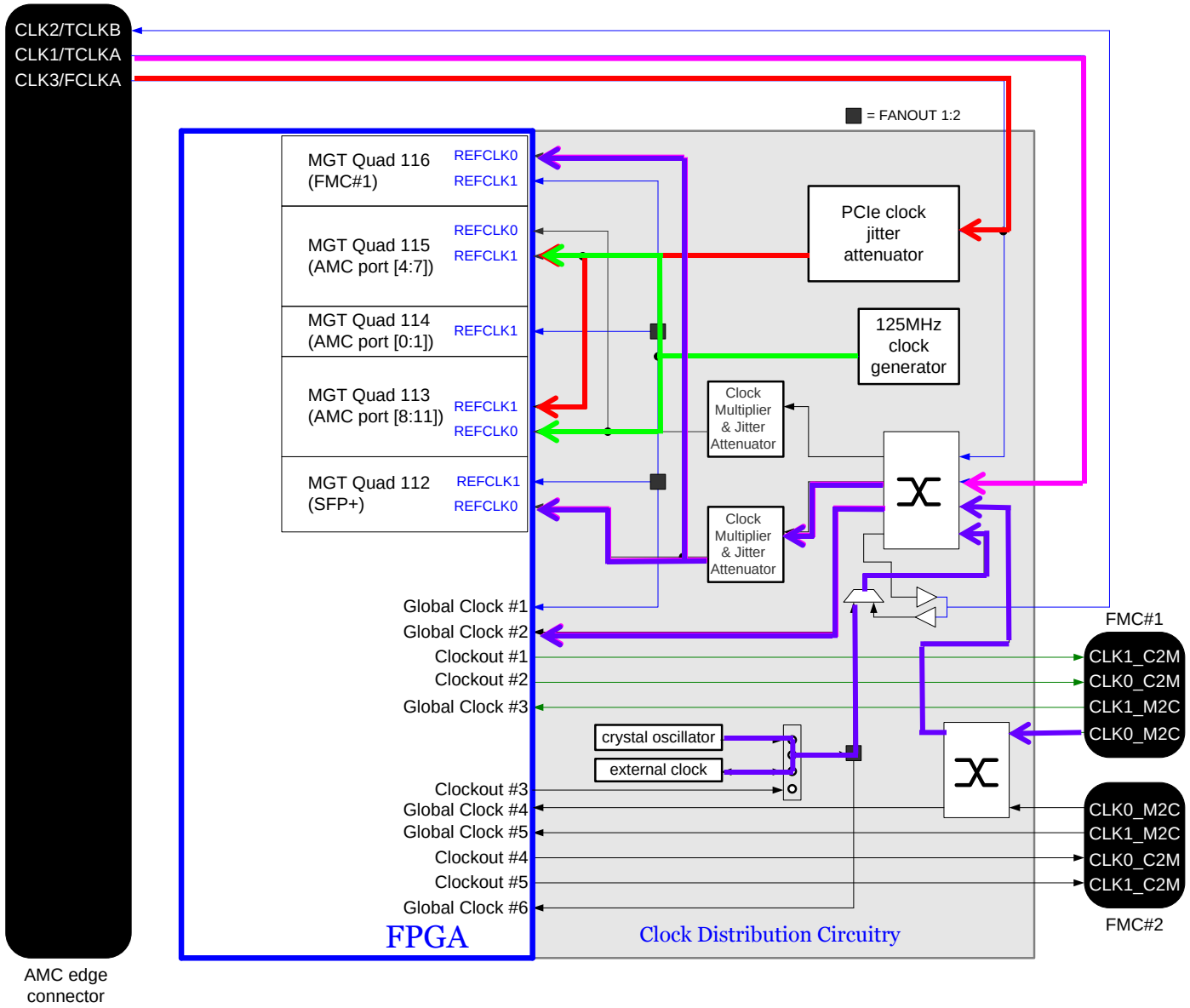
Firmware

TEST OF FIRMWARE EXAMPLE#1 (2/2)



Implementation

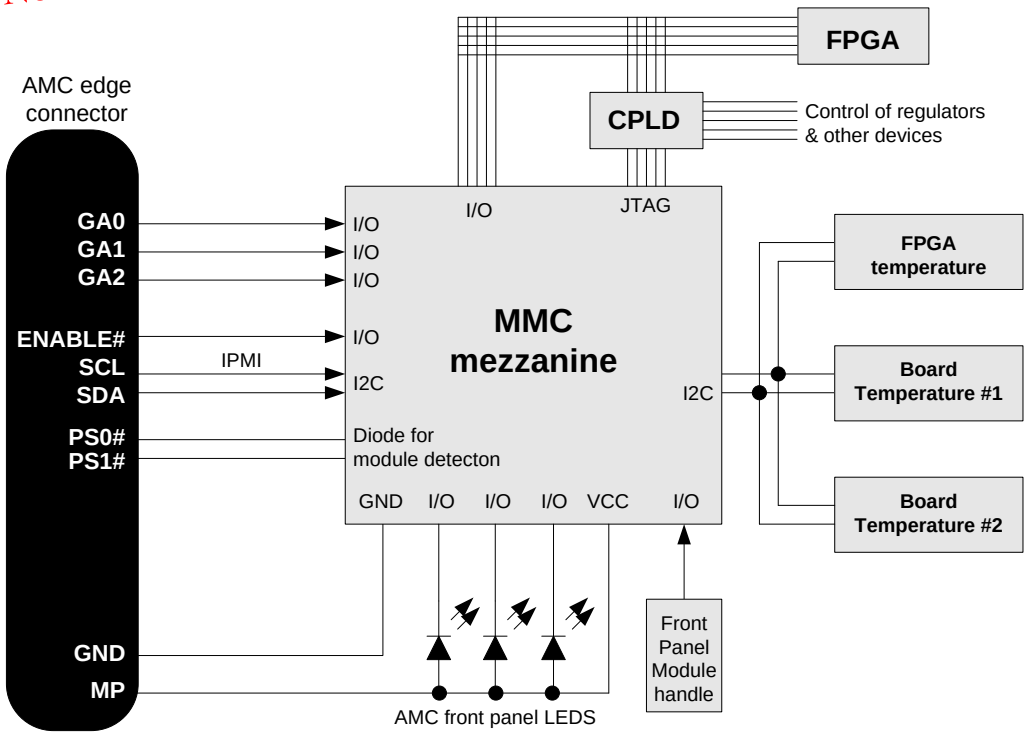
CLOCK DISTRIBUTION



Implementation

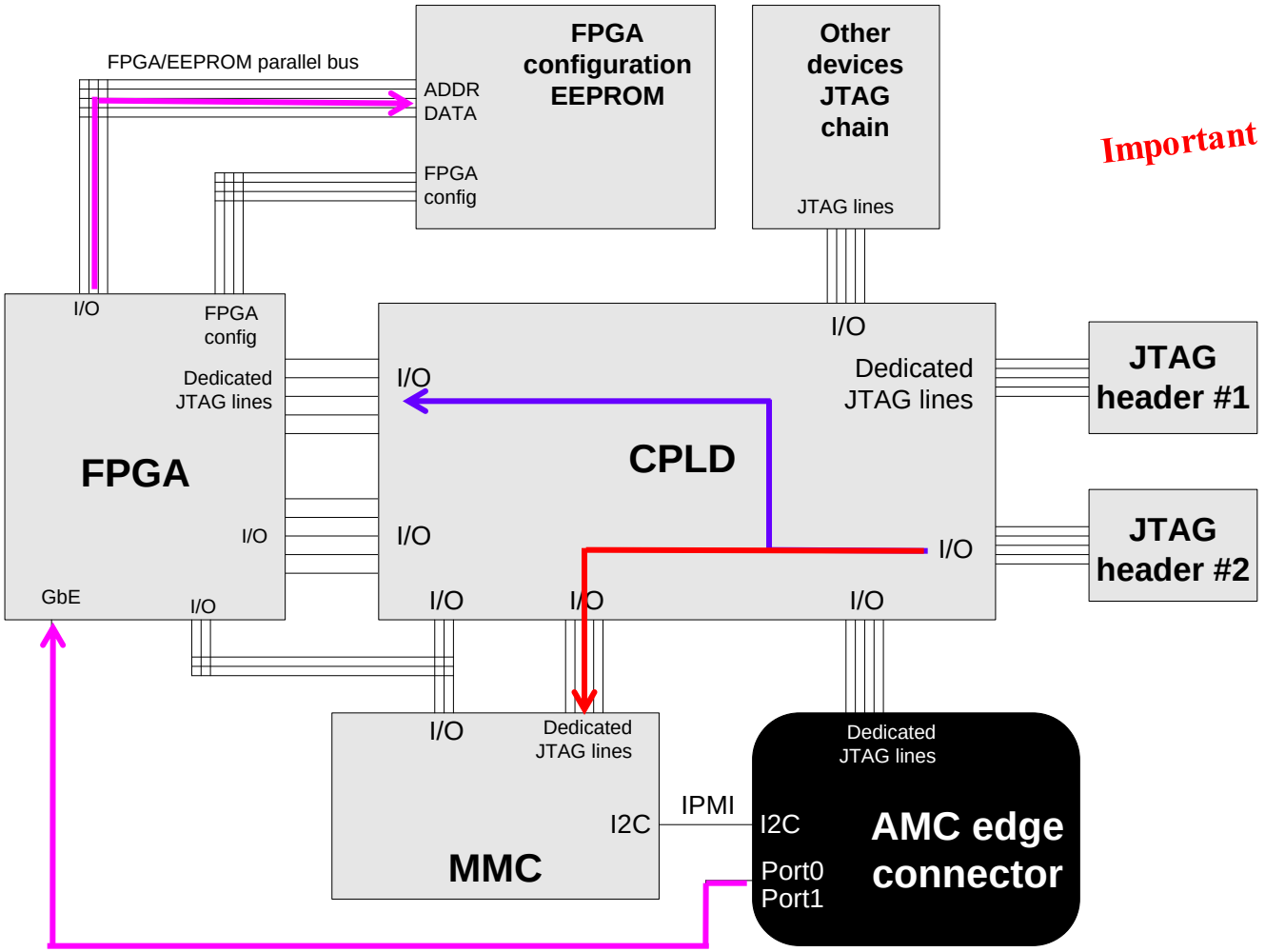
MODULE MANAGEMENT CONTROLLER

Note: Not required for bench-top applications



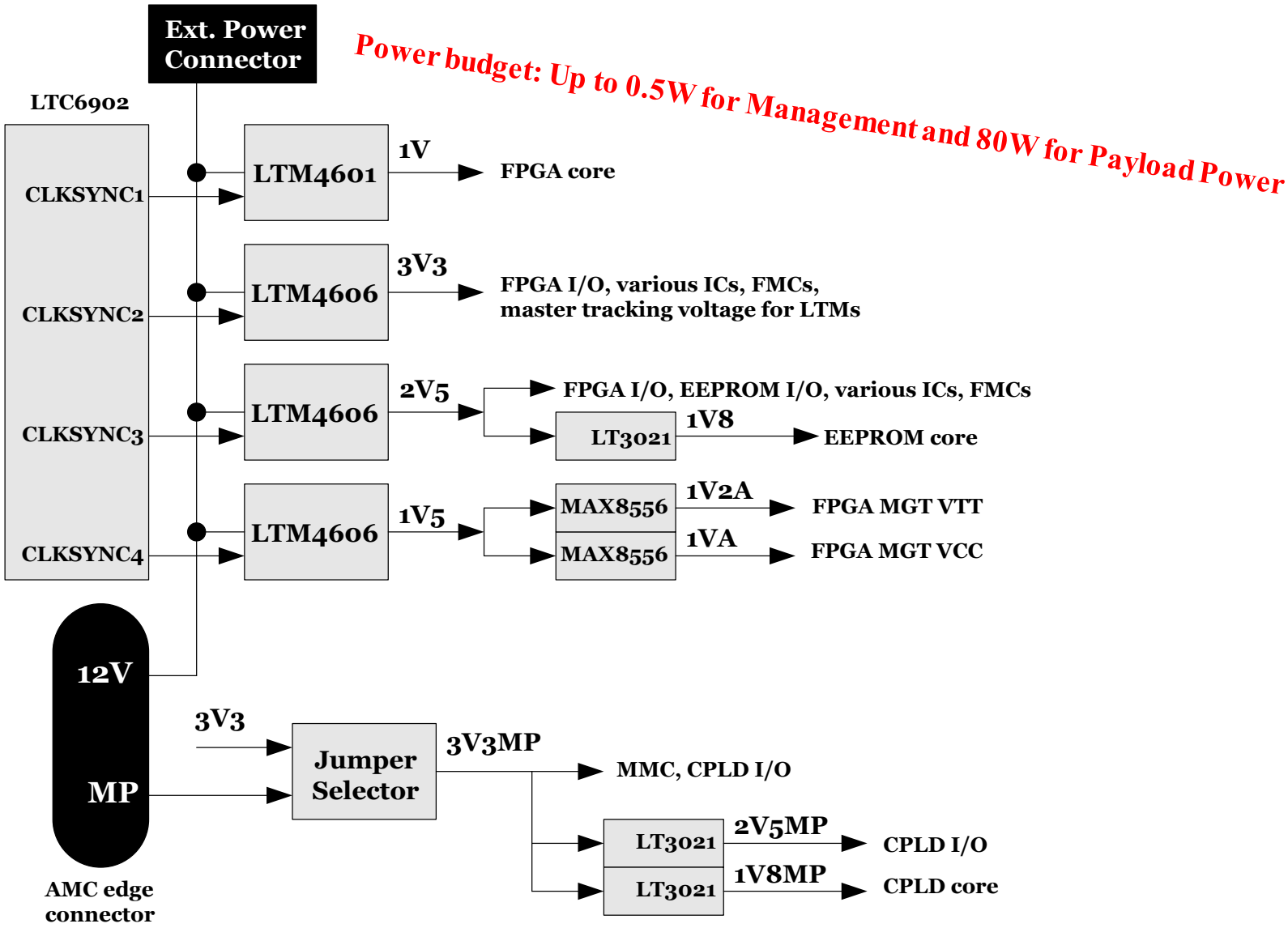
Implementation

JTAG CIRCUITRY



Implementation

POWERING



Implementation

POSSIBLE FMC IMPLEMENTATIONS