# Analog FE: ASIC

## Upgrade of the front end electronics of the LHCb calorimeter

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**ICC-UB,URL,LAL**

LHCb upgrade electronics – CERN – July 21th 2011

# Outlook

I. Introduction

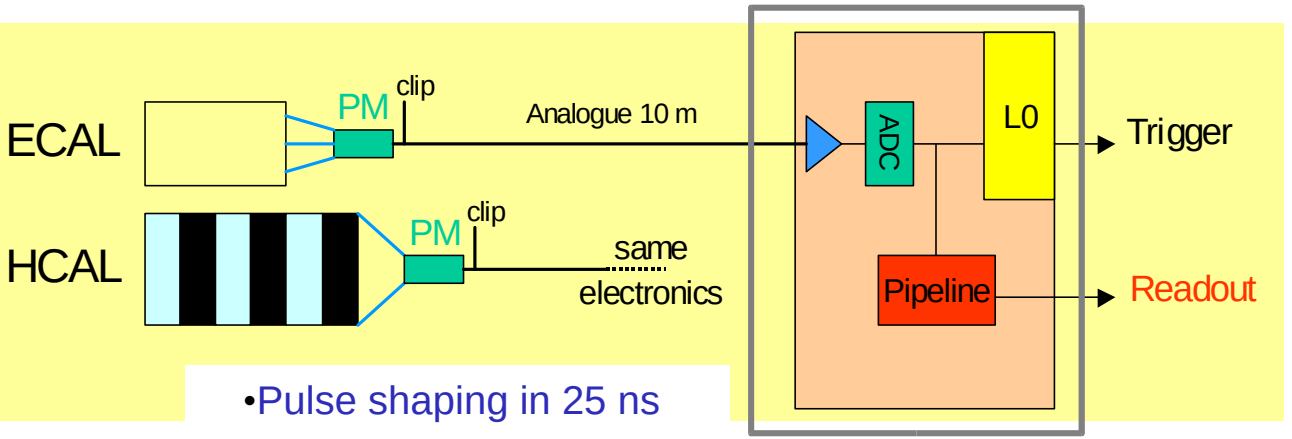
II. Input stage

III. Channel architecture

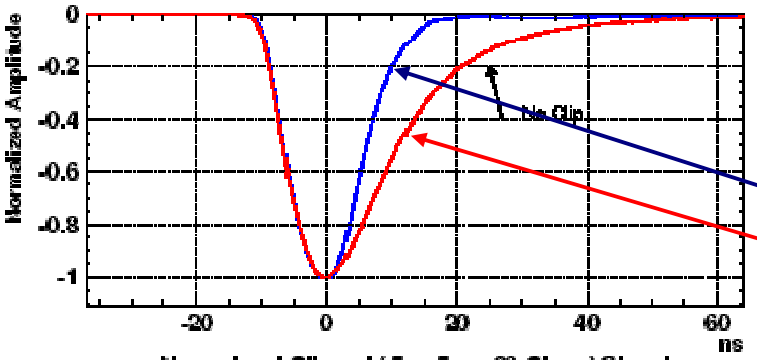
IV. Technology

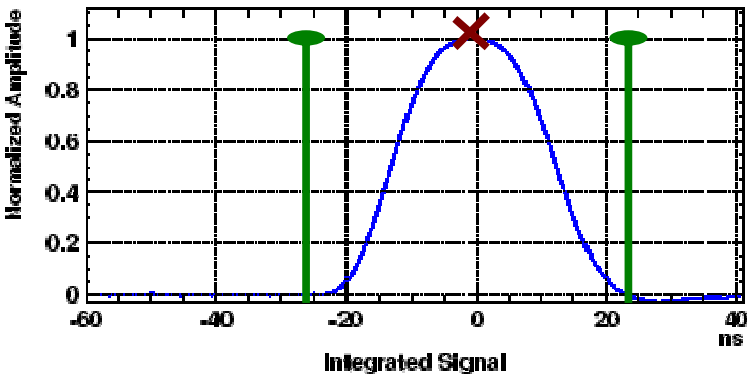
# I. Introduction: current ECAL/HCAL FE

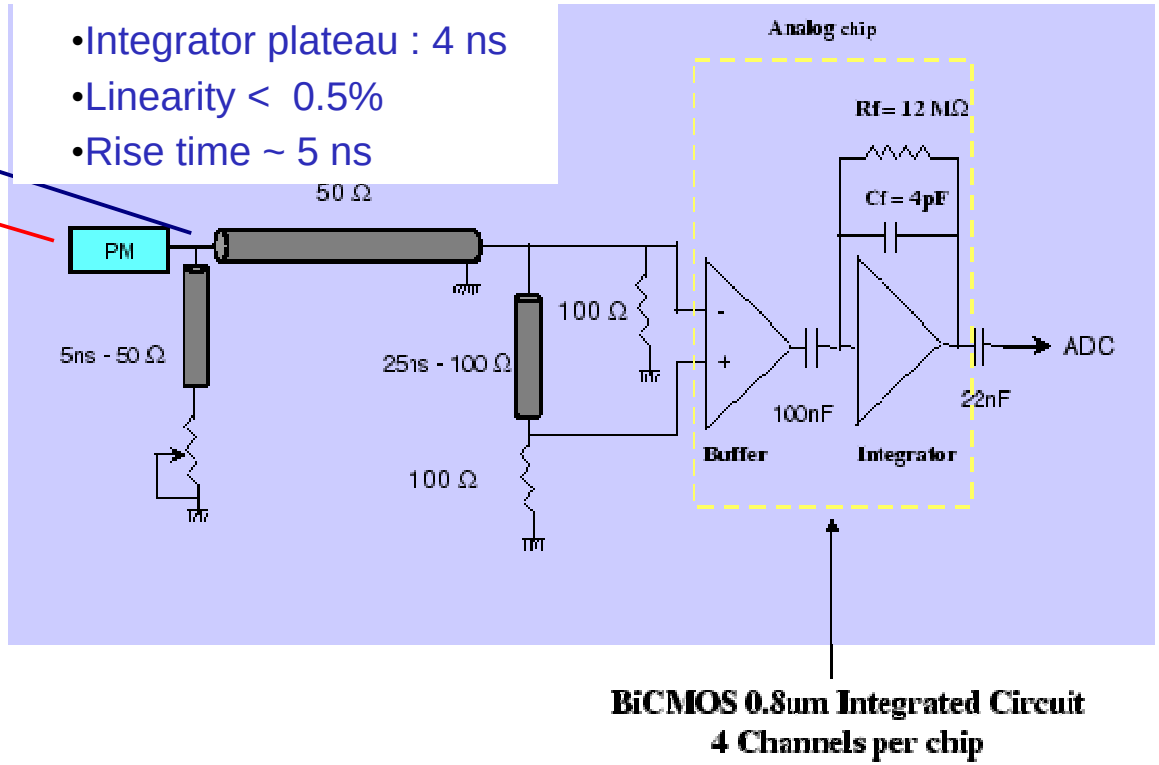
LAL-Orsay




- Pulse shaping in 25 ns
- Residue < 1% after 25 ns
- Integrator plateau : 4 ns
- Linearity < 0.5%
- Rise time ~ 5 ns



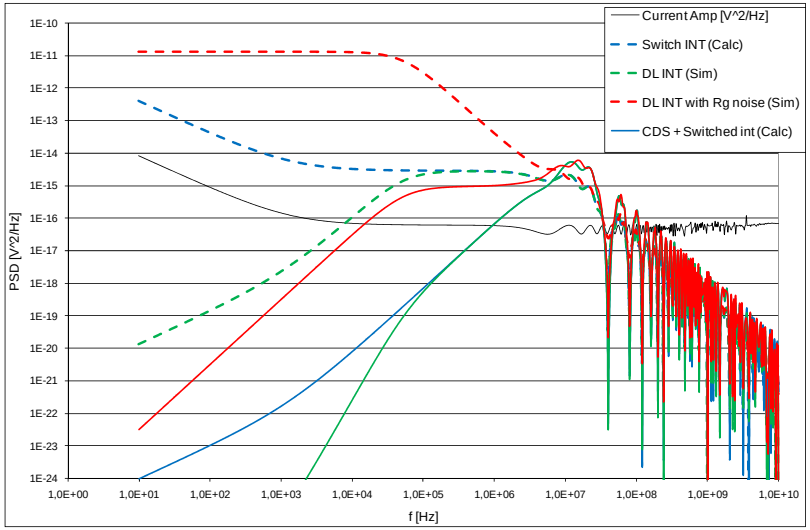



# I. Introduction: motivation and task sharing

- PM current has to be reduced
  - Otherwise PMT would die rapidly (require a factor ~ 5)
  - FE electronics gain has to be increased correspondingly
  - FE noise should not be increased in the operation !
- New front end board is required:
  - Low noise analog electronics
  - GBT for data transmission @ 40MHz
    - *Digital development @ LAL (Frédéric's talk)*
- For 12 bit DR, input referred noise:
  - Voltage amplifier: < 1 nV/sqrt(Hz)
  - Current amplifier: < 10 pA/sqrt(Hz)
  - Active cooled termination required:
    - *ASIC development @ UB (Edu's and this talks)*
- But 2/3 of the signal are lost by clipping:
  - Alternative solution: remove clipping at the PM base (detector)
  - Perform clipping after amplification in FE
  - Alternative analog COTS + delay line solution
    - *COTS development @ URL (Carlos' talk)*

**See talk noise in June 2009 meeting:**

http://indico.cern.ch/materialDisplay.py?contribId=1&sessionId=0&materialId=slides&confId=59892




**This talk considers single ended implementation, results should be scaled by xsqrt(2)**

# I. Introduction: requirements

- Requirements (LOI):

| | Value | Comments |
|---|---|---|
| **Energy range** | 0-10 GeV/c (ECAL)<br>Transverse energy | 1-3 Kphe / GeV<br>Total energy |
| **Calibration** | 4 fC /2.5 MeV / ADC cnt | 4 fC input of FE card: assuming 25 Ω clipping at PMT base<br>12 fC / ADC count if no clipping |
| **Dynamic range** | 4096-256=3840 cnts :12 bit | Enough? New physic req.? Pedestal variation? Should be enough |
| **Noise** | <≈1 ADC cnt or ENC < 5 -6 fC | < 0.7 nV/√Hz → |
| **Termination** | 50 ± 5 Ω | Passive vs. active |
| **AC coupling** | Needed | Low freq. (pick-up) noise |
| **Baseline shift Prevention** | Dynamic pedestal subtraction (also needed for LF pick-up) | How to compute baseline?<br>Number of samples needed? |
| **Max. peak current** | 4-5 mA over 25 Ω<br>1.5 mA at FE input if clipping | 50 pC in charge |
| **Spill-over correction** | Clipping | Residue level: 2 % ± 1 % ? |
| **Spill-over noise** | << ADC cnt | Relevant after clipping? |
| **Linearity** | < 1% | |
| **Crosstalk** | < 0.5 % | |
| **Timing** | Individual (per channel) | PMT dependent |

**See talk about noise in June 2009 meeting:**

http://indico.cern.ch/materialDisplay.py?contribId=1&sessionId=0&materialId=slides&confId=59892

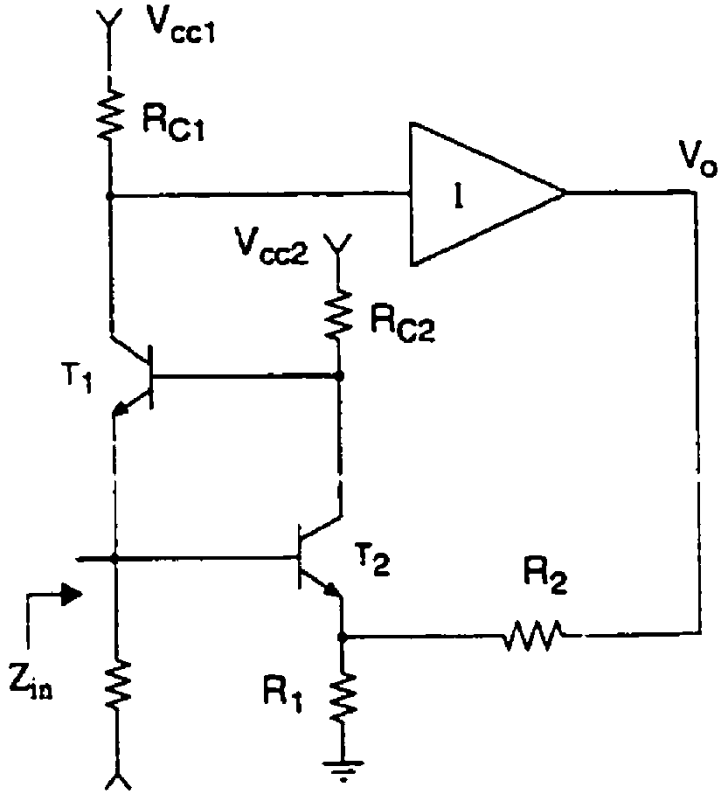
**This talk considers single ended implementation, results should be scaled by xsqrt(2)**

# II. Input stage: active line termination

- Electronically cooled termination required:
  - 50 Ohm resistor noise is too high
  - e. g. ATLAS LAr (discrete component)
- Common gate with double voltage feedback
  - Inner loop to reduce input impedance preserving linearity and with low noise
  - Outer loop to control the input impedance accurately

$$Z_i \approx \frac{1/g_{m1}}{G} + R_{C1}\frac{R_1}{R_1 + R_2}$$

- Transimpedance gain is given by $R_{C1}$
- Noise is < 0.5 nV/sqrt(Hz)
  - Small value for R1 and R2
  - Large gm1 and gm2
- Need ASIC for LHCb
  - 32 ch / board: room and complexity

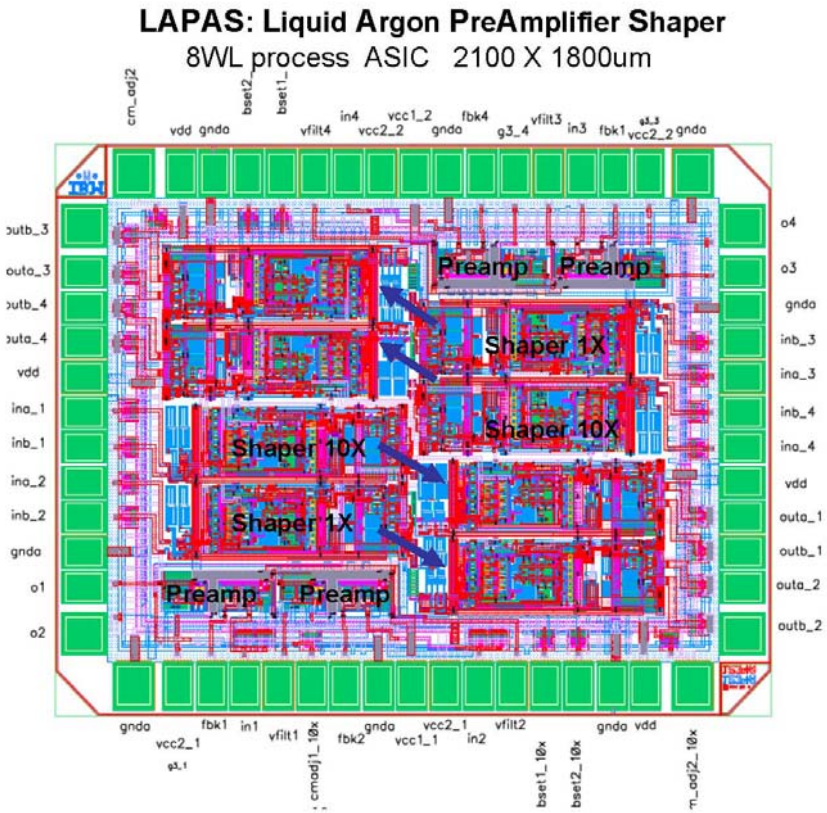


# II. Input stage : LAPAS chip for ATLAS LAr upgrade

- TWEPP 09

## LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter

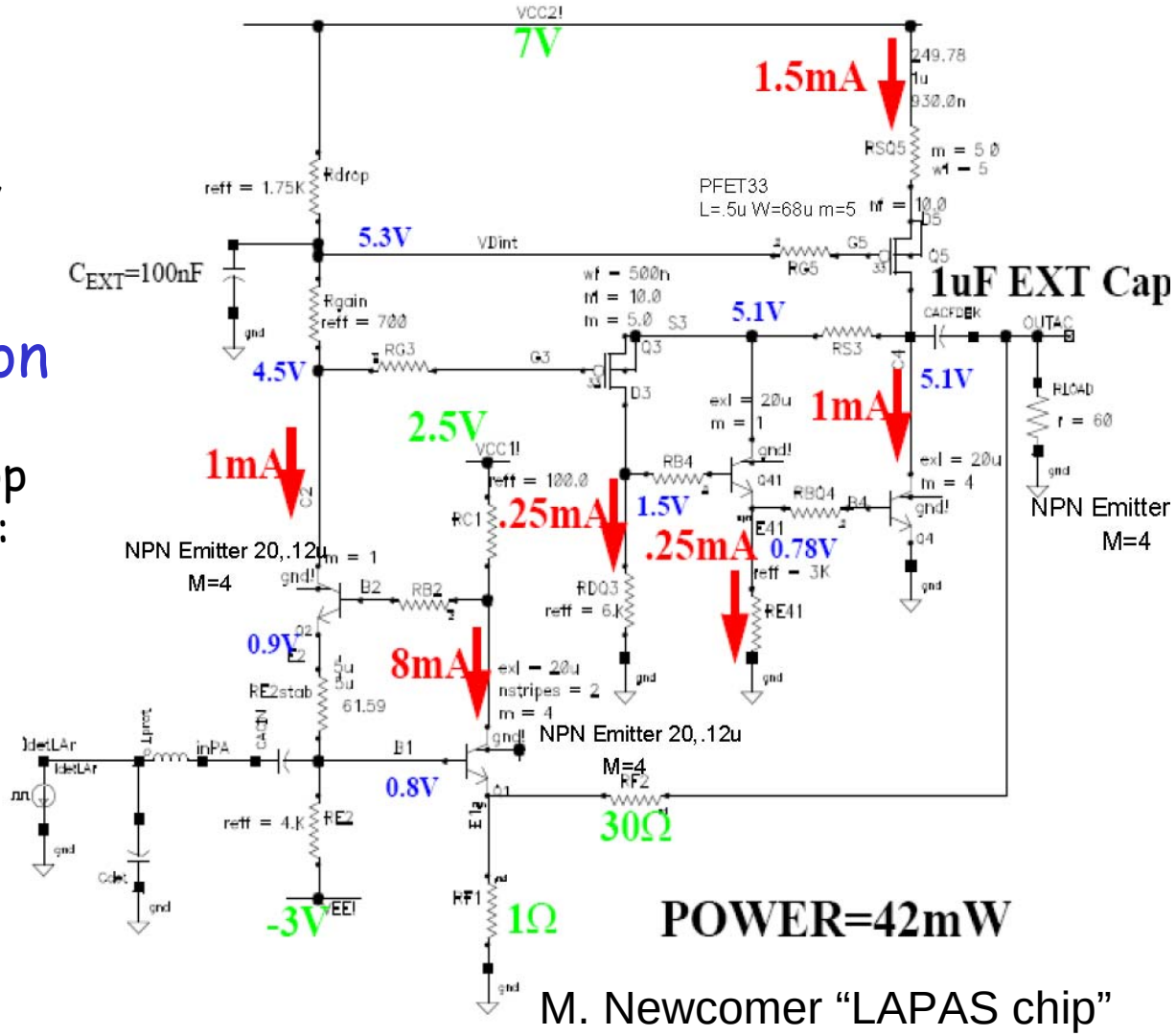
Mitch Newcomer
On Behalf of the ATLAS LAr Calorimeter Group*




*Special Acknowledgment of the significant contributions of Emerson Vernon, Sergio Rescia (BNL) and Nandor Dressnandt (Penn) to this work.*

# II. Input stage: LAPAS chip for ATLAS LAr upgrade

- Technology:
  - IBM 8WL SiGe BiCMOS
  - 130 nm CMOS (CERN's techno)
  - Radiation tolerance:
    - FEE Rad Tolerance TID~ 300Krad,
    - Neutron Fluence ~$10^{13}$ n/cm$^2$
- Circuit is "direct" translation
  - Need external 1 uF AC coupling capacitor for outer feedback loop
  - Three pads per channel required:
    - Input
    - Two for AC coupling capacitor
  - Voltage output



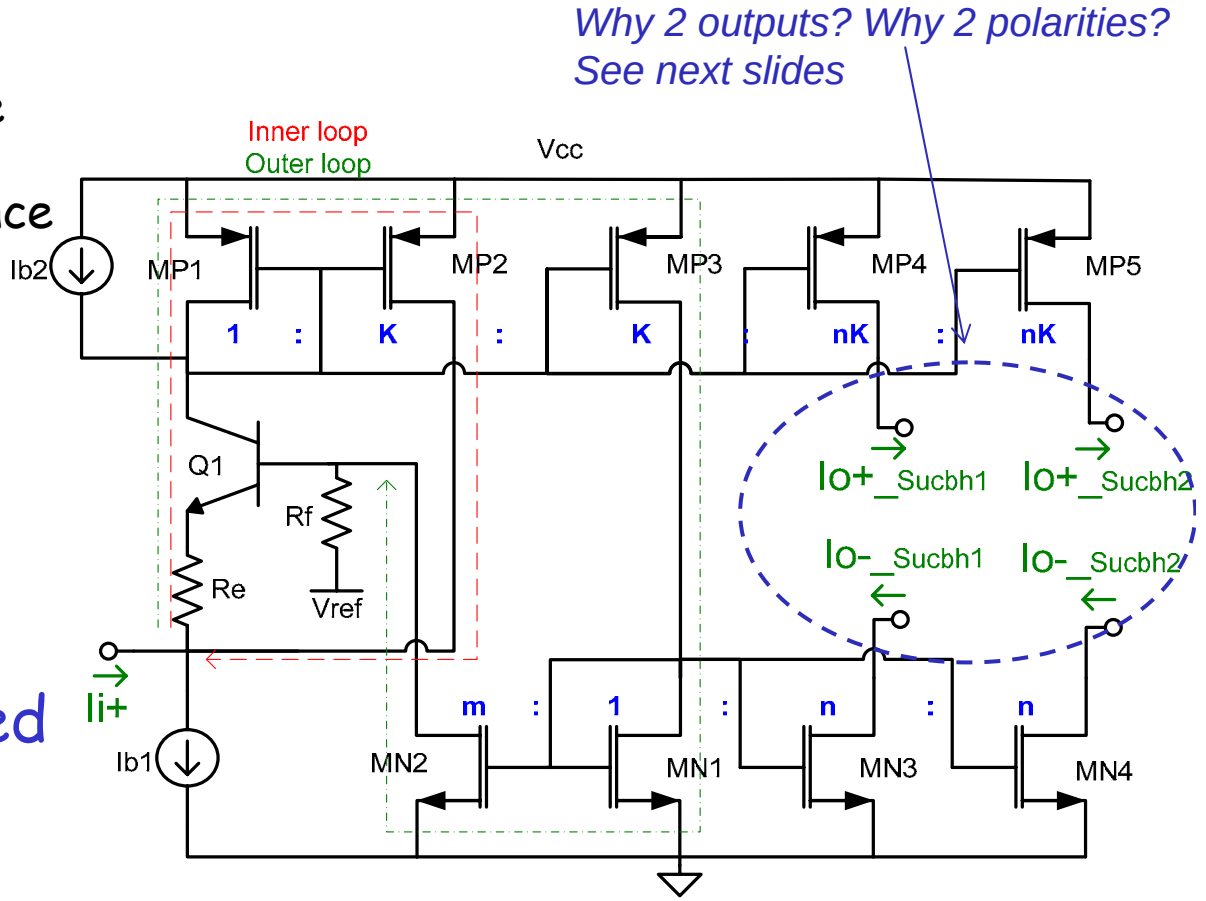

M. Newcomer "LAPAS chip"

# II. Input stage: current output / current feedback

- Current mode feedback:
  - Inner loop: lower input impedance
    - Current feedback (gain): mirror: K
  - Outer loop: control input impedance
    - Current feedback: mirror: m
- Current gain: m
- Input impedance

$$Z_i \approx \frac{1/g_{m1} + \mathrm{Re}}{1+K} + \frac{K}{1+K} mR_f$$

- Current mode feedback used
  - Optical comunications
  - SiPM readout
- Low voltage
  - Only 1 Vbe for the super common base input stage
- Better in terms of ESD:
  - No input pad connected to any transistor gate or base




**POWER < 10 mW**

# III. Channel architecture

*Very difficult to integrate HQ anlog delay lines*

↓

*2 switched alternated paths as in PS/SPD*

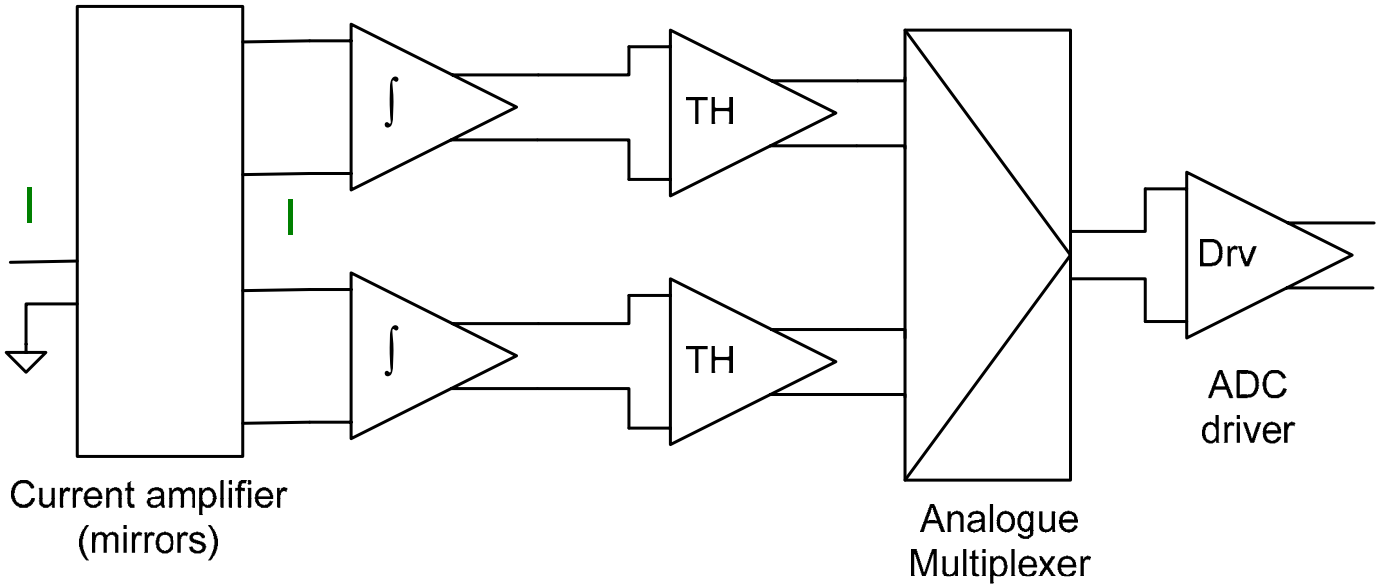
↓

*Switching noise !*

↓

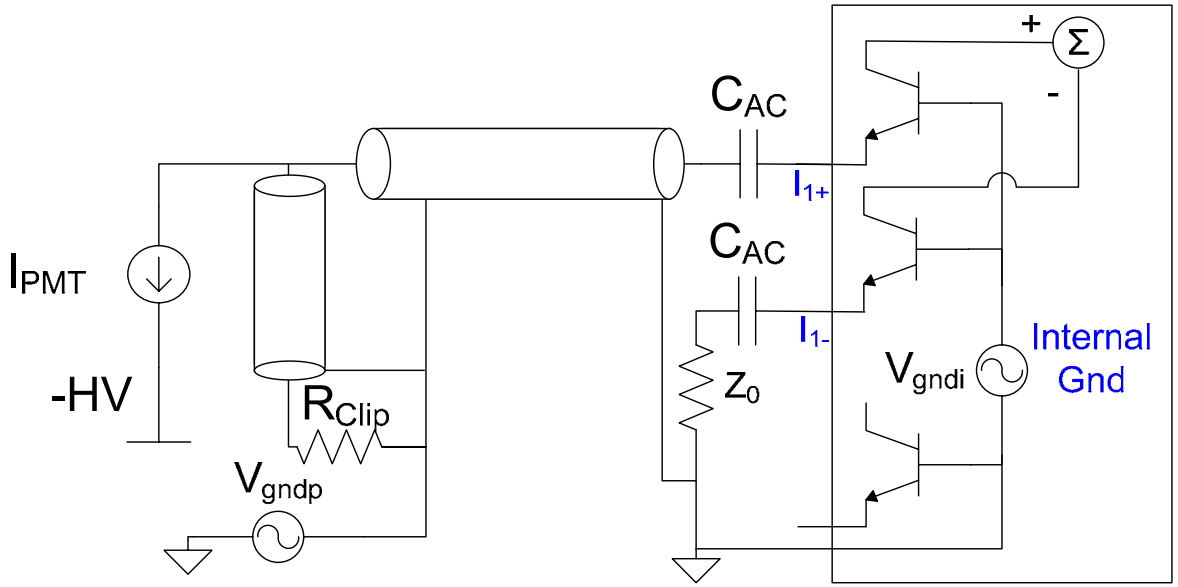
*Fully differential ASAP*

- Current mode amplifier
- Switched integrator
  - Fully differential Op Amp
- Track and hold
  - 12 bit: flip-around architecture
- Analogue multiplexer
- ADC driver
  - To match ADC input impedance



# III. Channel architecture: pseudo-differential input

- Pseudo-differential input attenuates ground (and CM) noise in FE:
  - Mitigates **Vgndi** (connducted) noise (attenuation depends on matching)
  - Symmetrical chip/PCB layout also mitigates capacitive coupling (xtalk, pick-up)

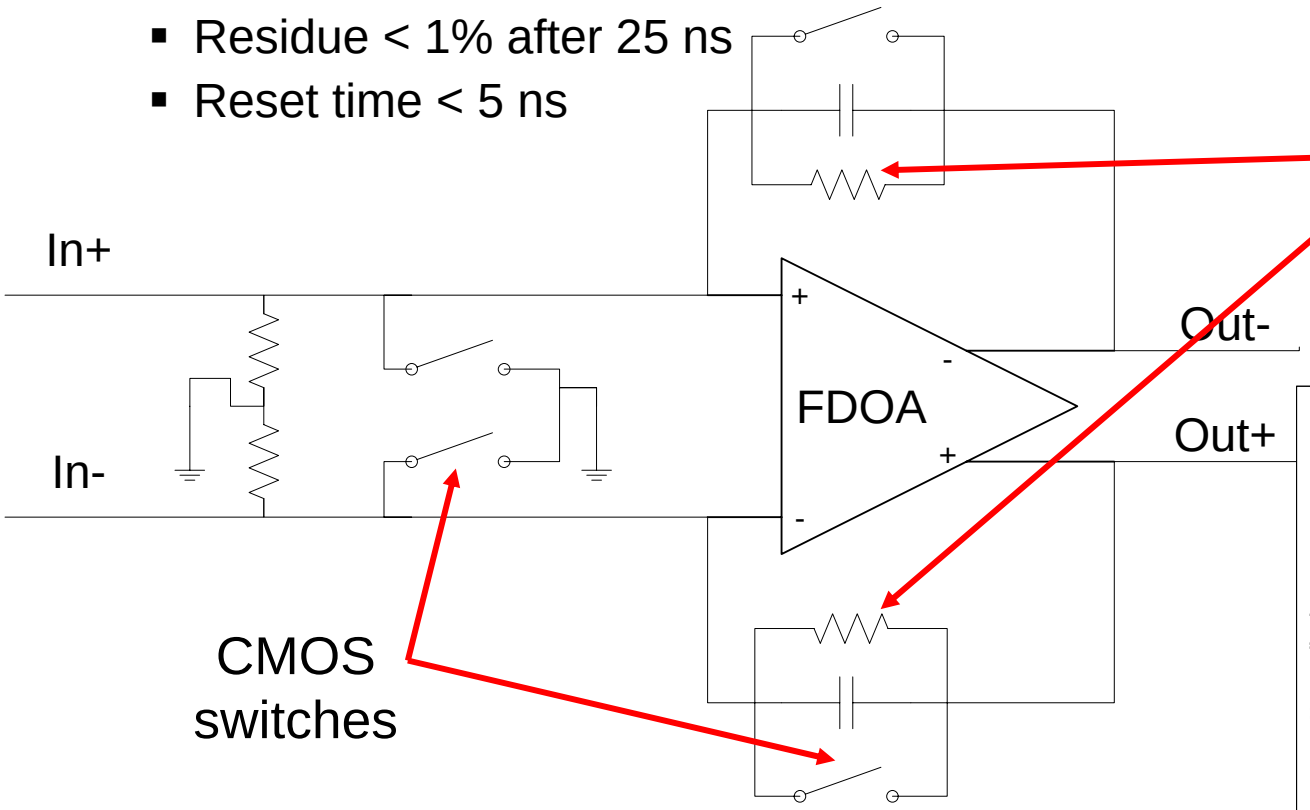


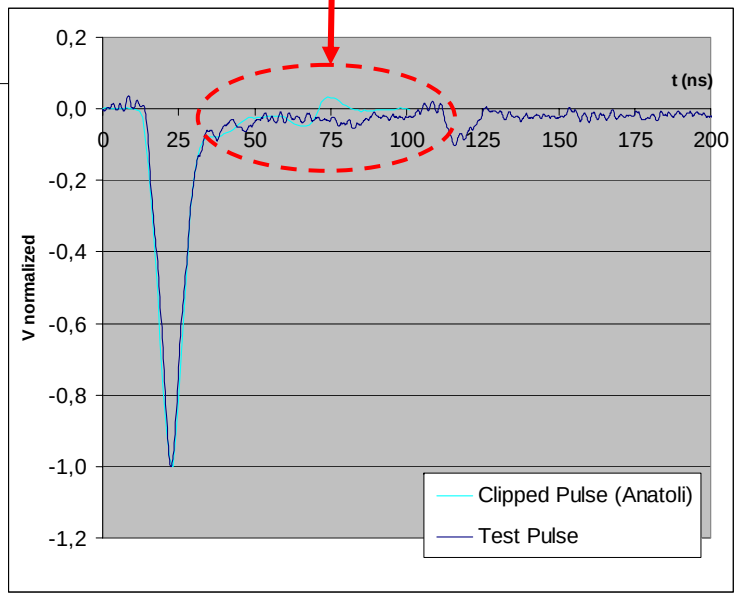

- Drawback: uncorrelated HF noise x √2
  - Predictable and stable effect
- Current mode preamplifier makes easier pseudo differential input:
  - Current: 2 pads per channel
  - Voltage (external component): 6 pads per channel

# III. Channel architecture

- Switched integrator
  - Integrator plateau : 4 ns
  - Linearity <  1%
  - Residue < 1% after 25 ns
  - Reset time < 5 ns

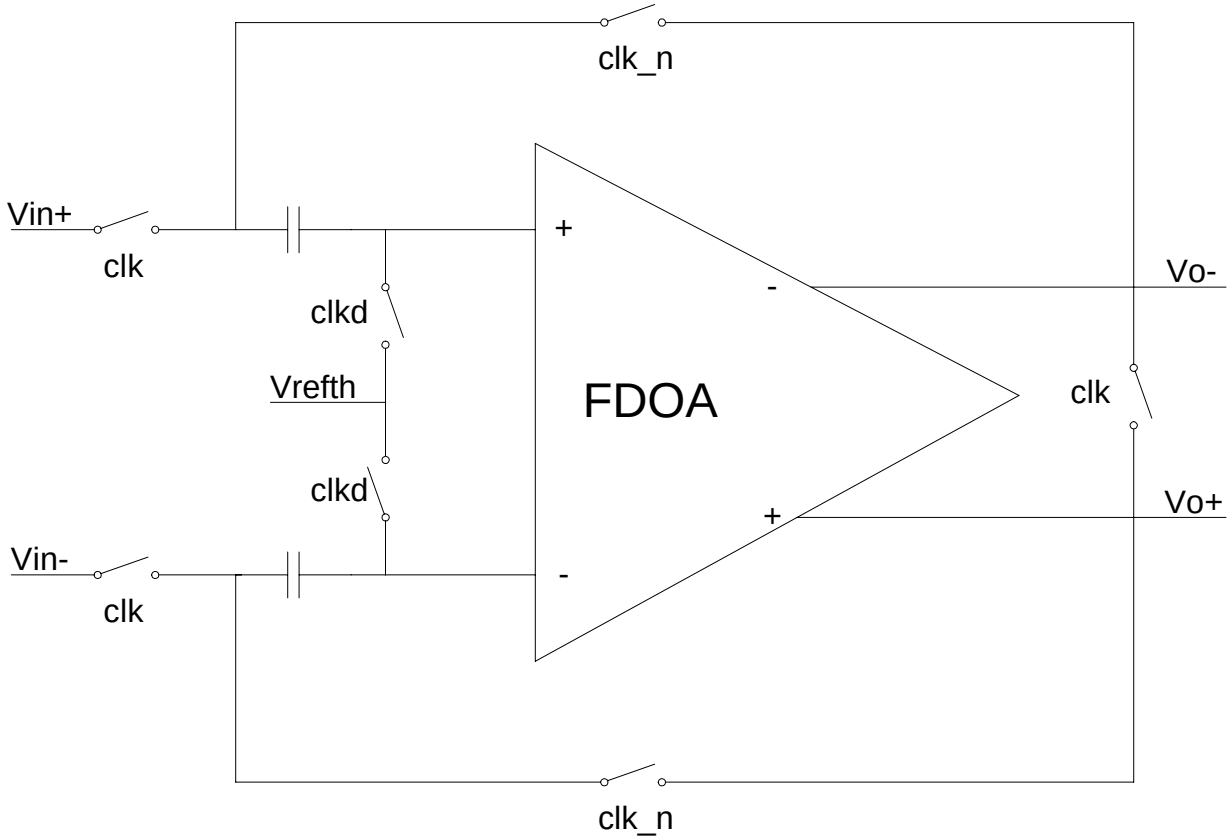
- Rf to improve plateau
  - 100 ns time constant
  - Cancel slow component of the clipped signal (remanent)



# III. Channel architecture

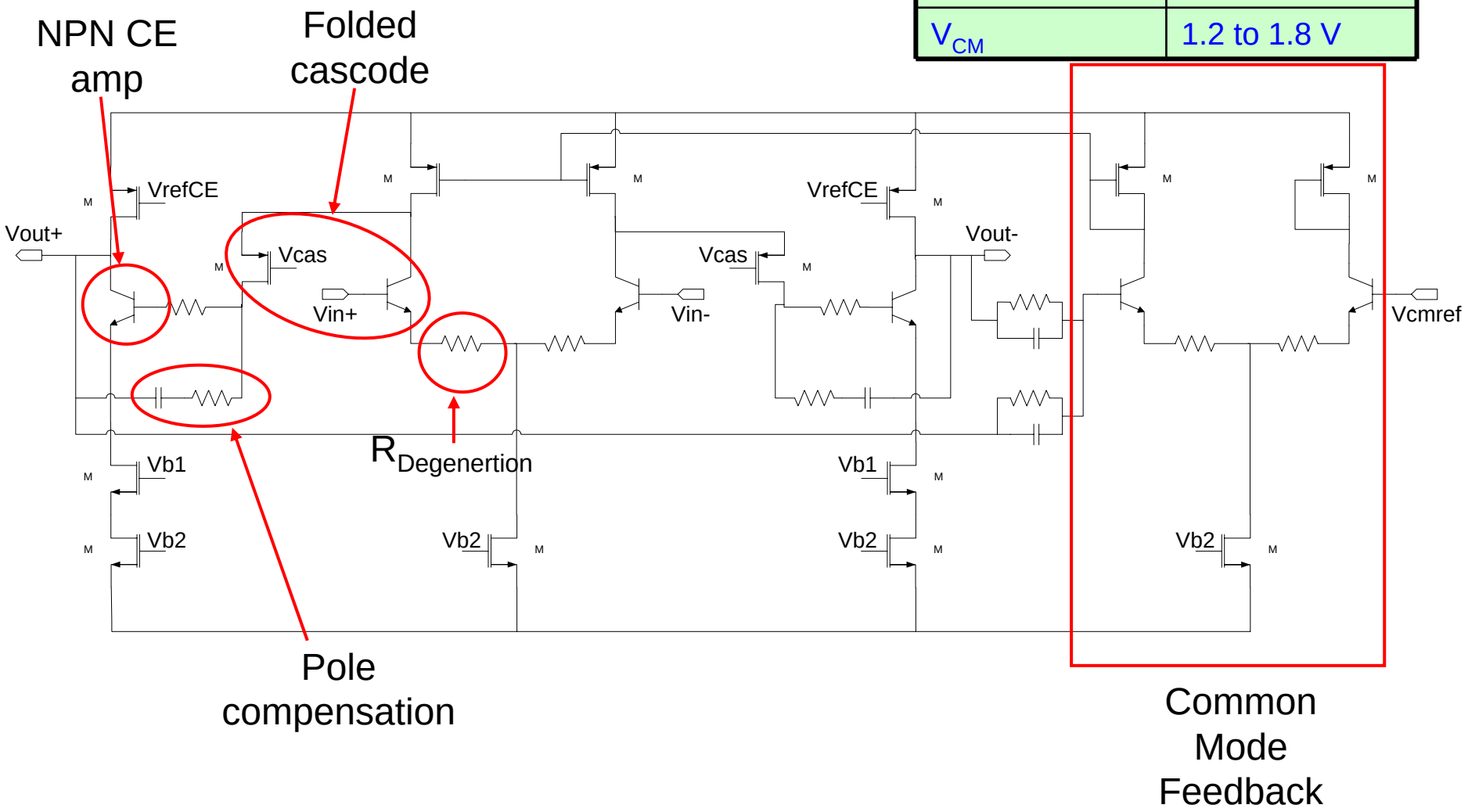
- Track and hold
  - 12 bit: flip-around architecture



# III. Channel architecture

| FDOA specifications | |
|---|---|
| **Parameter** | **Value** |
| Gain bandwidth | 500 MHz |
| Phase margin | > 65º |
| Slew rate | > 0.5 V/ns |
| $V_{CM}$ | 1.2 to 1.8 V |

- Fully differential Op Amp
  - Folded cascode + Miller stage with CMFB



# IV. Technology: choice of technology

- SiGe BiCMOS is preferred:
  - SiGe HBTs have higher gm/Ibias than MOS: less noise, less Zi variation
  - SiGe HBTs have higher ft (>50 GHz): easier to design high GBW amplifiers
- Several technologies available:
  - IBM
  - IHP
  - AMS BiCMOS 0.35 um

| | IBM | IHP | AMS |
|---|---|---|---|
| HBT ft | > 100 GHz | 190 GHz | 60 GHz |
| CMOS | 0.13 um | 0.13 um | 0.35 um |
| Proto Cost [€ /mm$^2$] | > 3 K | > 3 K | 1 K |

- AMS is preferred
  - Factor 2 or 3 cheaper
  - Too deep submicron CMOS not required / not wanted:
    - Few channels per chip (4 ?)
    - Smaller supply voltage
    - Worst matching
  - Radiation hardness seems to be high enough (to be checked)

# IV. Technology: radiation tolerance

- Requirements:
  - Dose in 5 years (TID): 10-20 krad
  - Neutron fluence?
- AMS SiGe BiCMOS 0.35 um should be ok:
  - Omega studies about ILC calorimeters…
  - ATLAS: CNM studies: http://cdsweb.cern.ch/record/1214435/files/ATL-LARG-SLIDE-2009-337.pdf
  - ***CMS: Technology adopted for HCAL upgrade (QIE10 chip)***
    - Total radiation dose = 10 krad = 100 Gy
    - Neutron fluence = $10^{13}/cm^2$
    - Charged hadron fluence = $2 \times 10^{10}/cm^2$

*Possible to share efforts on rad qualification? Enginnering run? Cost…*

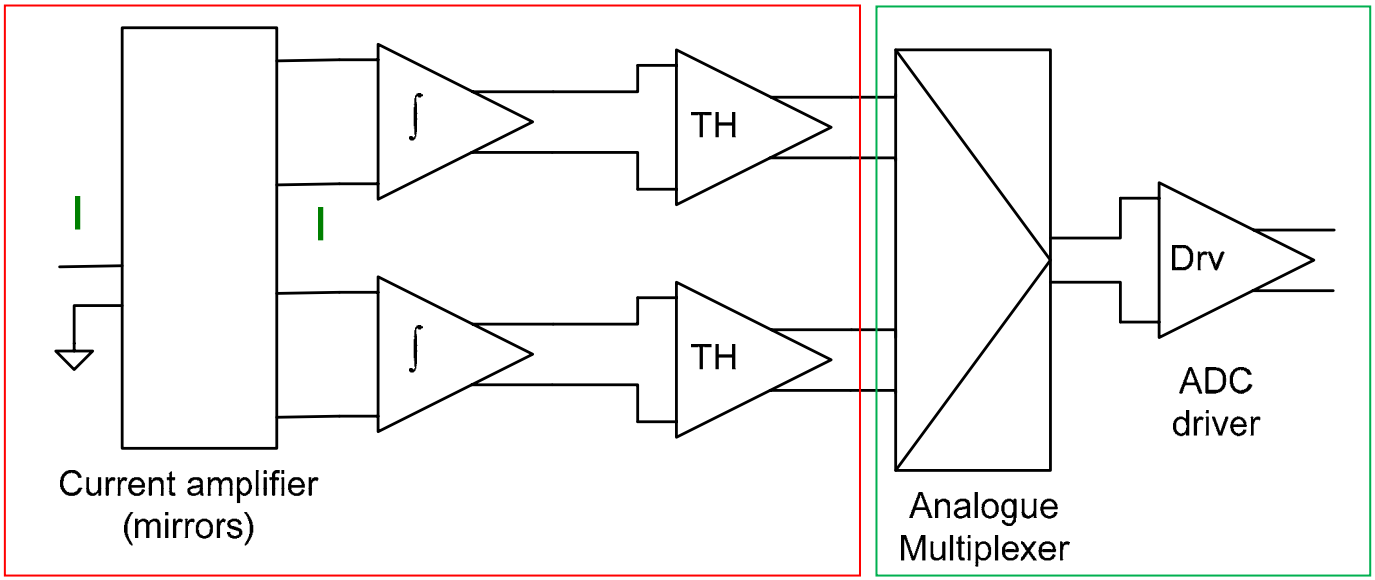
- Radiation tolerance should be taken into account at design:
  - Cumulative effects:
    - Use feedback (global or local): minimal impact of beta degradation
    - Not rely on absolute value of components, use ratios but
  - Transient events:
    - Guard rings for CMOS and substrate contacts: avoid SEL
    - Majority triple voting: SEU hardened logic (if any)

# V. Status and plans

- Prototyped in AMS :
  - Low noise current amplifier:
  - Basic schemes
  - Integrator:
    - High GBW fully differential OpAmp
  - Track and hold
  - Clock generation

- Channel will be final with:
  - Analogue multiplexer
  - ADC driver
  - Tuneablility on gain, input impedance and integration plateau
    - To compensate process variations
    - To cover different operation conditions

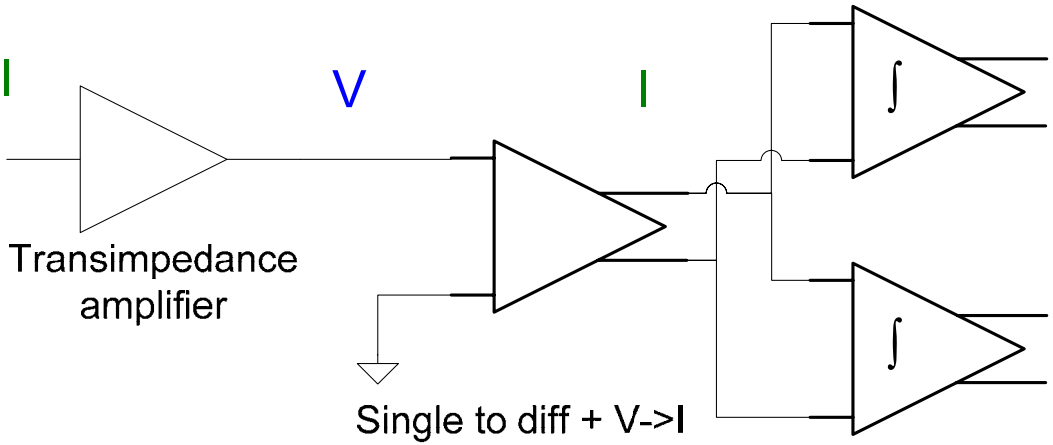
***See Edu's talk***



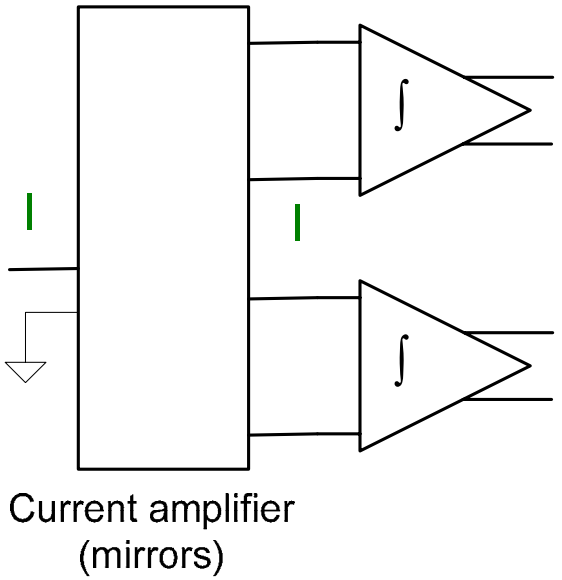
# BACK-UP

# I. Introduction: voltage output versus current output

- Voltage output:
  - Pros:
    - Tested
  - Cons:
    - I (PMT) -> V and V -> I (integrate)
    - Larger supply voltage required
    - External components
    - 2 additional pads per channel

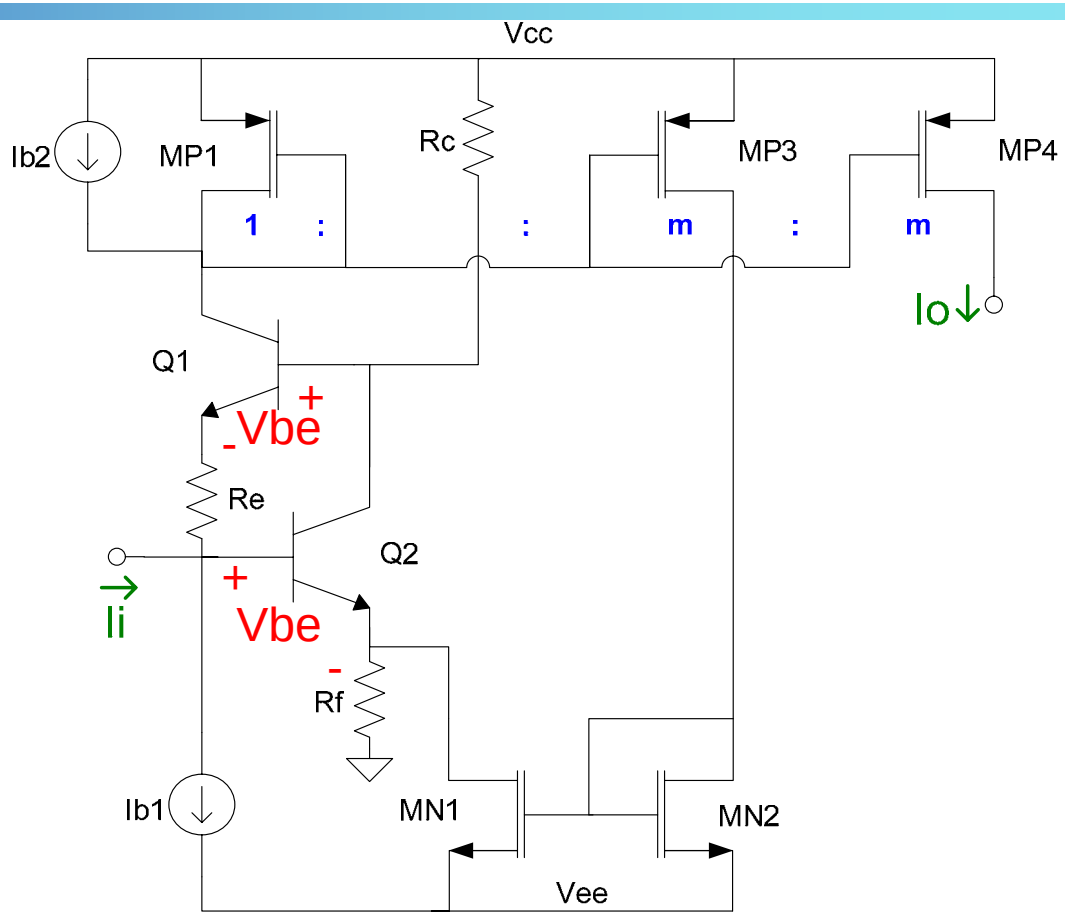



- Current output ("à la PS")
  - Pros:
    - "Natural" current processing
    - Lower supply voltage
    - All low impedance nodes:
      - Pickup rejection
    - No external components
    - No extra pad
  - Cons:
    - Trade-off in current mirrors: linearity vs bandwidth



# II. Preamplifier: current output / mixed feedback

- Mixed mode feedback:
  - Inner loop: lower input impedance
    - Voltage feedback (gain): Q2 and Rc
  - Outer loop: control input impedance
    - Current feedback: mirrors and Rf

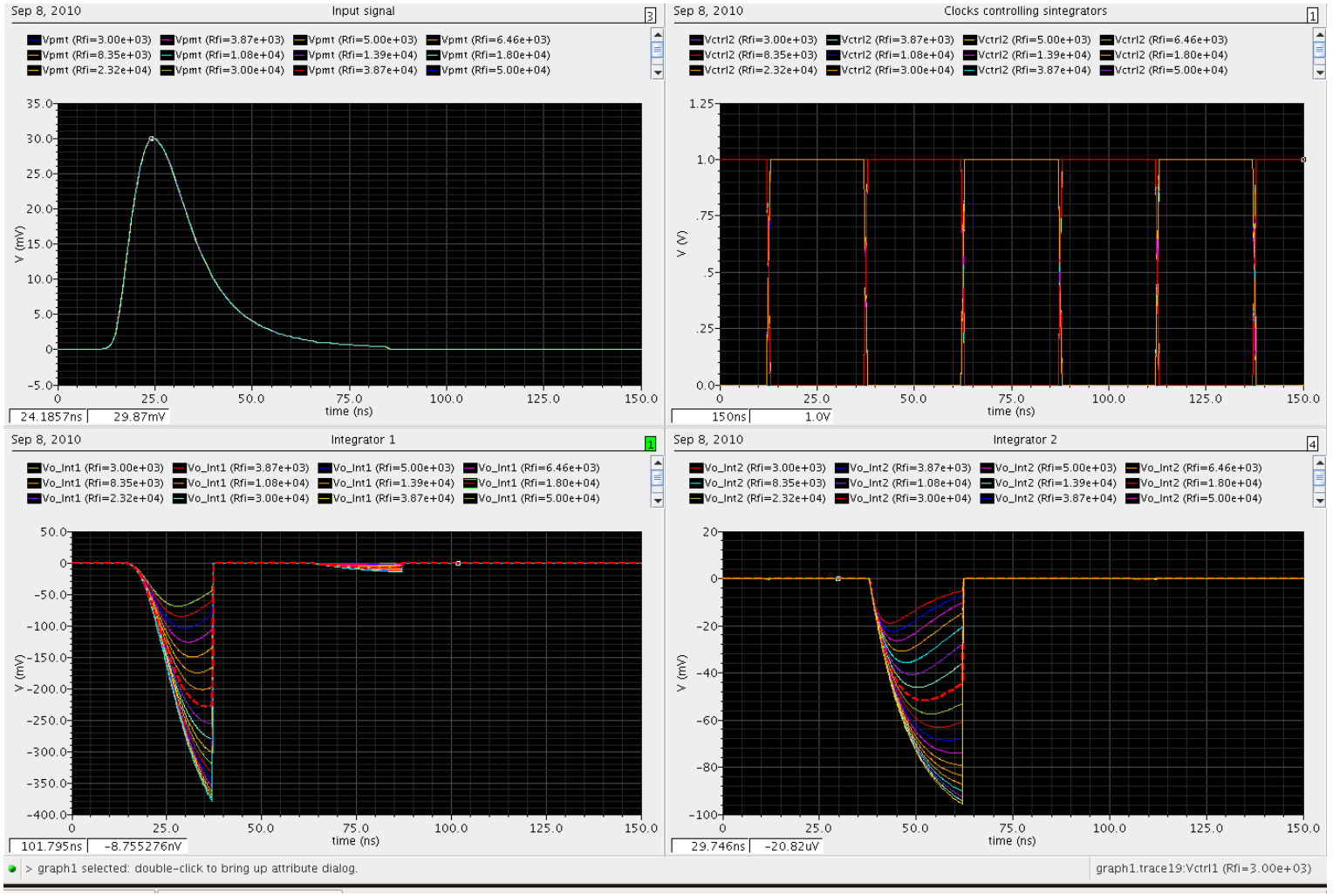



- Variation of LAr preamplifier
- Current gain: m
- Input impedance

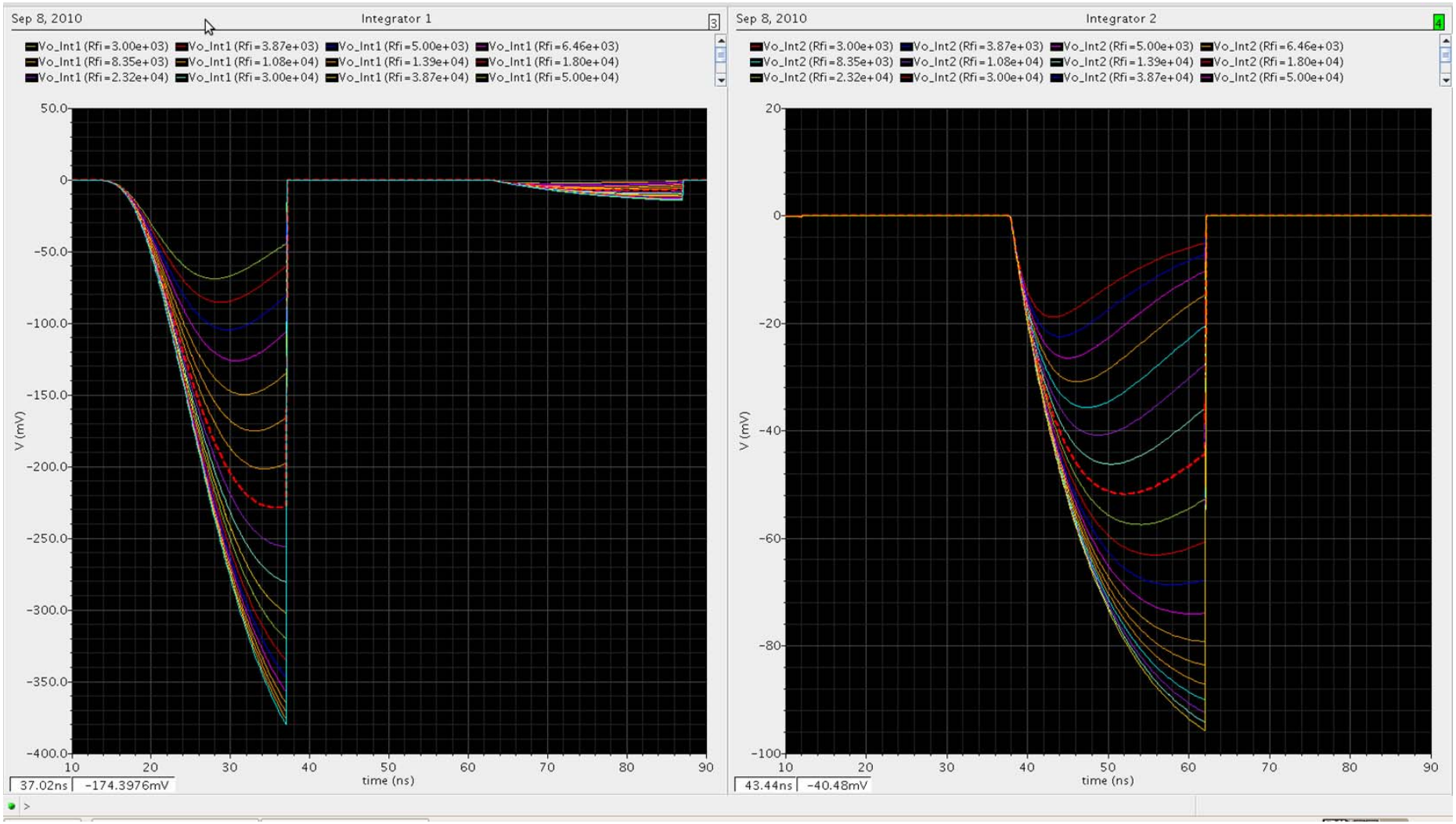
$$Z_i \simeq \frac{1/g_{m1} + \mathrm{Re}}{g_{m2} Rc} + mR_f$$

- Problem:
  - Voltage feedback for the super common base needs 2 Vbe (about 1 .5 V !)
  - Small room for current mirrors with 3.3 V
    - Need cascode current mirrors
    - 5 V MOS available: but poor HF performance

- Possible alternative to delay line clipping or gaussian shaping



- Possible alternative to delay line clipping or gaussian shaping

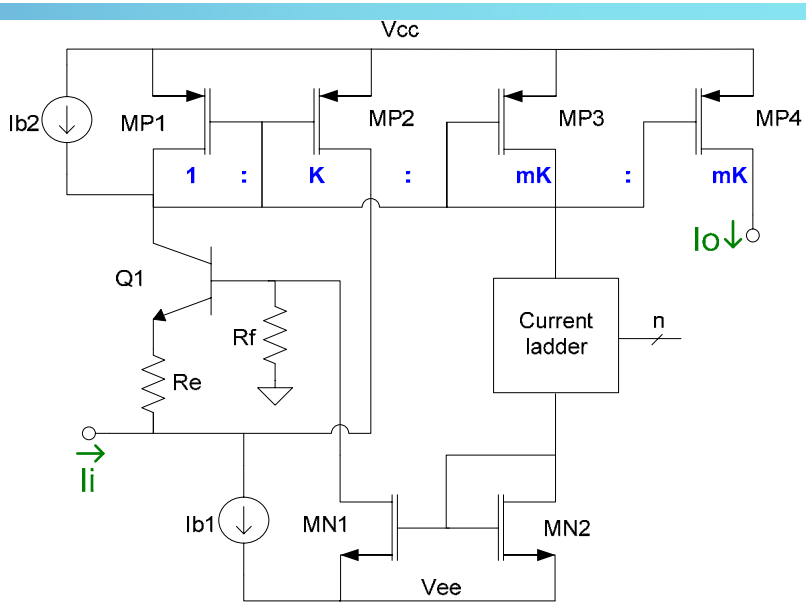


# IV. Technology issues: effect of process variations

- Input impedance is the key point
- Two types of parameter variation simulated
  - Mismatch between closely placed devices (local variation component to component)
    - No problem: 1 % level
  - Process variation (lot to lot):
    - Problem: 10-30 % level !! (uniform distribution)
      - Pessimistic: experience tell that usually production parameters are close to the typical mean values
- In principle process variation affects whole production (1 run)
  - Could be compensated with an external resistor in series / parallel with the input
- Variation wafer-to-wafer or among distant chips in the same wafer:
  - Can not be simulated
  - Higher than mismatch and lower than process variation
  - According to previous experience: 2-3 % sigma: BUT NO WARRANTY
- Should we foresee a way to compensate it?
  - Group (2-3) chips and:
    - Different pcb (2 – 3 different external resistor values
    - Tune a circuit parameter
  - Automatic tunning

# IV. Technology issues: effect of process variations

- Input impedance controllable by:
  - Tune feedback resistor Rf
    - Difficult: small value (Ron of the switch)
  - Tune second feedback current
    - Binary weighted ladder (3 bits?): simple




- How control current ladder control?
  - Group ASICs a fix the value, set by:
    - External jumper
    - Slow control: dig interface required
  - Automatic tunning
    - Reference voltage
      - Reference currents: external or band gap
      - External resistor
    - Wilkinson or SAR ADC style logic