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Institut de Ciències del Cosmos

Progress on ICECAL prototypes and chip tests

Upgrade of the front end electronics of the LHCb calorimeter

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Calorimeter upgrade meeting – CERN – July 22nd 2011

Outline

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   ii. Test set-up
   iii. Offset
   iv. Noise
   v. Input impedance
   vi. Linearity
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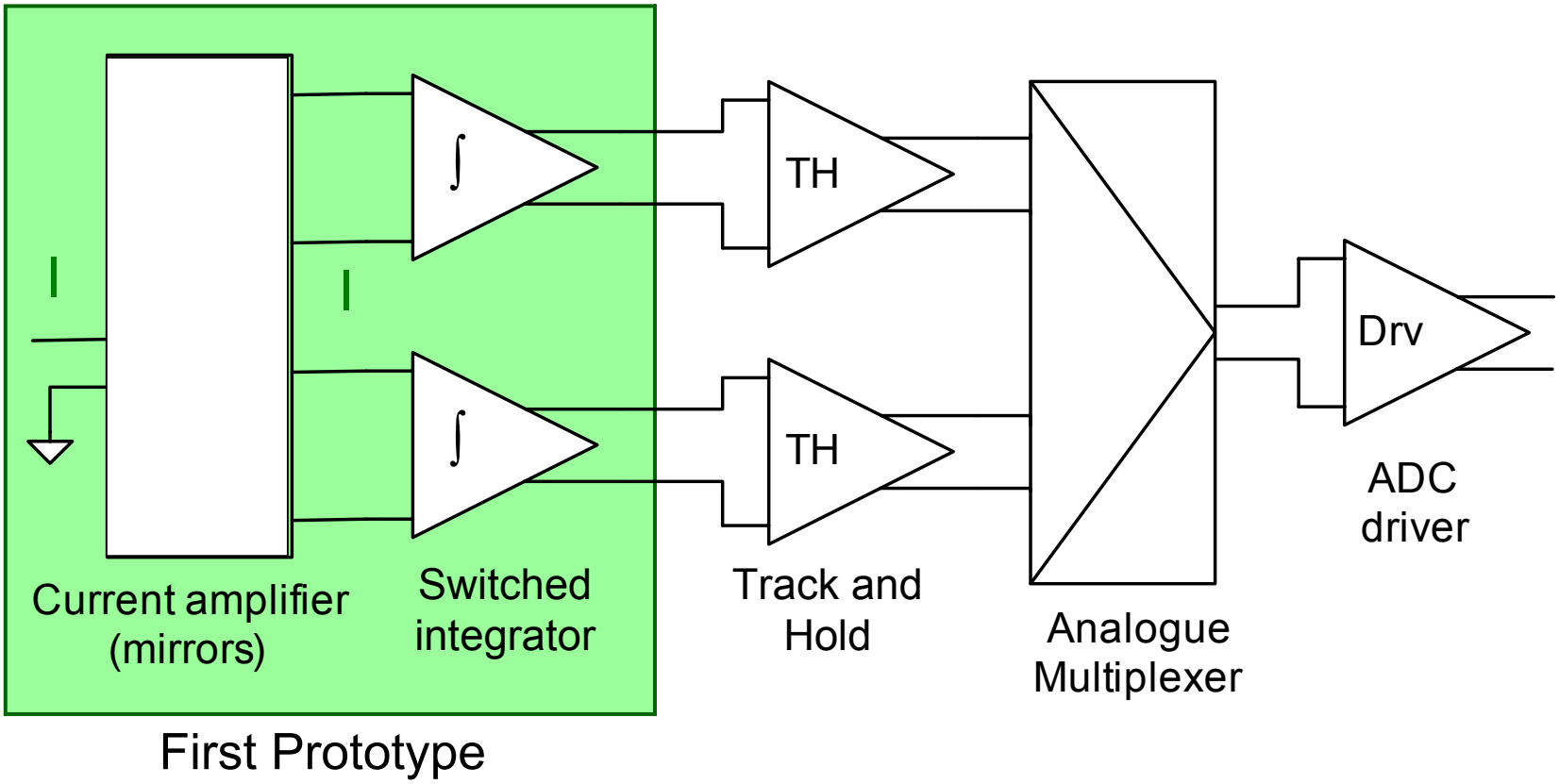
   viii. Characterization of preamp
2. Second prototype
   i. What is new
   ii. Flatness: clock jitter vs input signal
3. Summary

First prototype

- ECAL analogue FE IC: channel architecture



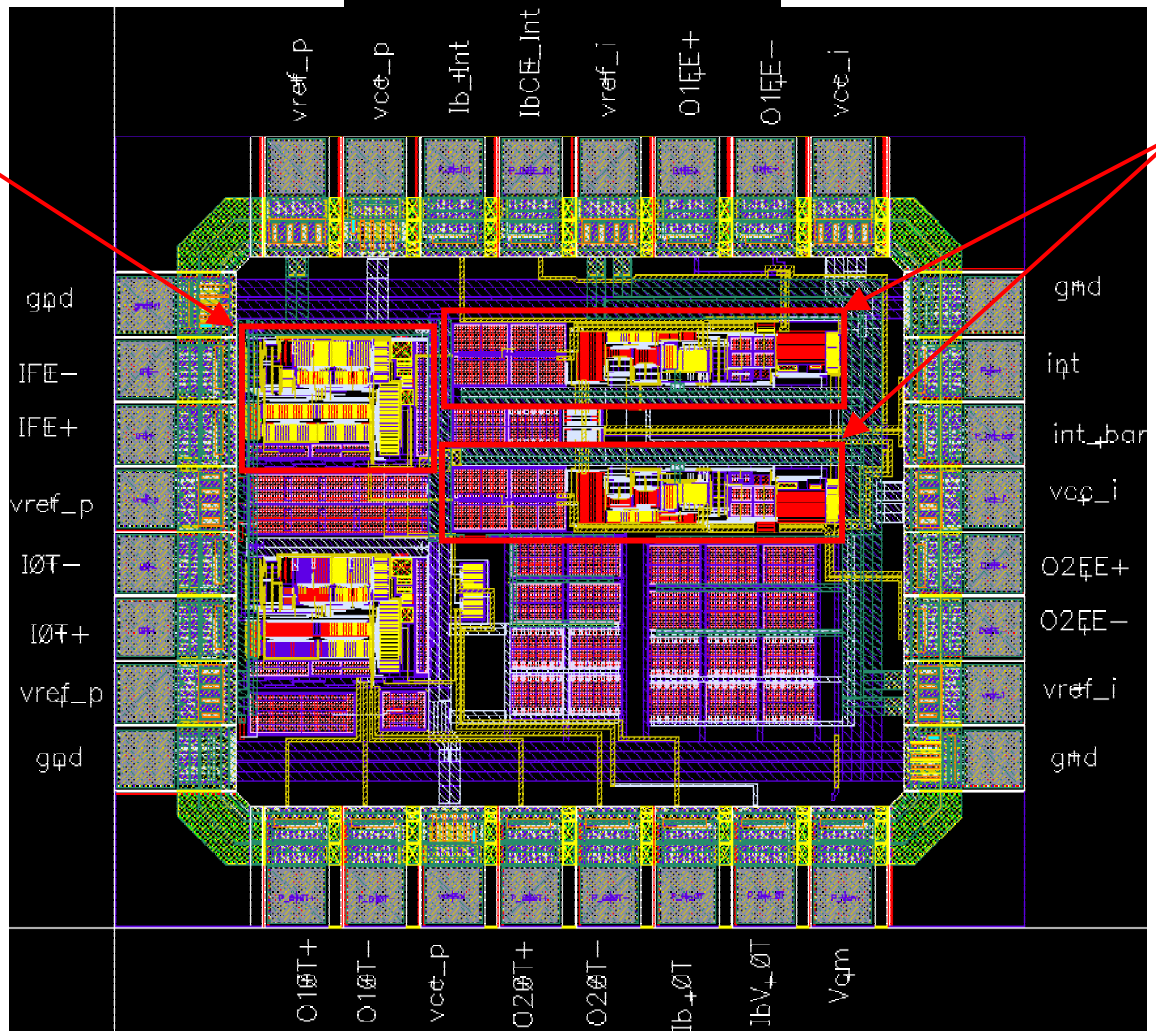
First prototype

- ICECAL chip

SiGe BiCMOS 0.35um
AMS 2 mm²
Submitted: June 7th 2010

Current preamp

Integrators

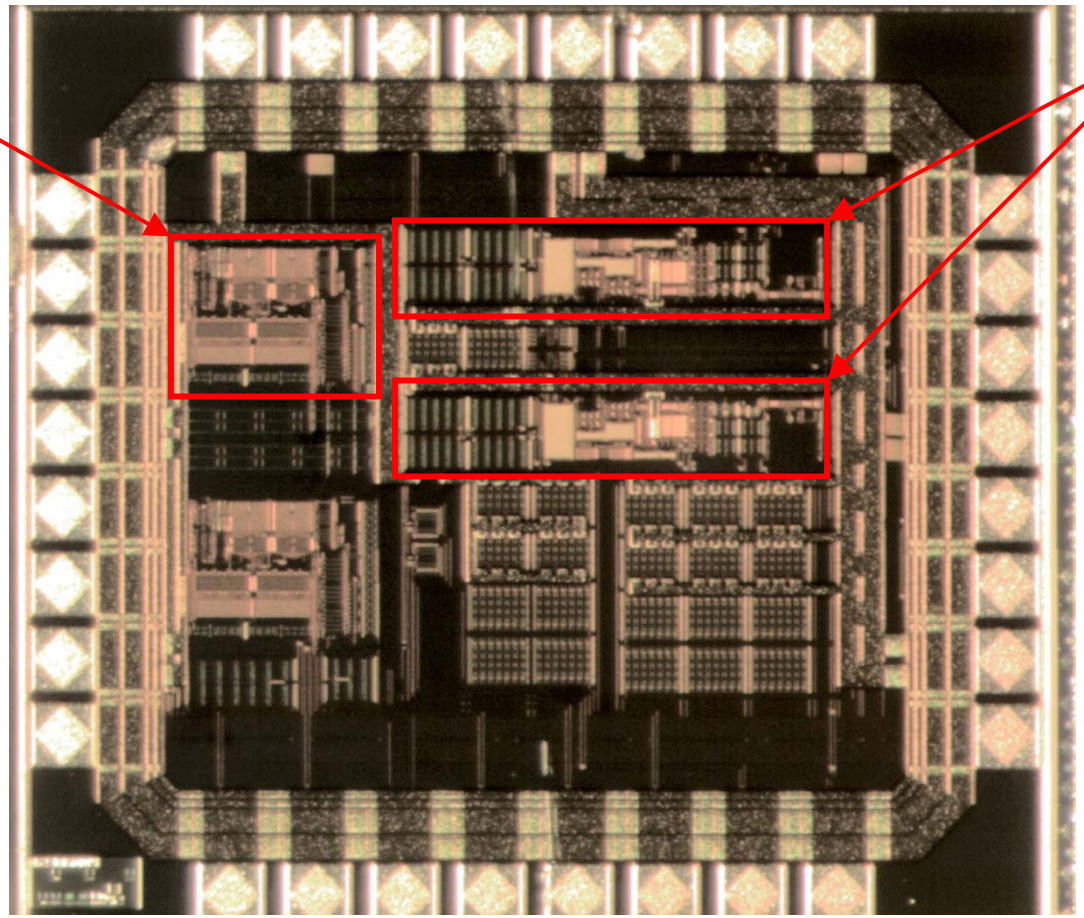


First prototype

- ICECAL chip

SiGe BiCMOS 0.35um
AMS 2 mm²
Received: October 2010
12 chips

Current preamp



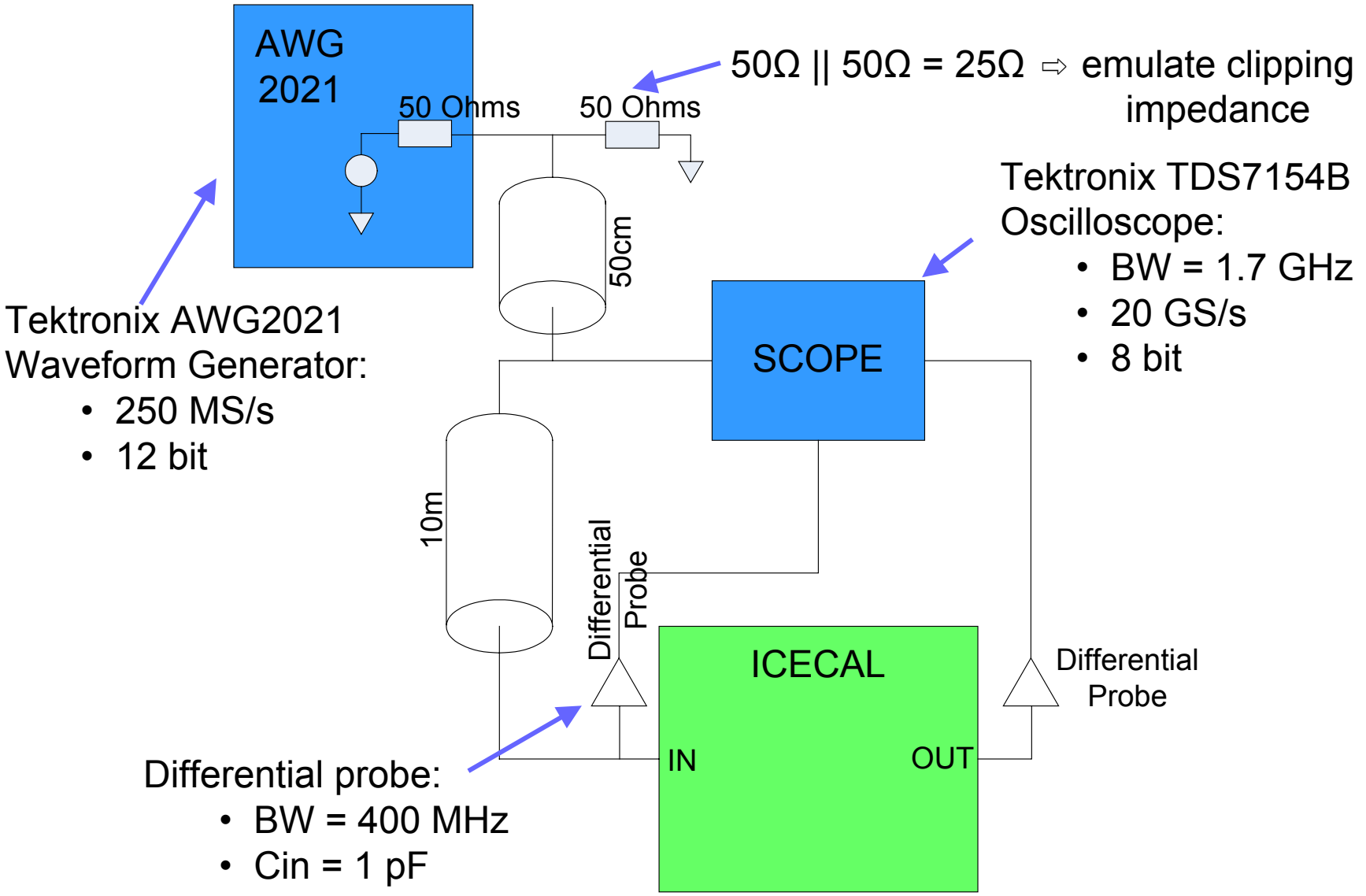
Integrators

Key tests on the first prototype

- The purpose of this prototype is to test key points of a novel circuit idea:
  - Input impedance control by current feedback
  - Low noise performance
  - Dynamic range:
    - Linearity

- Also, to test critical aspects of a switched solution:
  - Offset between subchannels
  - Noise
  - “Flatness” of the integrator output
    - Effect of the clock jitter versus signal

Test set-up



Tektronix AWG2021
Waveform Generator:

- 250 MS/s
- 12 bit

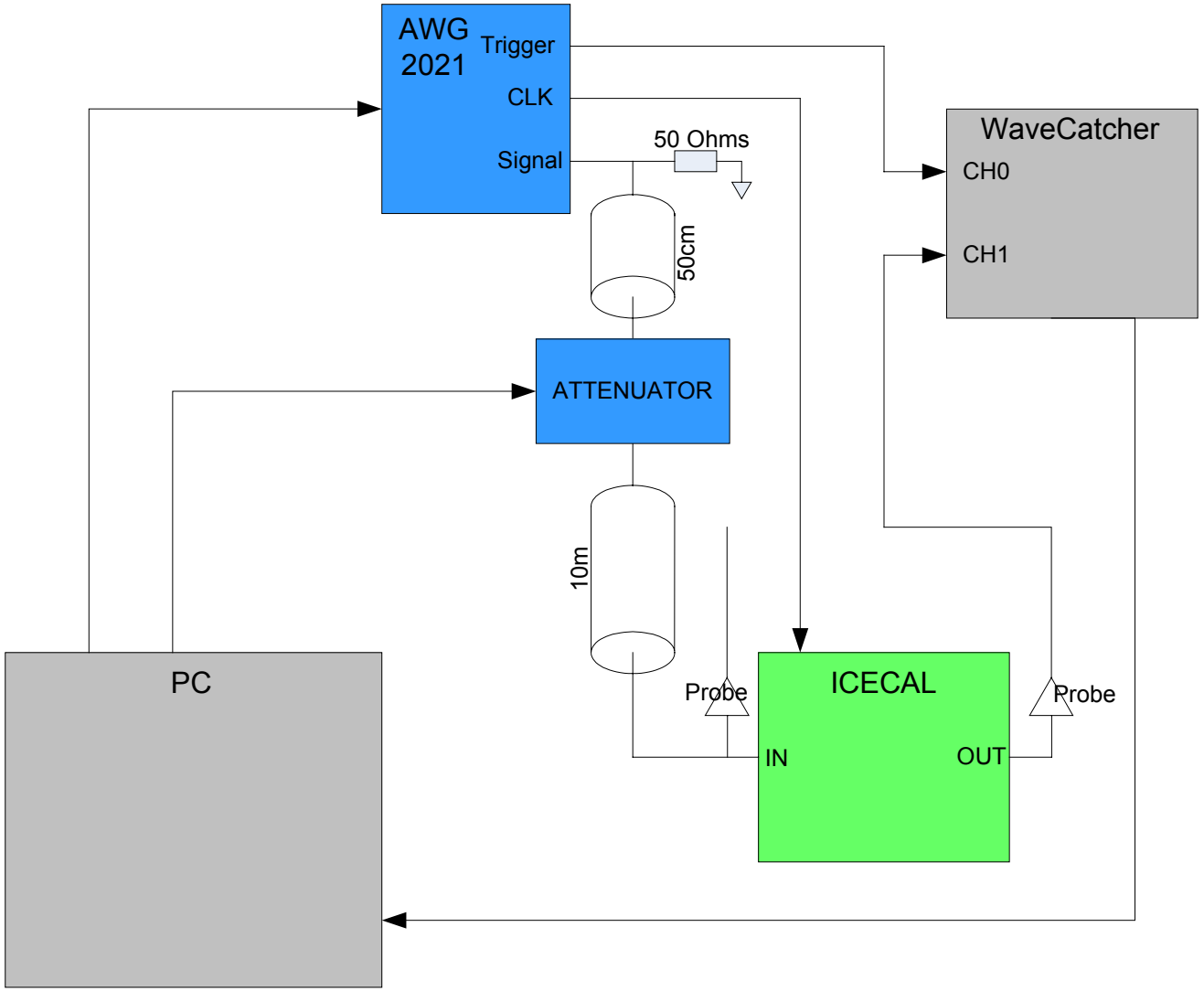
Tektronix TDS7154B
Oscilloscope:

- BW = 1.7 GHz
- 20 GS/s
- 8 bit

Differential probe:

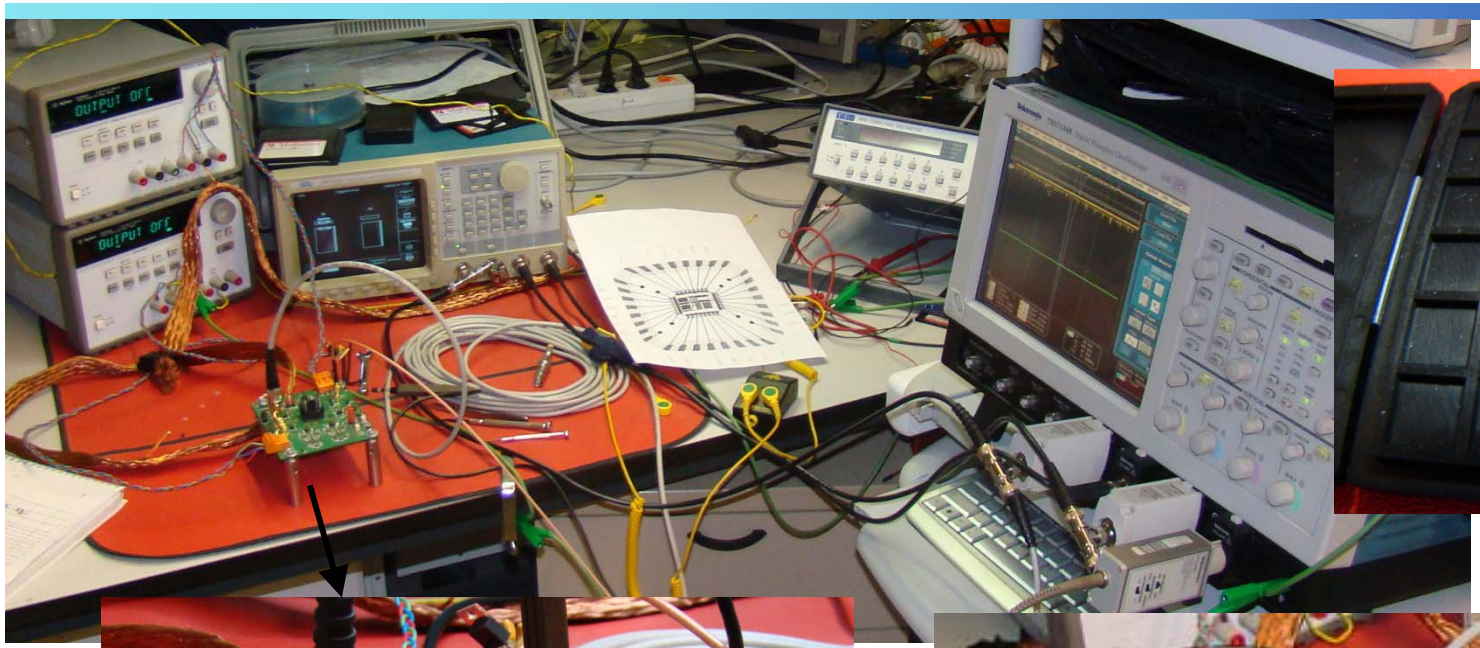
- BW = 400 MHz
- Cin = 1 pF

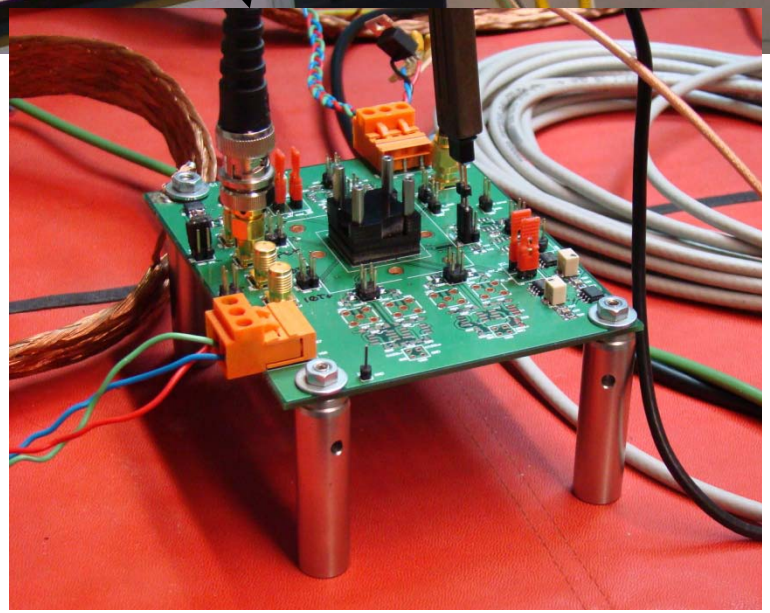
Test set-up: linearity



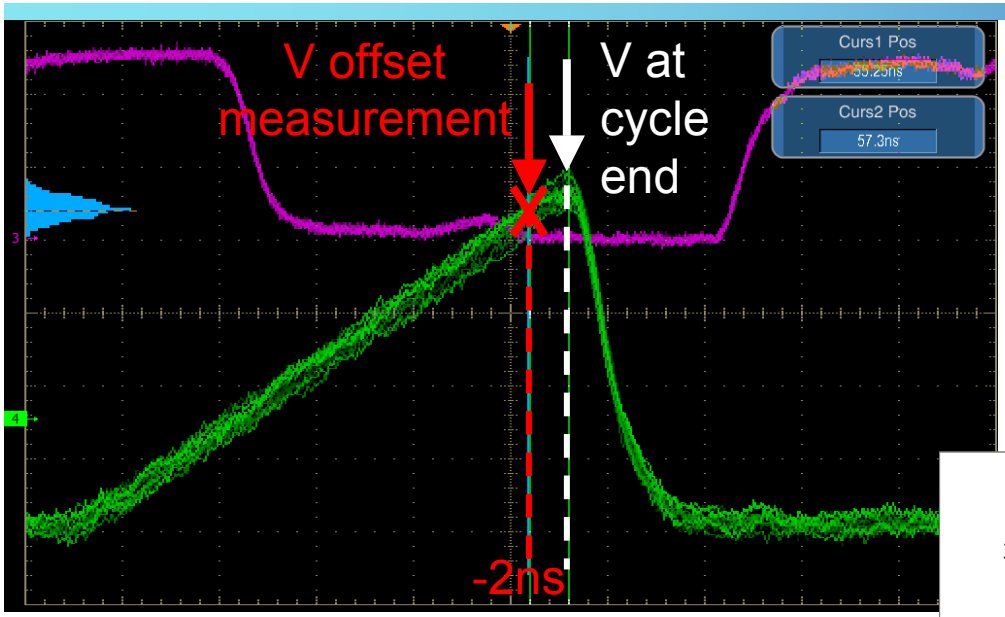
- Attenuator:
  - Better linearity than AWG (<1%)
  - No need for timing corrections
- WaveCatcher:
  - Better linearity than oscilloscope
- PC:
  - Automatized system

Test set-up





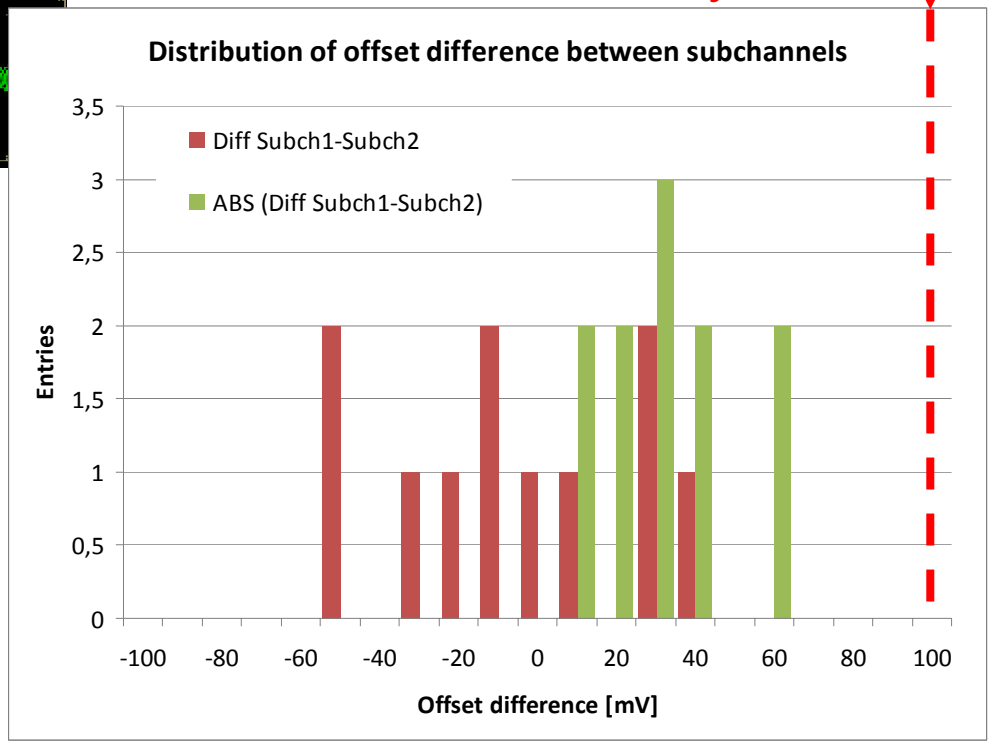
First Prototype: Offset



Offset measurement:

Preamp current offset is integrated

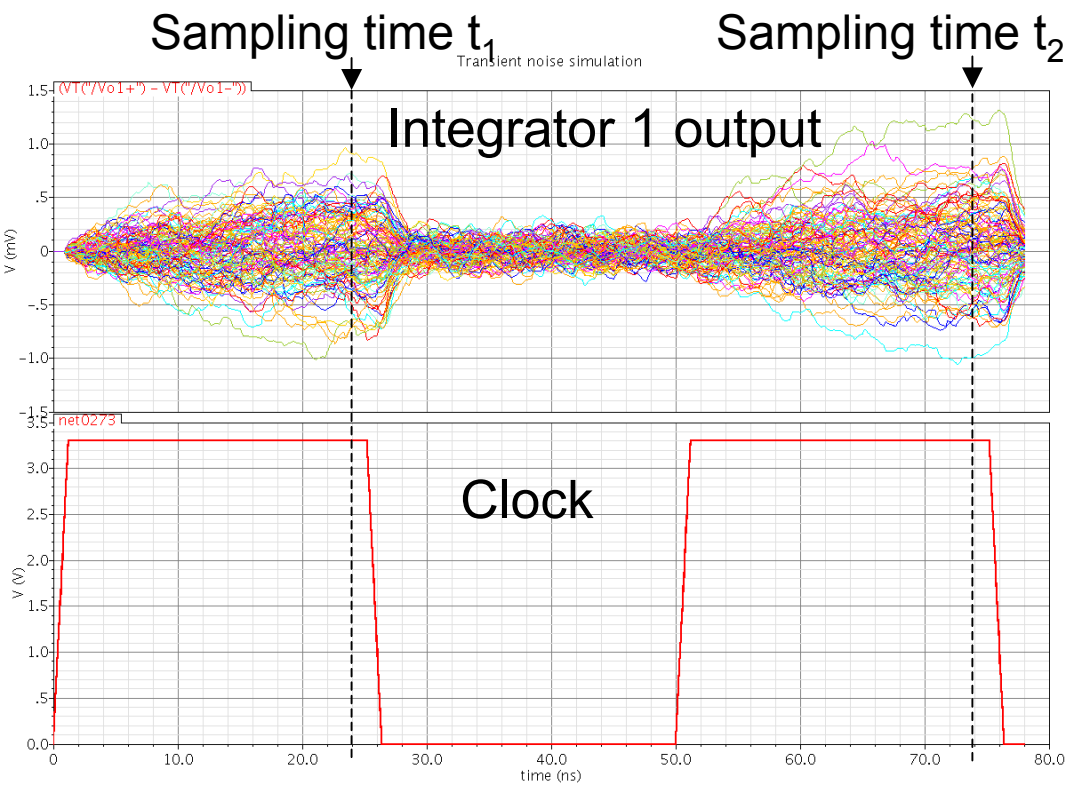
=> Offset at output

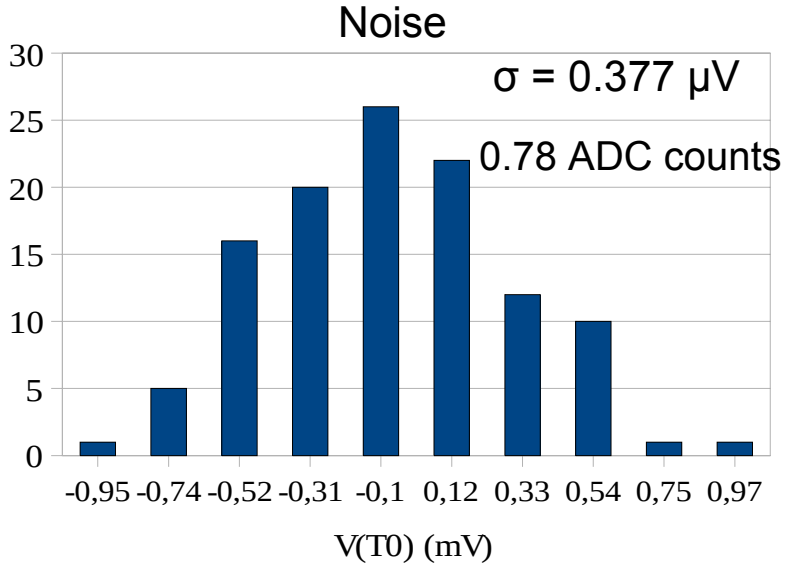


- With AC coupling between ICECAL and ADC what really matters is the difference between the offset of the 2 subchannels
- Well below the 5 % of the full scale range (2 V)

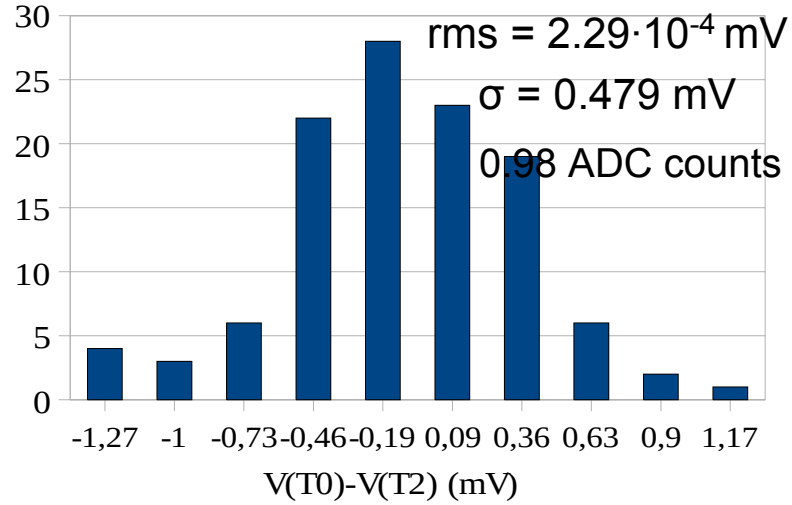
Noise: simulation

- Transient noise analysis





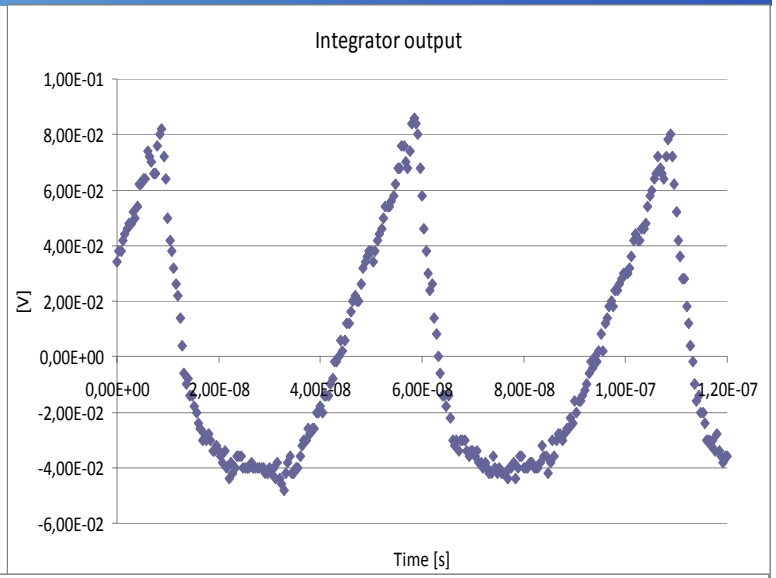
Noise after dynamic pedestal subtraction

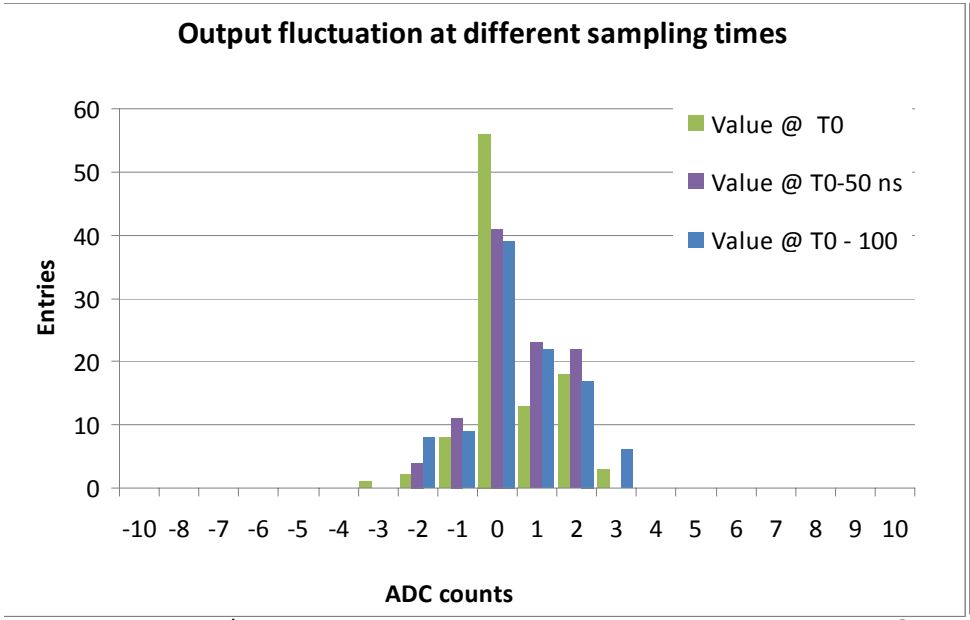


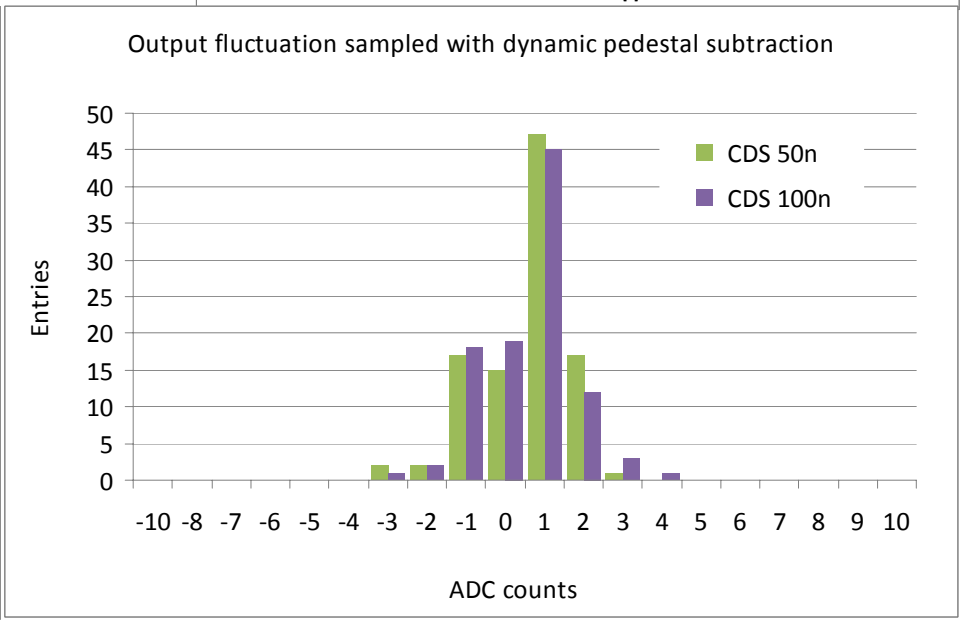
- Correlated sampling: distributon of $V(t_1)$-$V(t_2)$ to remove LF noise

Noise

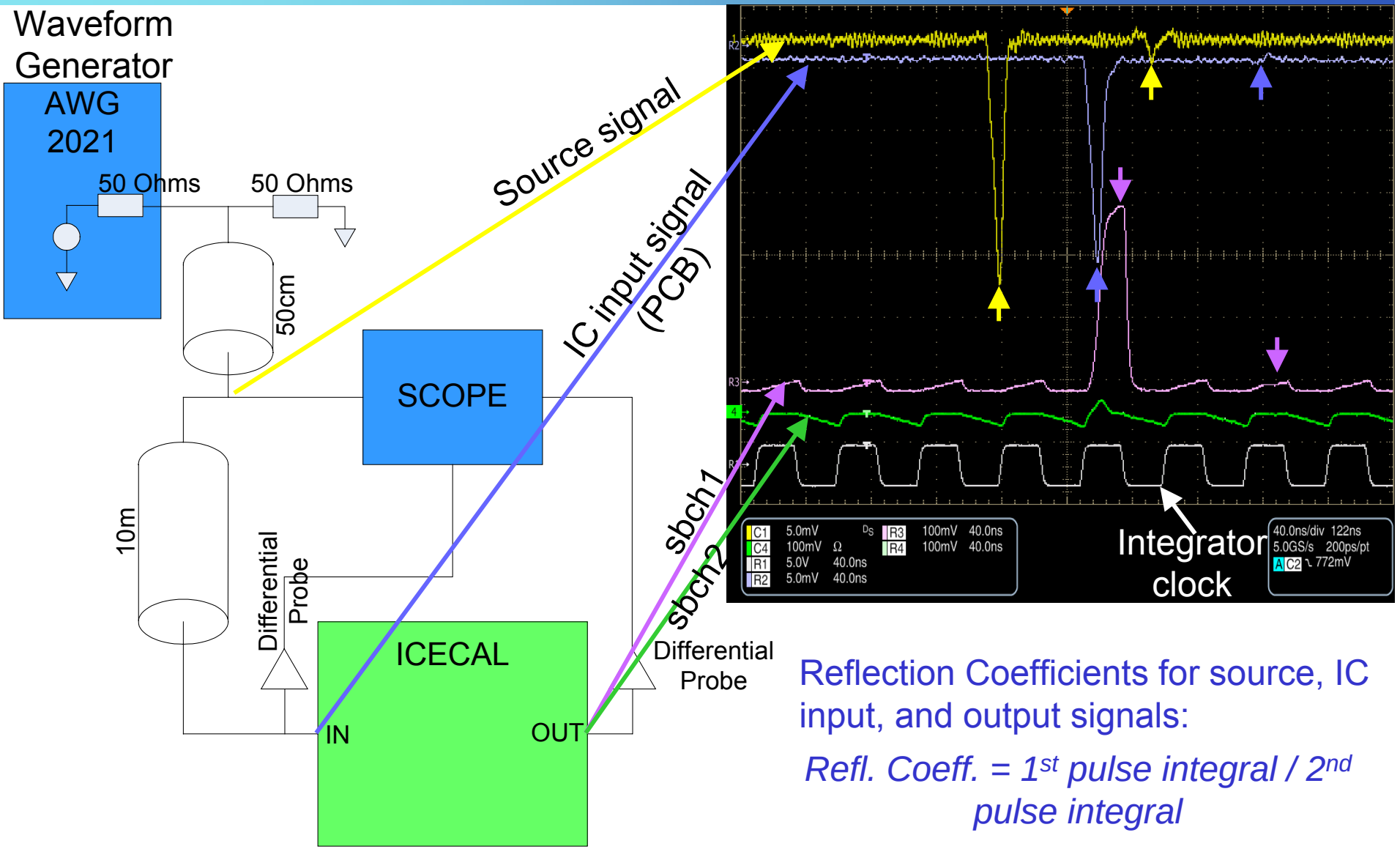
- The noise:
  - Generate a histogram of the voltage value by the end of the cycle (from 100 waveforms).
  - Gaussian fit => standard deviation
- Correlated Double Sampling (CDS) ↔ dynamic pedestal subtraction:
  - LF pick-up noise at measurements (chip connection/socket)
  - without CDS: 1.8 ADC counts
  - with CDS: 1.2 ADC counts (≈1 ADC count from simulations)







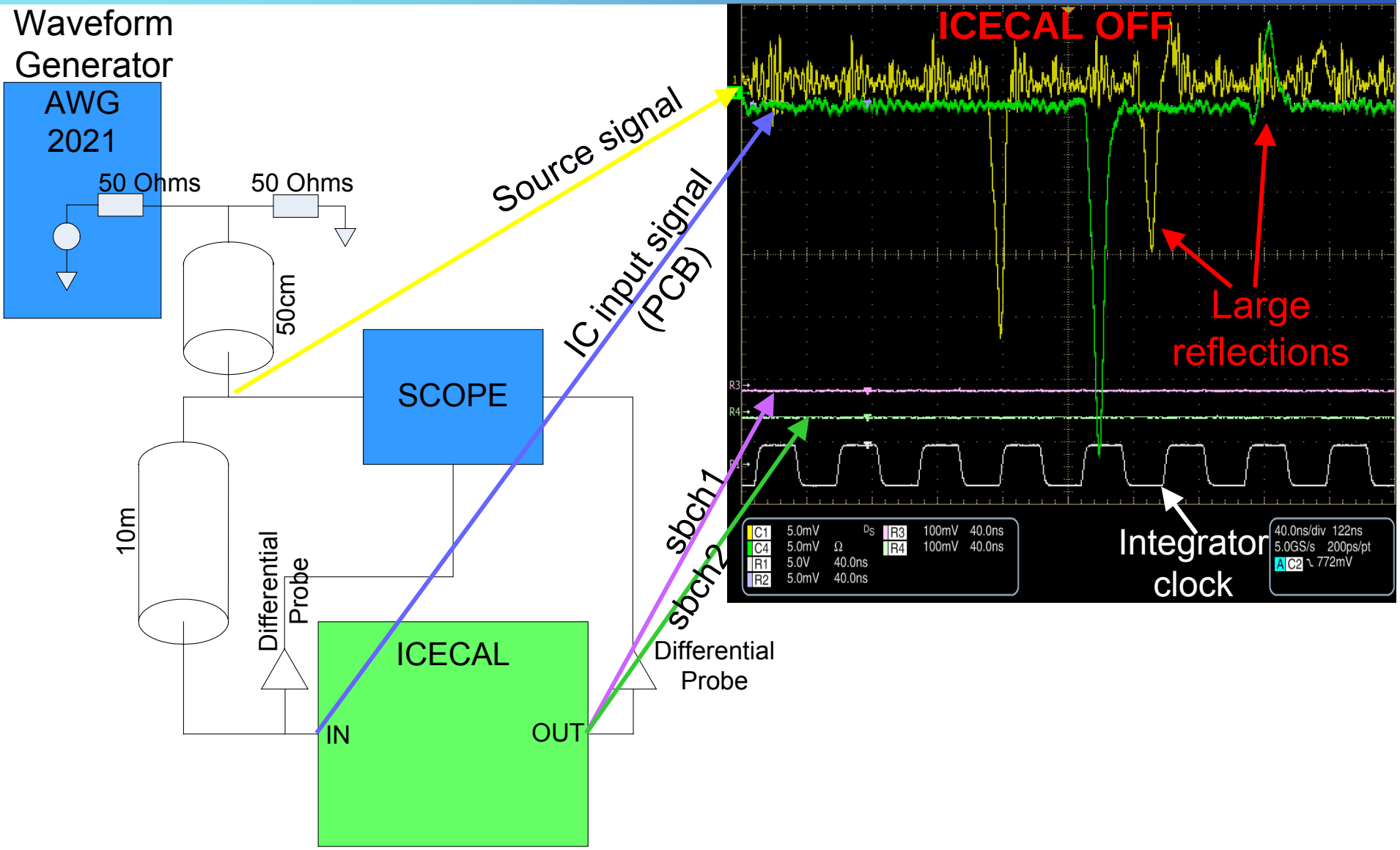
Input impedance



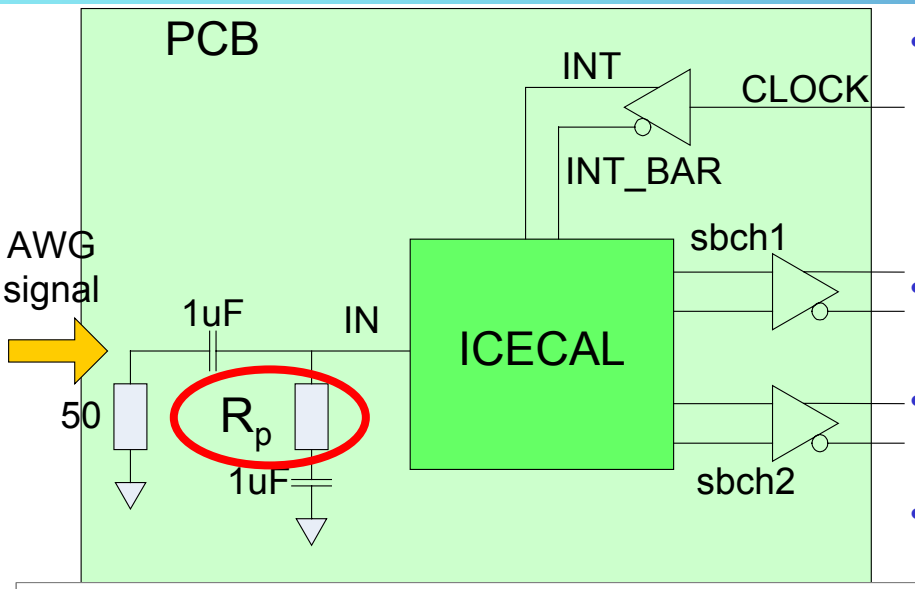
Reflection Coefficients for source, IC input, and output signals:

Refl. Coeff. = 1st pulse integral / 2nd pulse integral

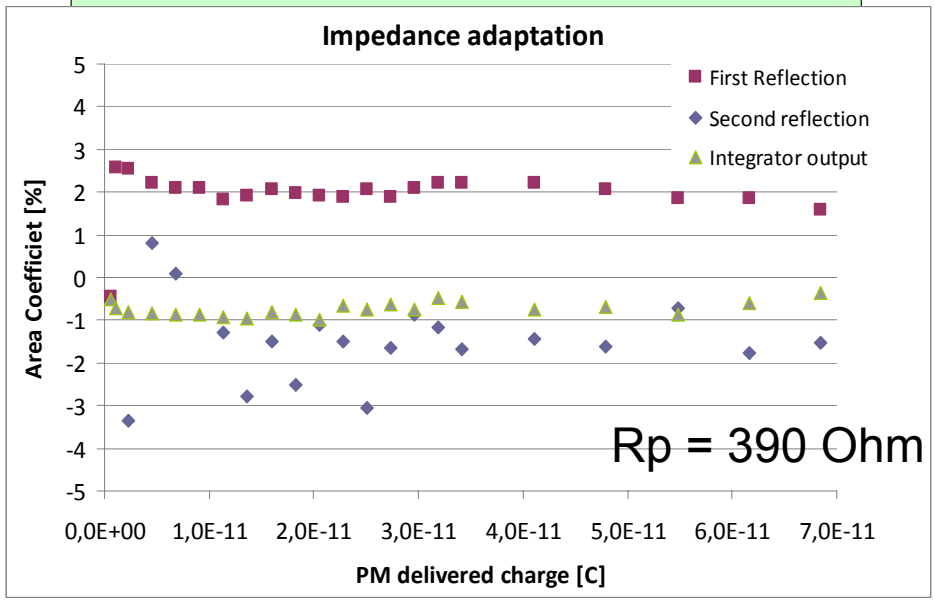
Input impedance

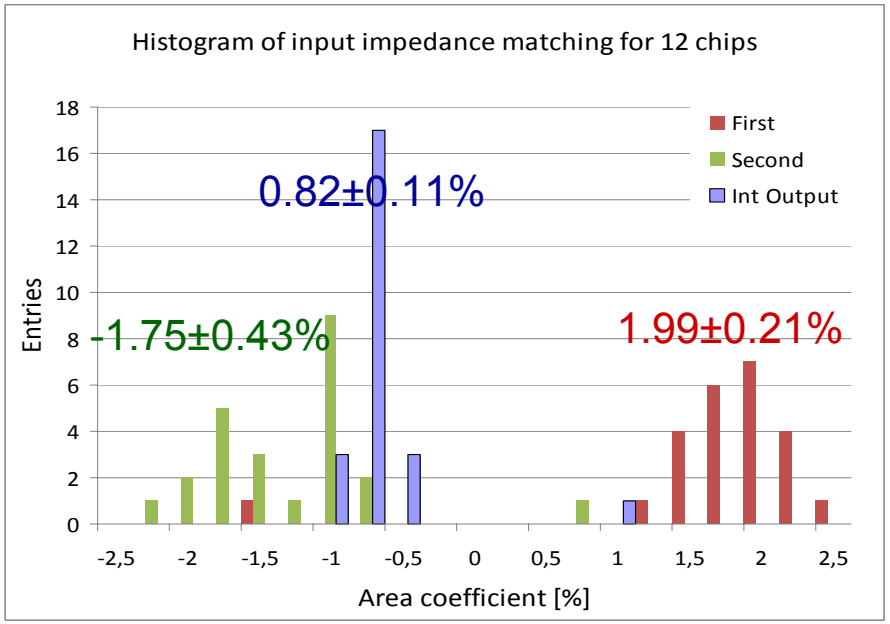


Input impedance

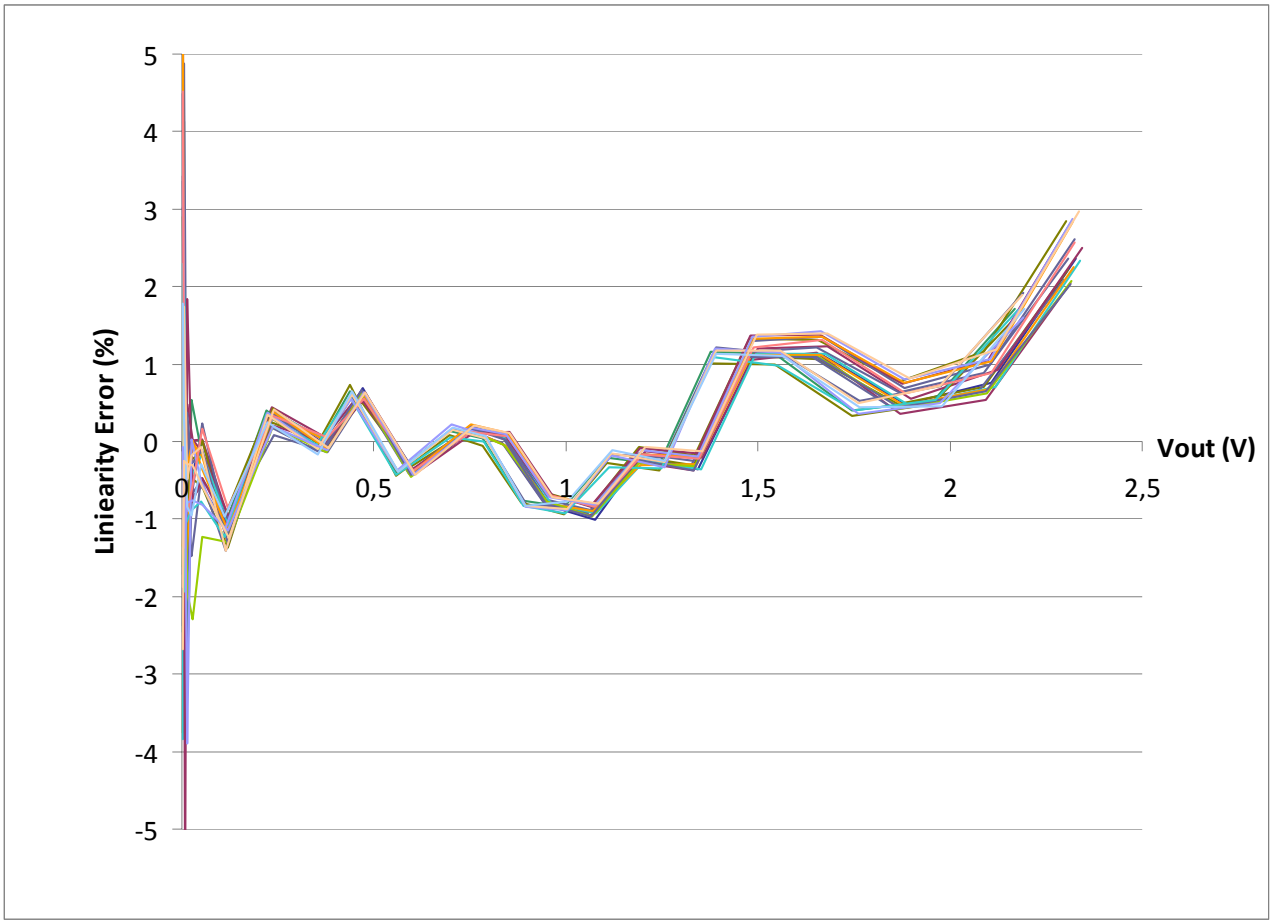


- PCB input circuit with AC coupling with Rp:
  - Zin a little higher than 50Ω
  - Rp used to fine tune Zin
  - Optimal Rp is between 360 and 390 Ω
- Dynamic variation of input impedance is << 1 % for full dynamic (50 pC)
- Measurement error for second reflection is quite high for low amplitudes (diff probe noise)
- Low Refl. Coef. dispersion < 0.5%





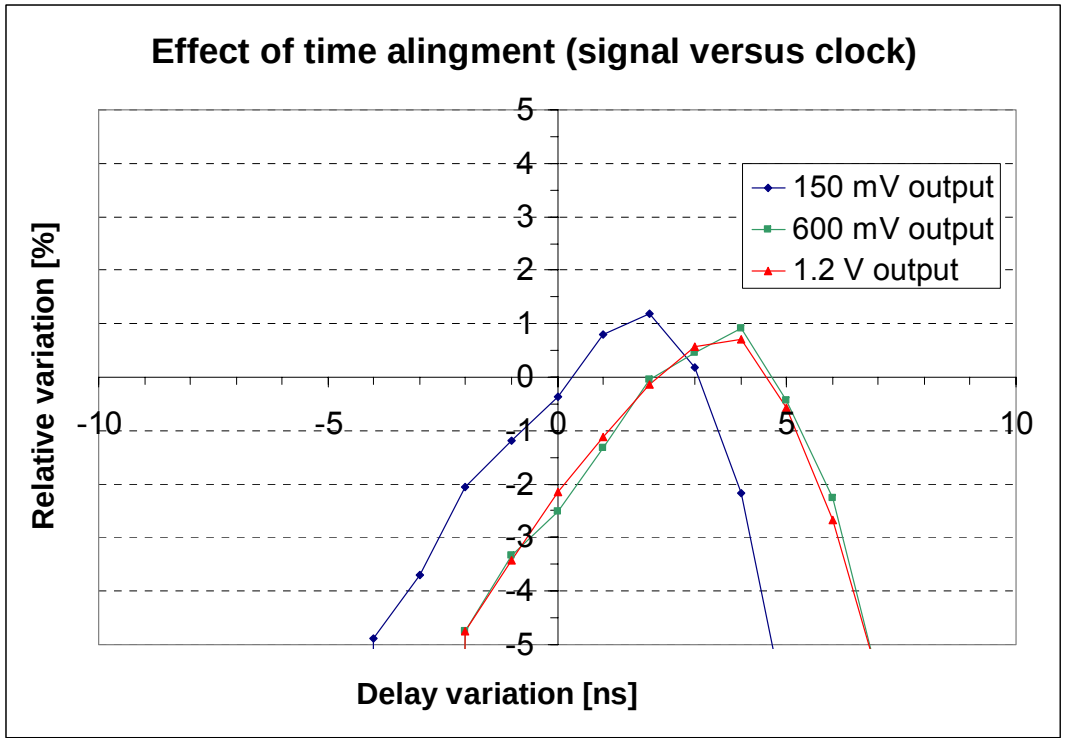
Linearity



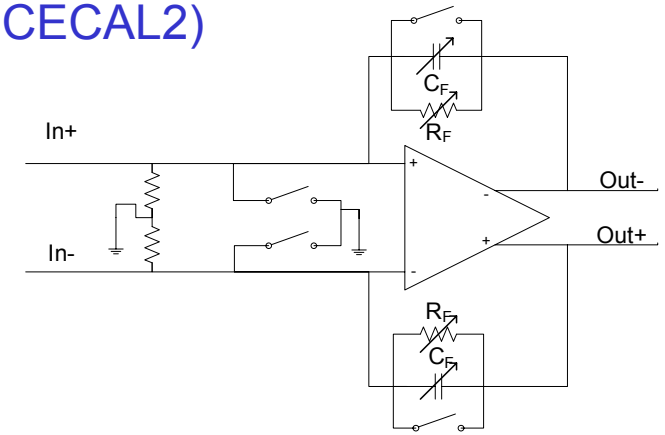
- Relative linearity error < 1%
  for the full range (2V)
- Error is large for very low amplitude values
- Attenuator and WaveCatcher offer better linearity but the differential probe may need calibration

Plateau at the integrator output

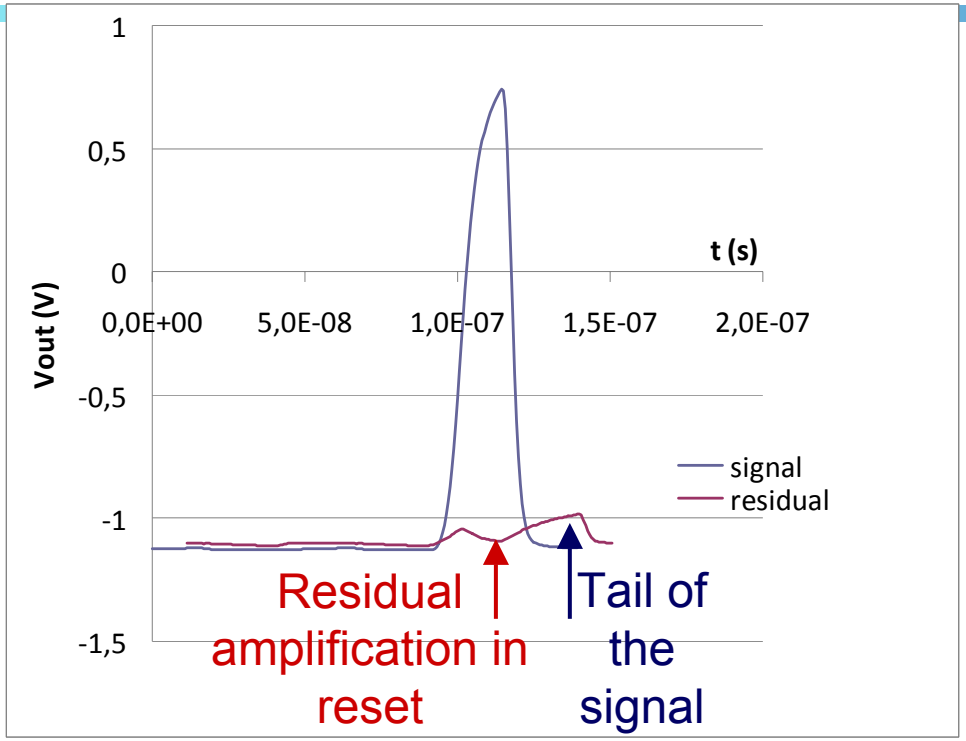
- Due to clock jitter, the signal at the output must be stable (<1%) for 4 ns.
- Input signal AWG generated similar to clipped.
- Method:
  - Delay clock signal in 1ns increments
  - Use LEMO cable



- The output variation is smaller than 1% for about 3 ns delay variation
  - Consistent for different signal amplitudes
- Can be improved using a resistor in parallel to the integrator capacitor (ICECAL2)



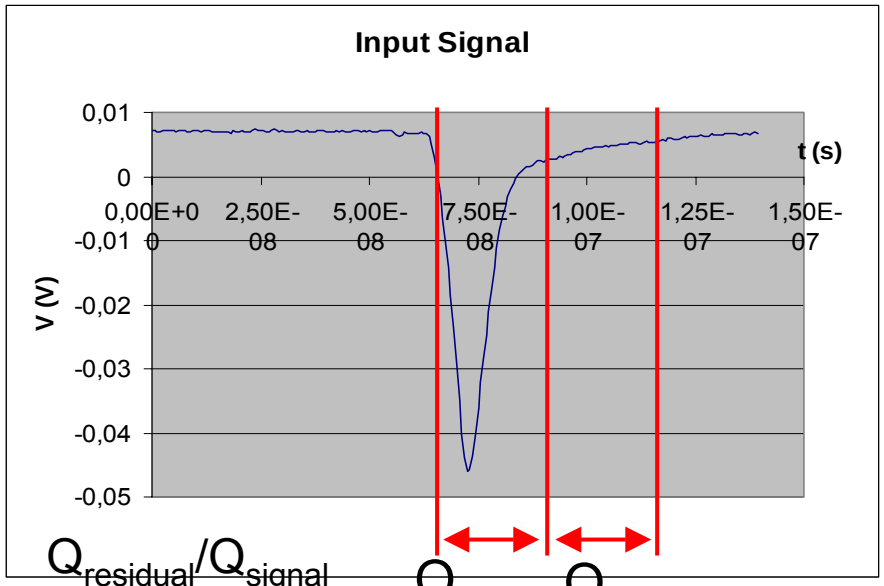
Residual Amplification (switch ON resistance)



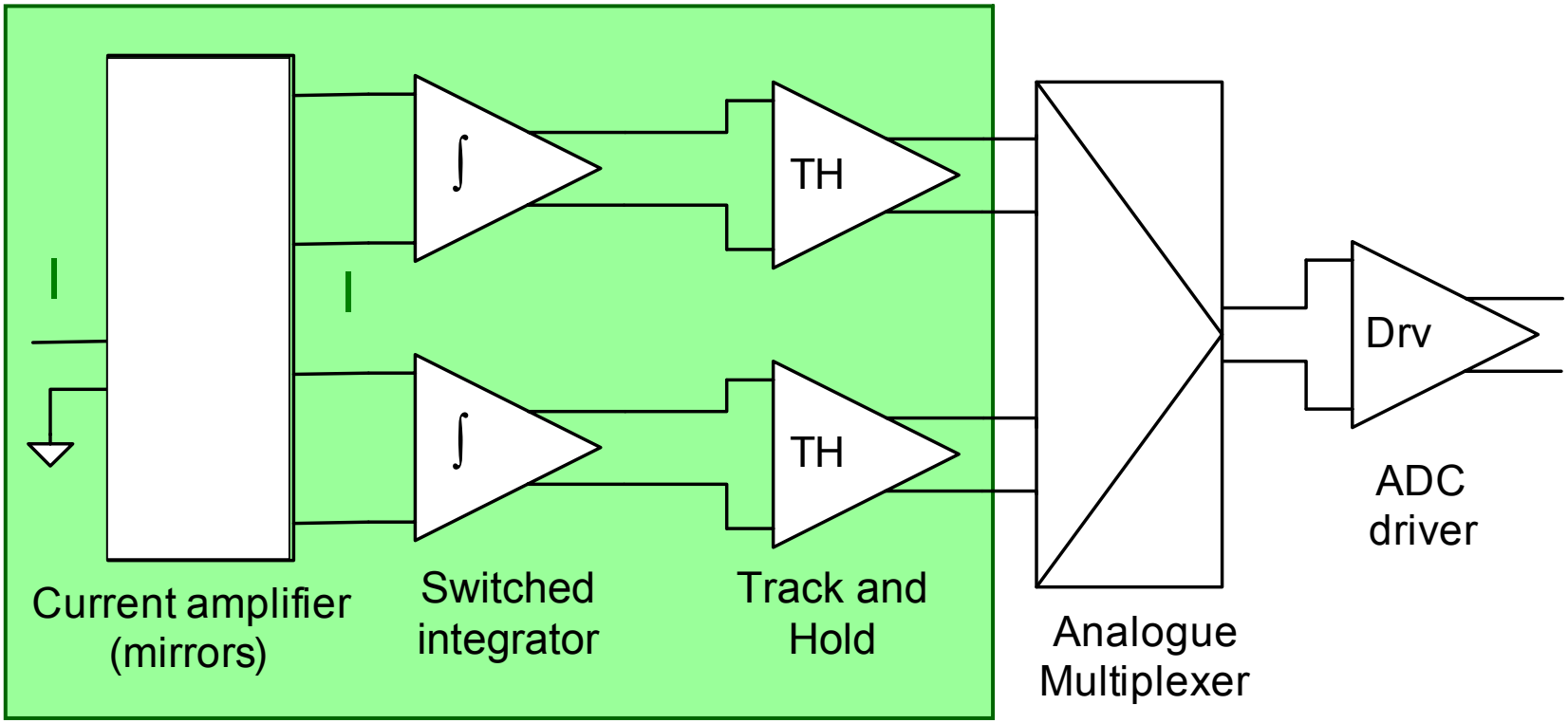
- Measure at 2 points after cycle with main signal:
  - Just after reset period (beginning of integration period)
  - End of integration period (effects of the tail of the signal)
    - Clipping is not perfect

    => small signal tail

- The residual amplification in reset is 2% of the main signal
- Effect of the tail of the signal:
  - Caused by the signal tail; due to not perfect clipping
  - Measured 12% of the main signal



ECAL analogue FE IC: channel architecture



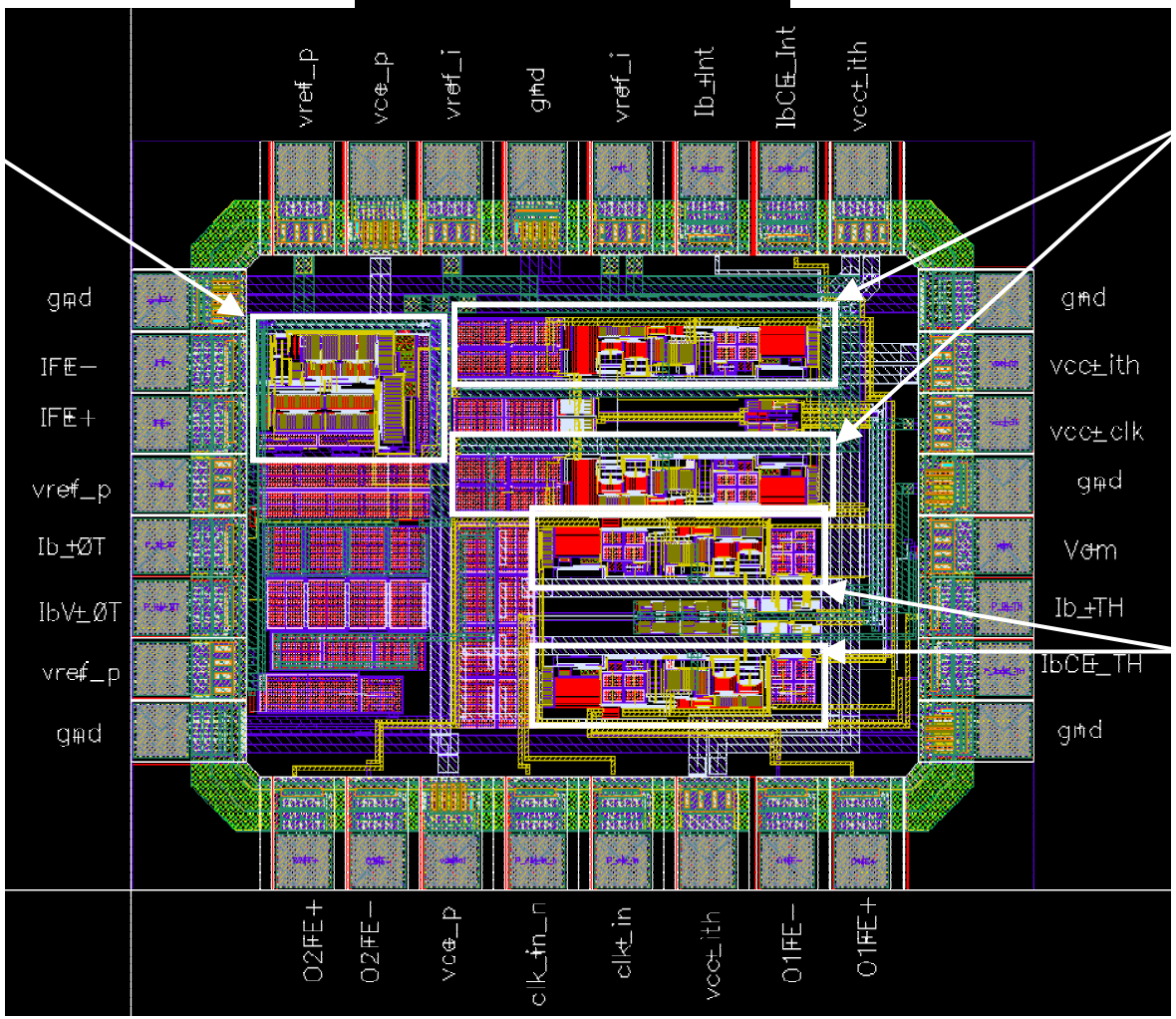
Second Prototype:
ICECAL2

Second Prototype

ICECAL2 chip

SiGe BiCMOS 0.35um
AMS 2 mm²
Submitted: June 6th 2011

Current preamp



Integrators

Track-and-Hold

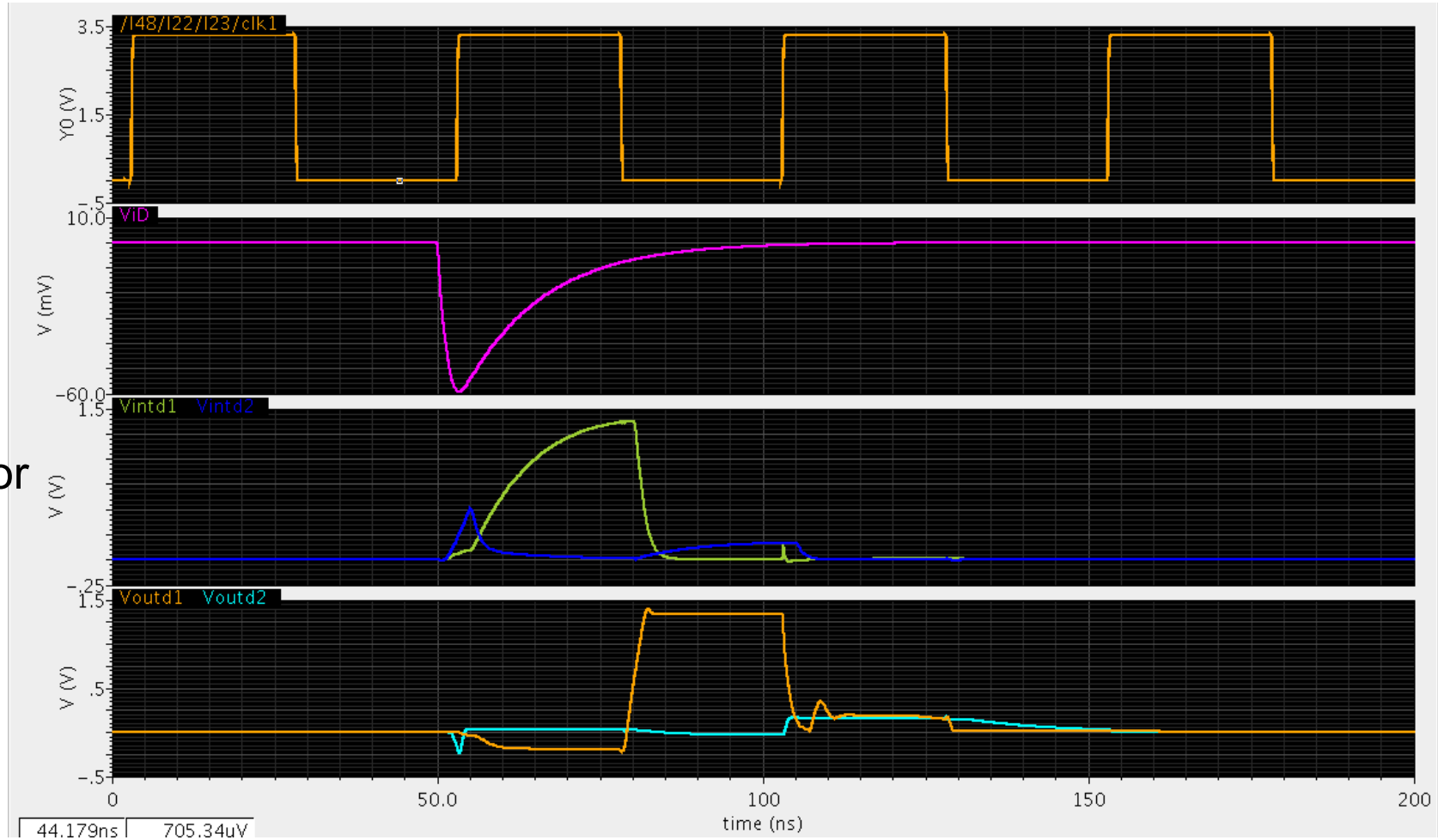
Second Prototype

Clock input

Input signal

Integrator output

TH output



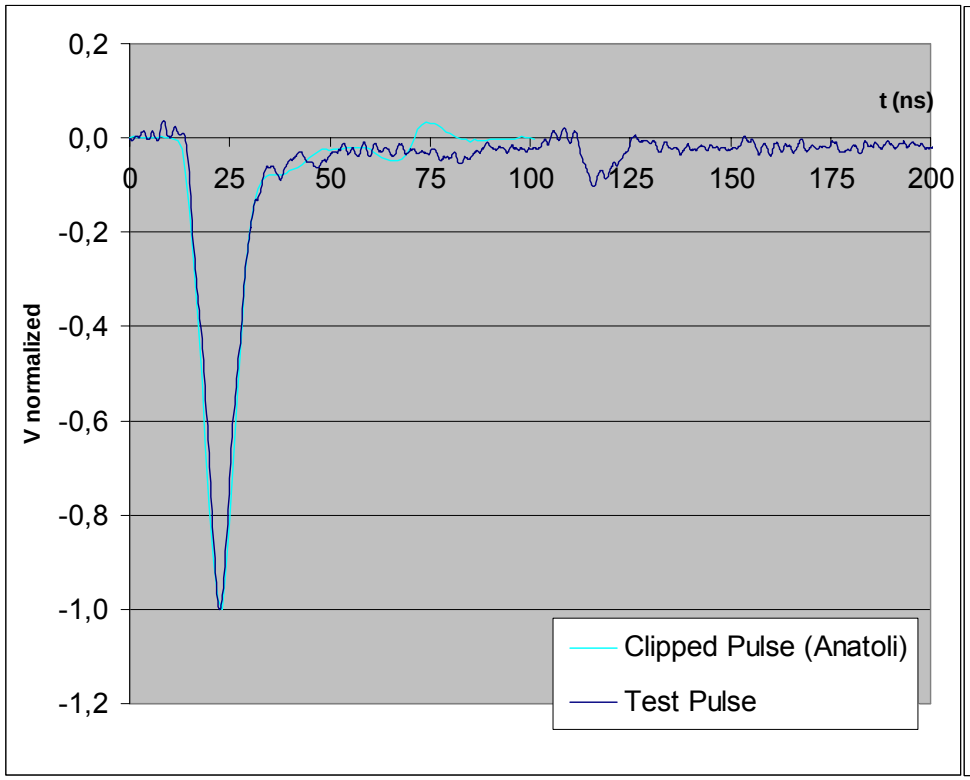
Summary

- Measurements of the first prototype of the input stage (preamp+integrator) are about finished
  - Principle is ok
  - Good results with 12 chips statistics
  - Need to study the effect of bias (op. paint) variation
- A second prototype was submitted in June
  - It includes: preamp + integrator + track-and-hold
  - Added a feedback resistor to improve the integrator output stability
- We are preparing a new set-up: AUTOMATIZED IN CAT
  - Analog mezzanine including ICECAL+ADC
  - Calibrated and programmable attenuators
  - 12 bit 500 MHz (3 GS/s) DAQ: WaveCatcher

Back-up:

Test set-up

Waveform Generator signal vs. Measured clipped signal (Anatoli)



Fast pulse (no tail) to measure reflections