Electronics Upgrade Meeting

Analog Electronics

COTS design
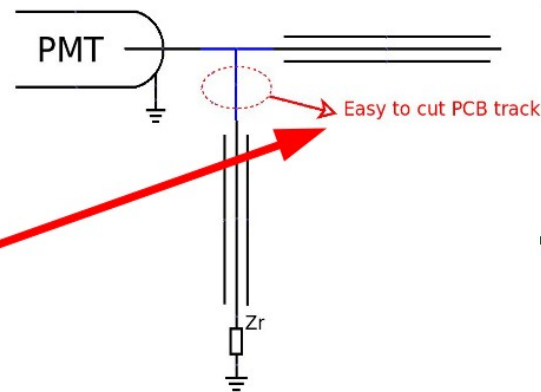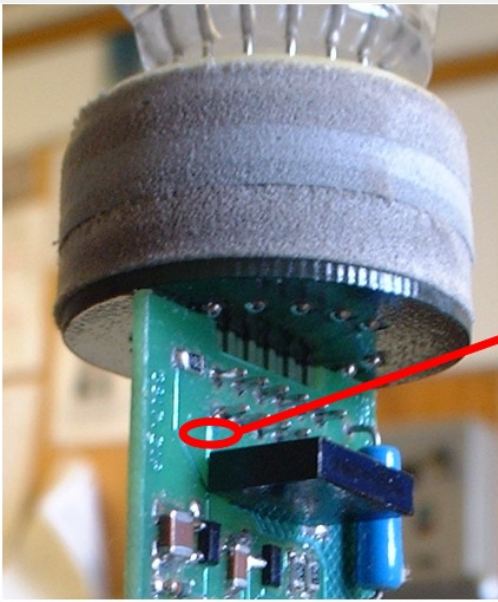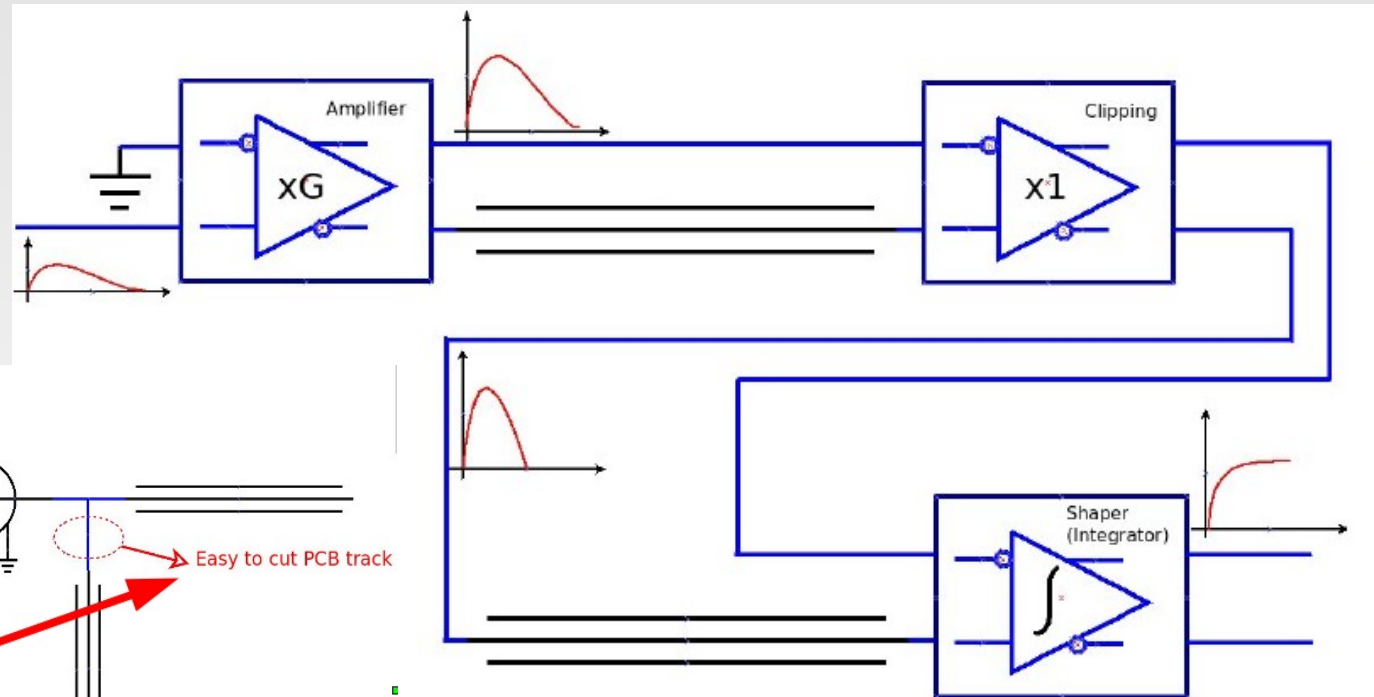
21/07/2011

Summary

- COTS approach

- Schematics

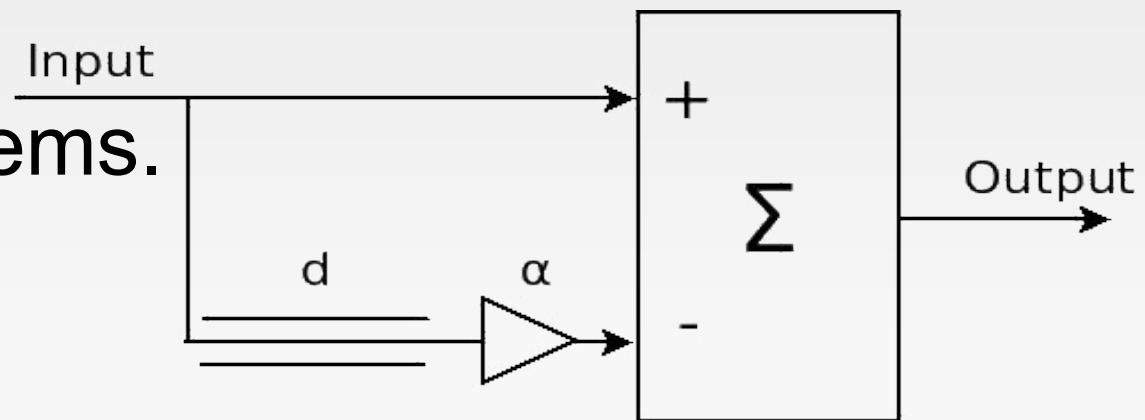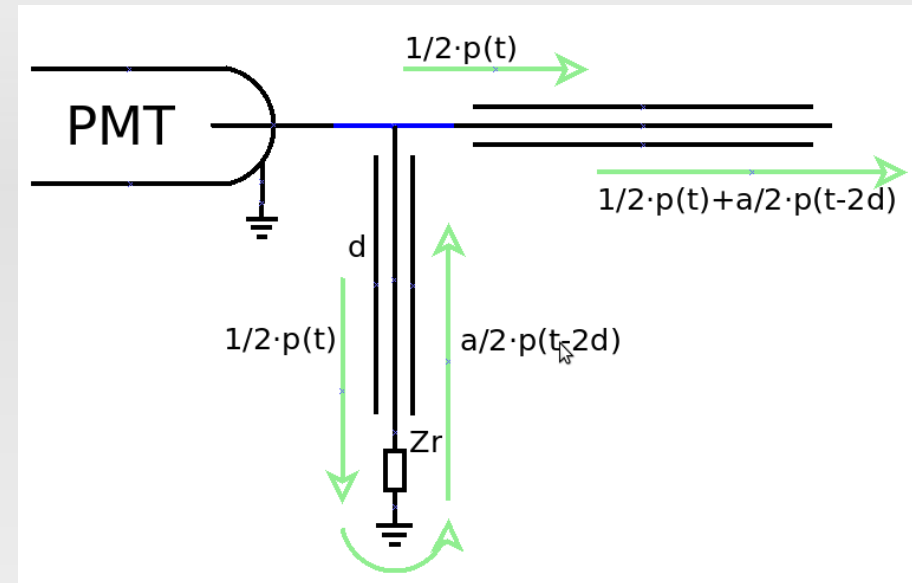- Board

- Measurements

- To do

COTS approach

- Noise requirements impossible to achieve with commercial components.

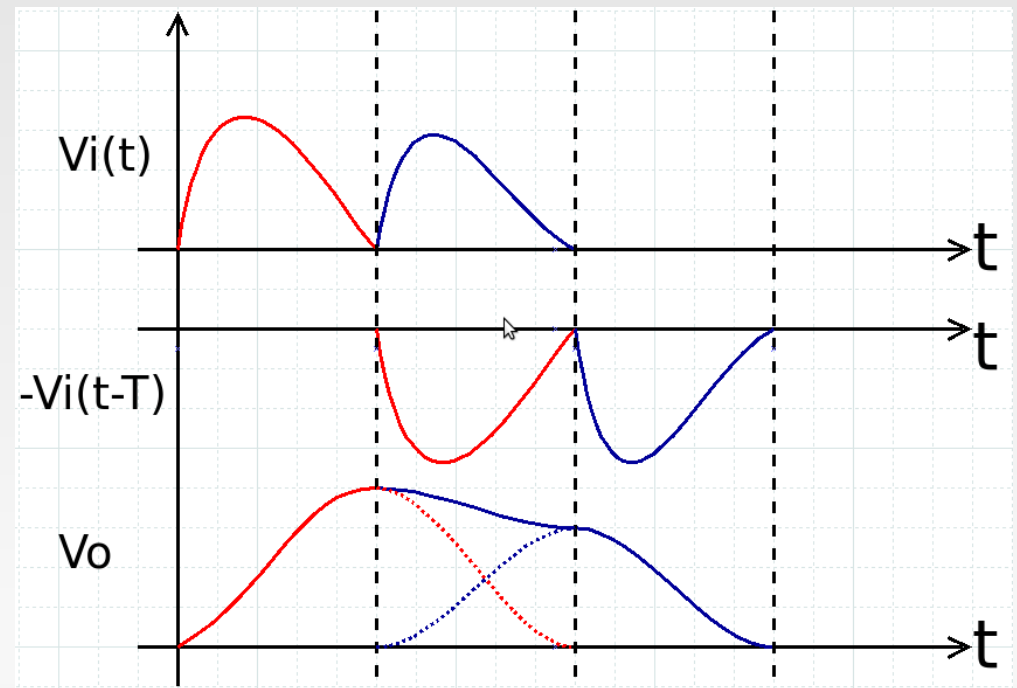- Friis rule -> need to amplify before doing any other operation.
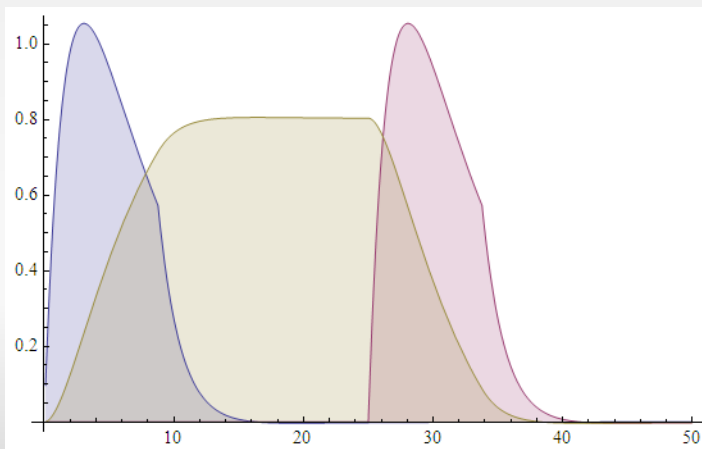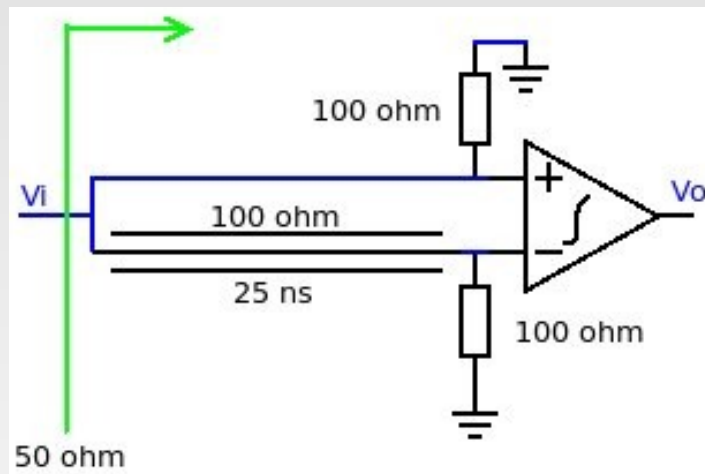
Different Clipping Approach

- Clipping after amplifying → Impedance problem

-

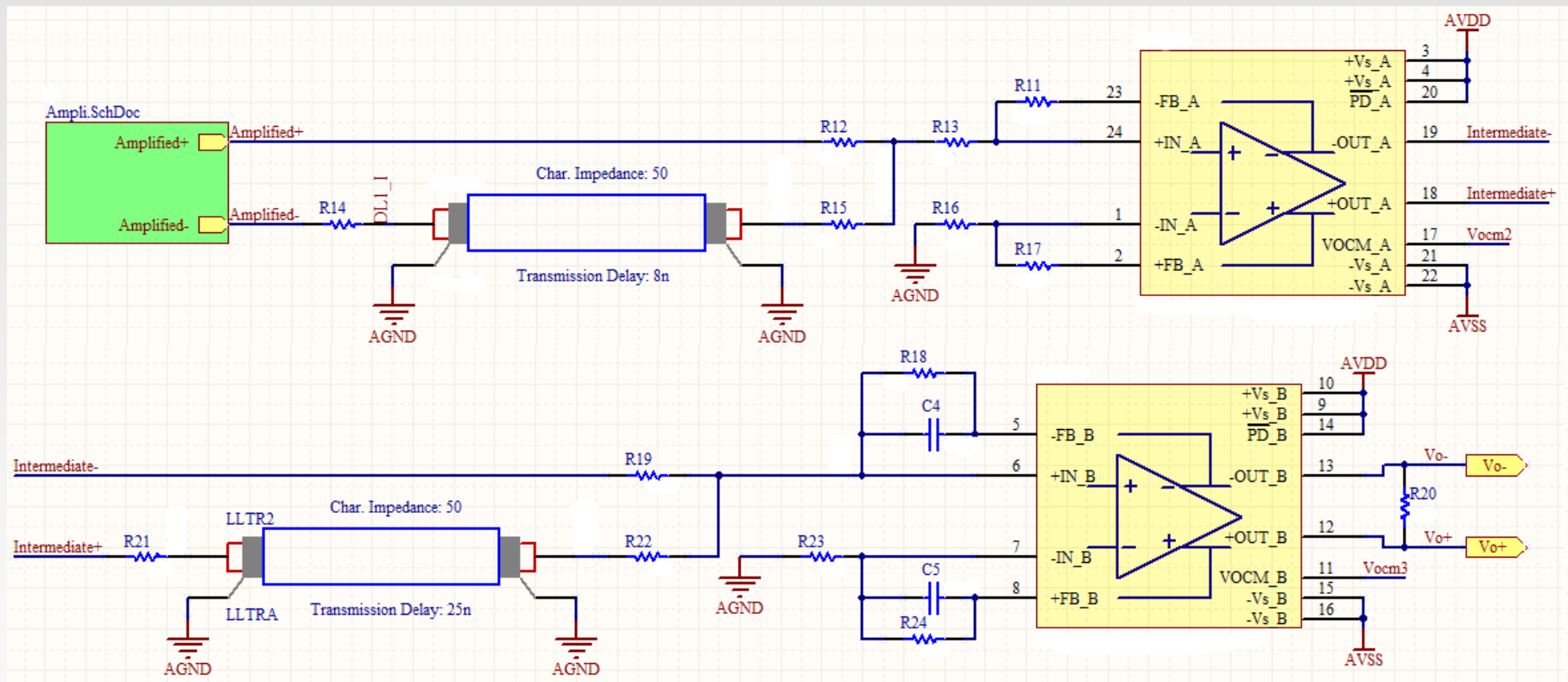- Equivalent system found, same impulse response but no impedance problems.

Same Integration system

- Integration
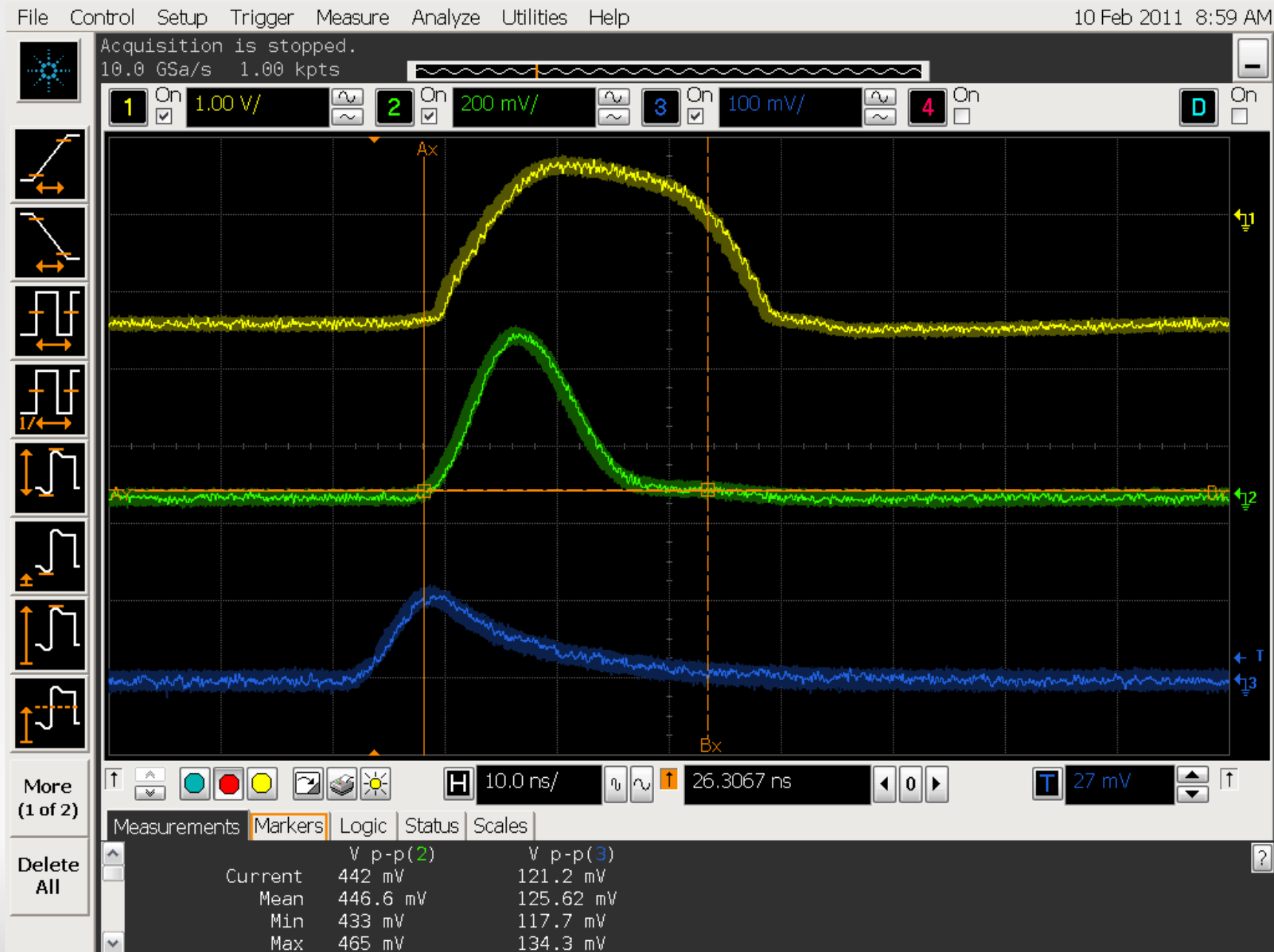   - Delayed Lines Integrator as in the current CALO

Schematics

- The COTS scheme requires 3 OP amps and 2 delay lines per channel

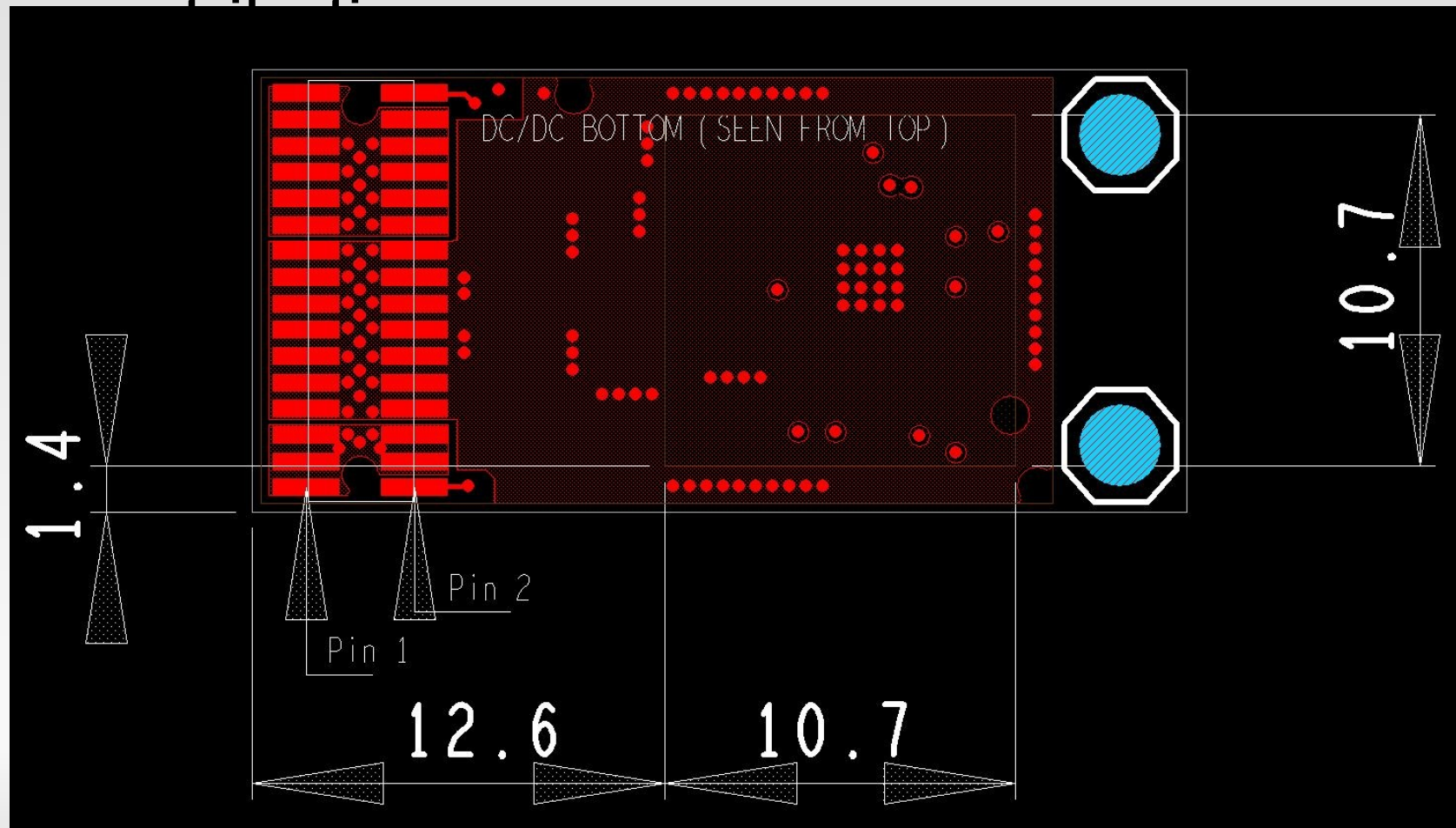# Preliminary measurements

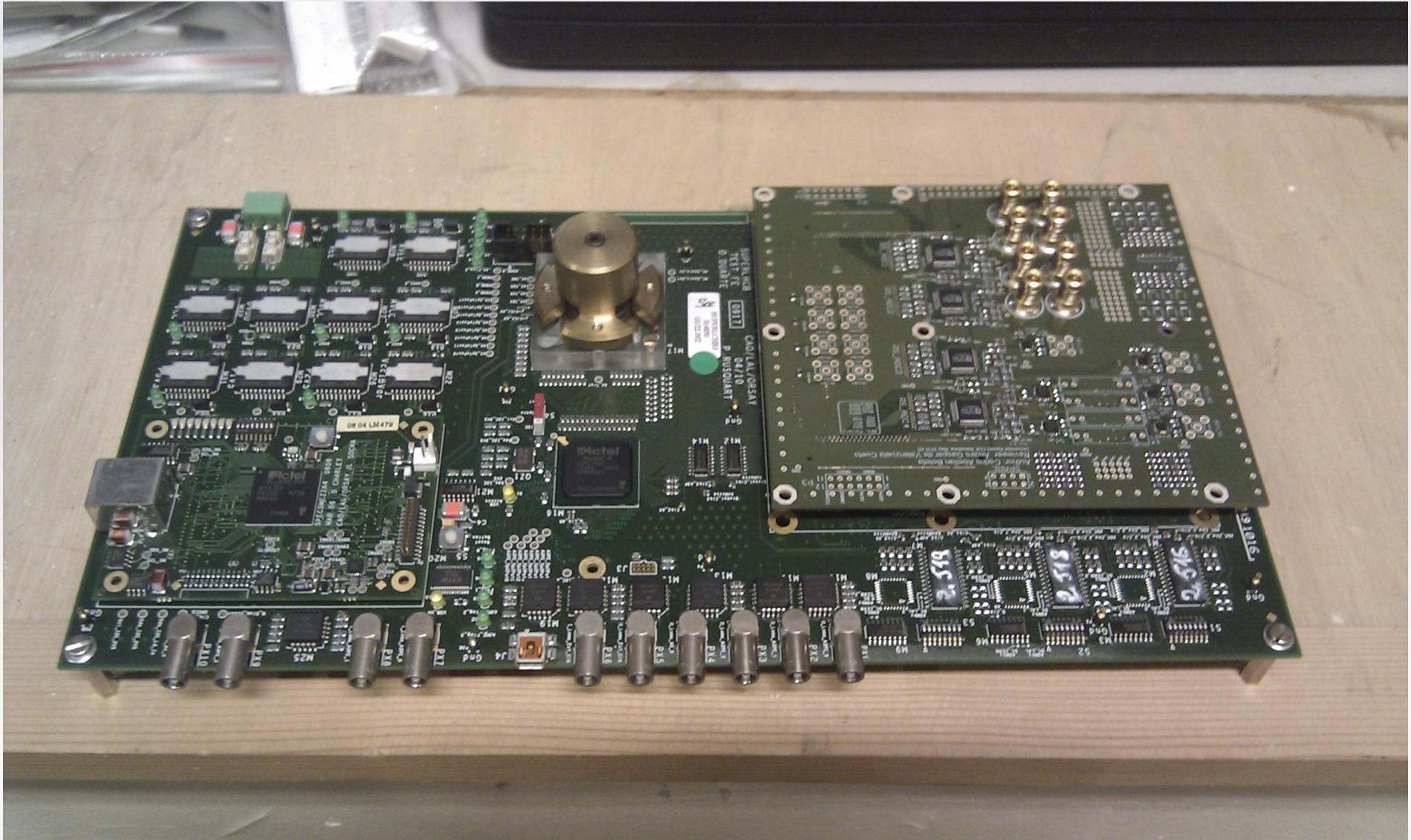# DC-DC converters

- Able to test DC-DC converters produced by CERN to evaluate possible noise

DC/DC BOTTOM (SEEN FROM TOP)

Pin 2

Pin 1

1.4

10.7

12.6   10.7

Mating connector: SAMTEC CLE-116-01-G-DV-A (female)
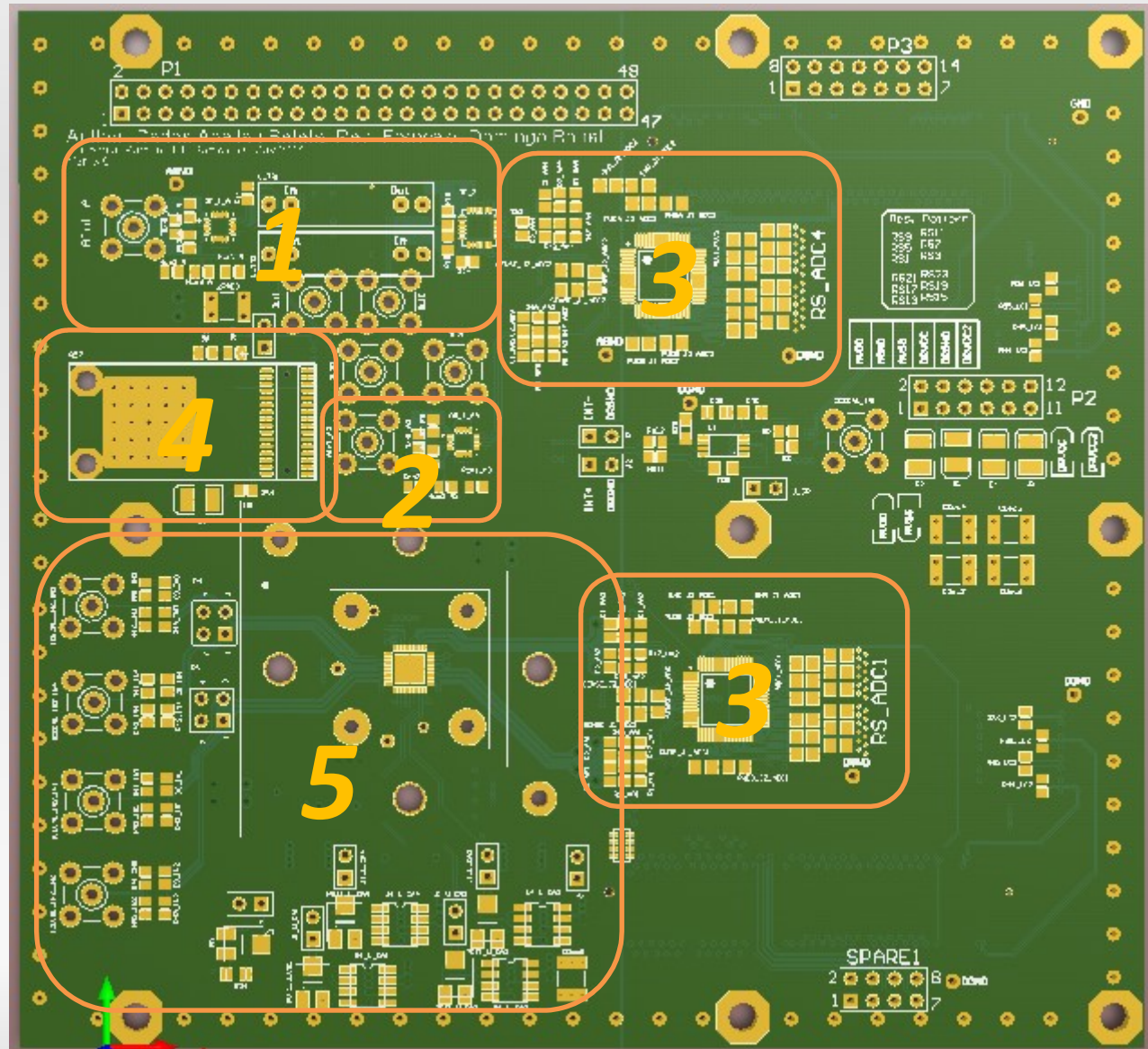
First Set of Prototypes

First Set of Prototypes

1. Analog Design
2. ADC test zone
3. ADCs
4. DC-DC converter
5. Switched Design
    (ASIC)
6.

10 Layer board
Stack:

70um conductors
100um FR4 for supplies
(better interplane capacity)
130um FR4 for external
(thin -> low crosstalk)
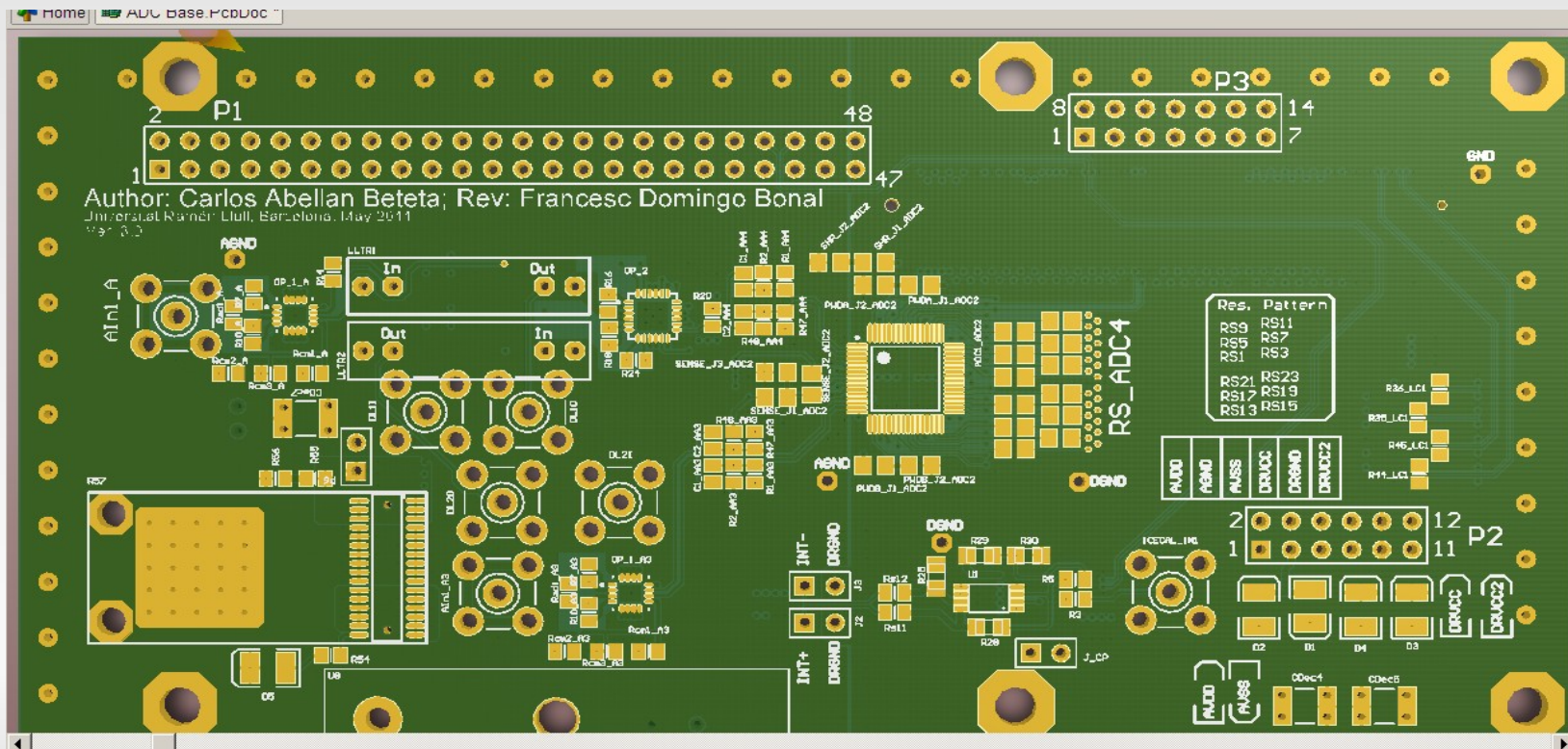230um FR4 for internal
(minimum to achieve 50Ω)

Testing

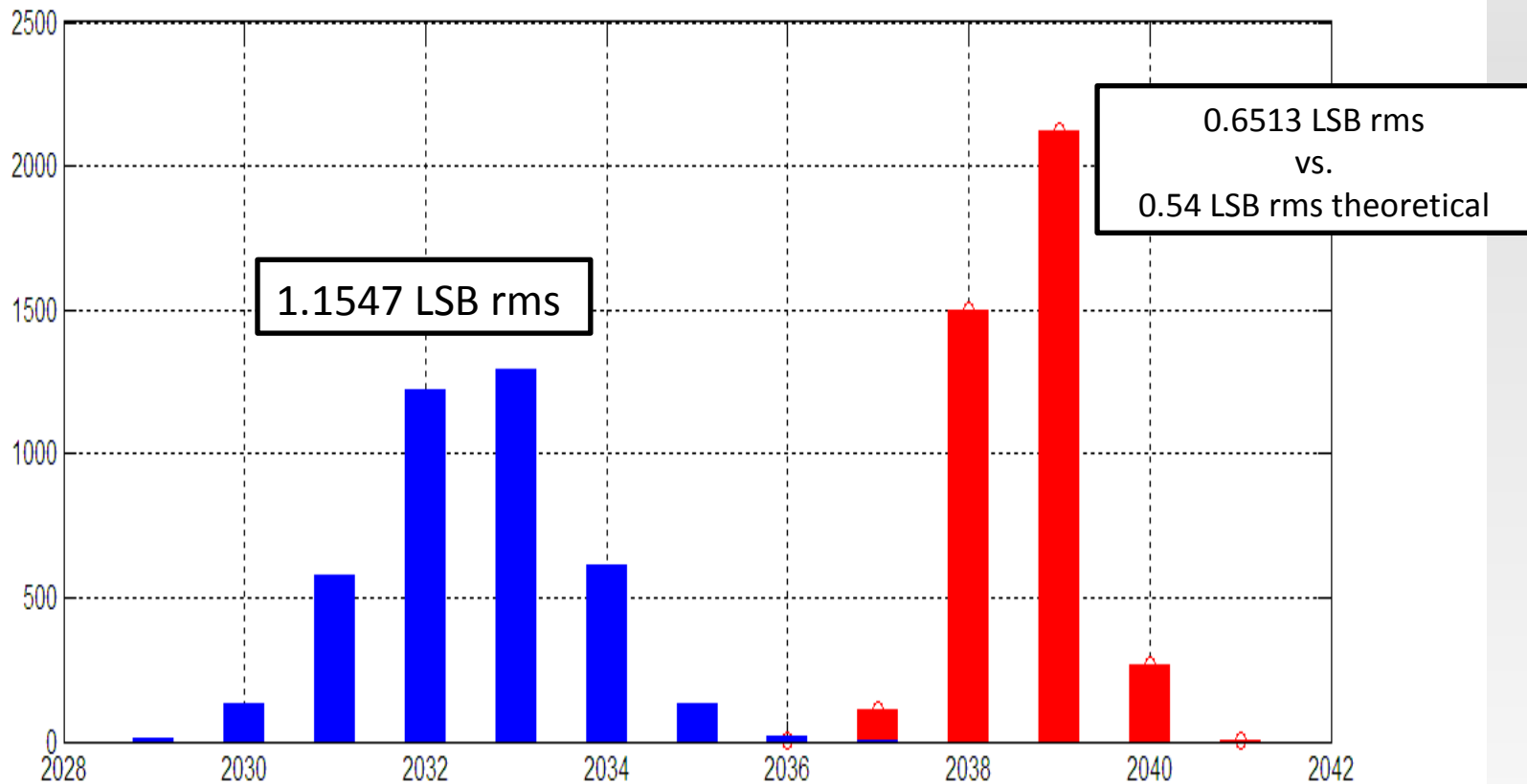On previous prototypes tested roughly analog design

On current prototype:

- In depth analog testing
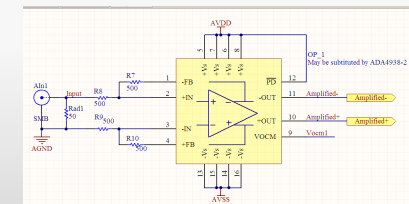- ADC testing
- DC-DC evaluation

ADC testing

First measurents with ADC reveal some noise, slightly higher than theoretical predicted one, different mean because R tolerances

4Ksamples histogram, Red with short circuit at the input, blue without the short circuit (driven by a zeroed unitary gain driver)
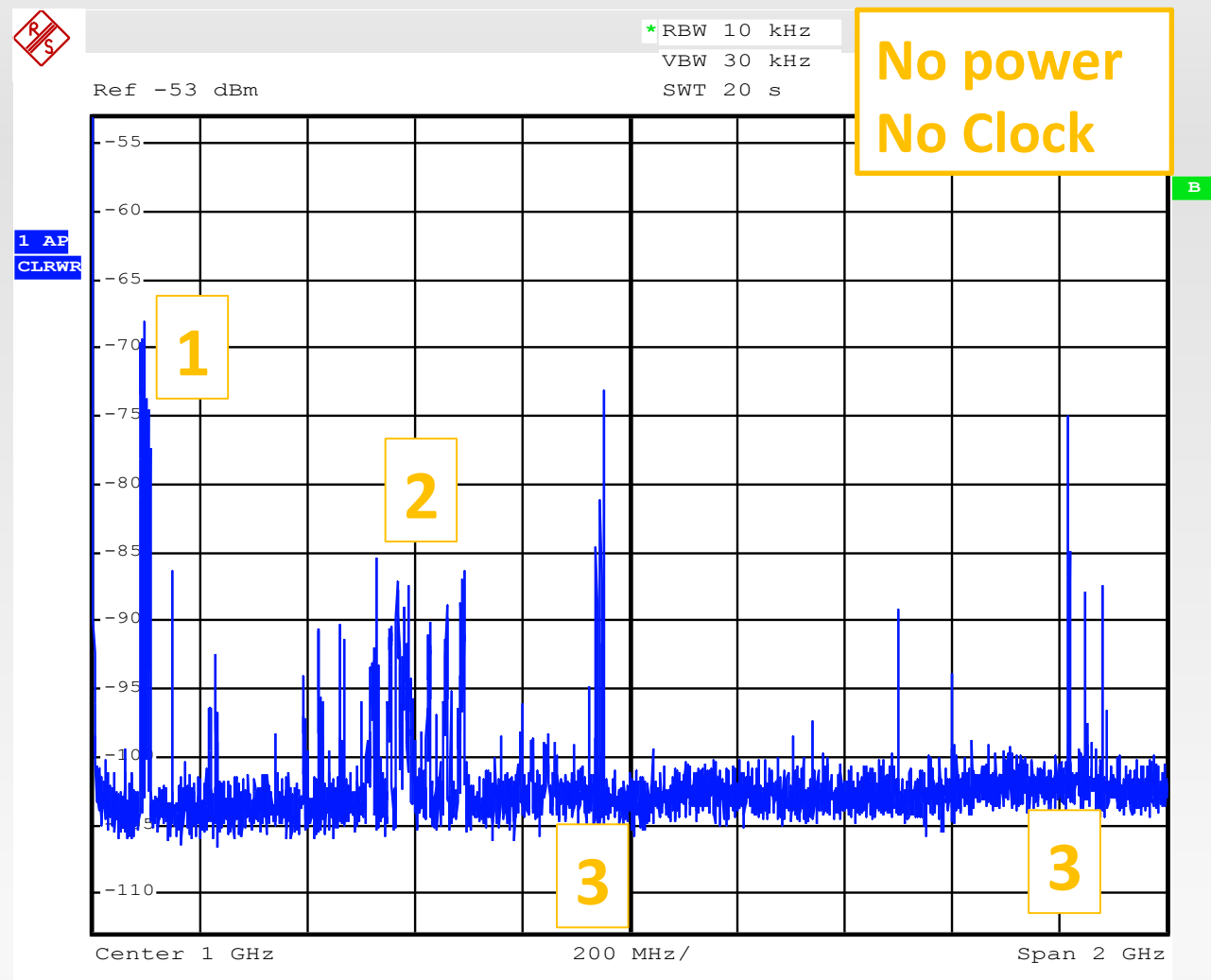
Analog power supply

Can it have something to do with the power supply decoupling?

Measured the analog supply with a spectrum analyzer.

No isolated chamber:

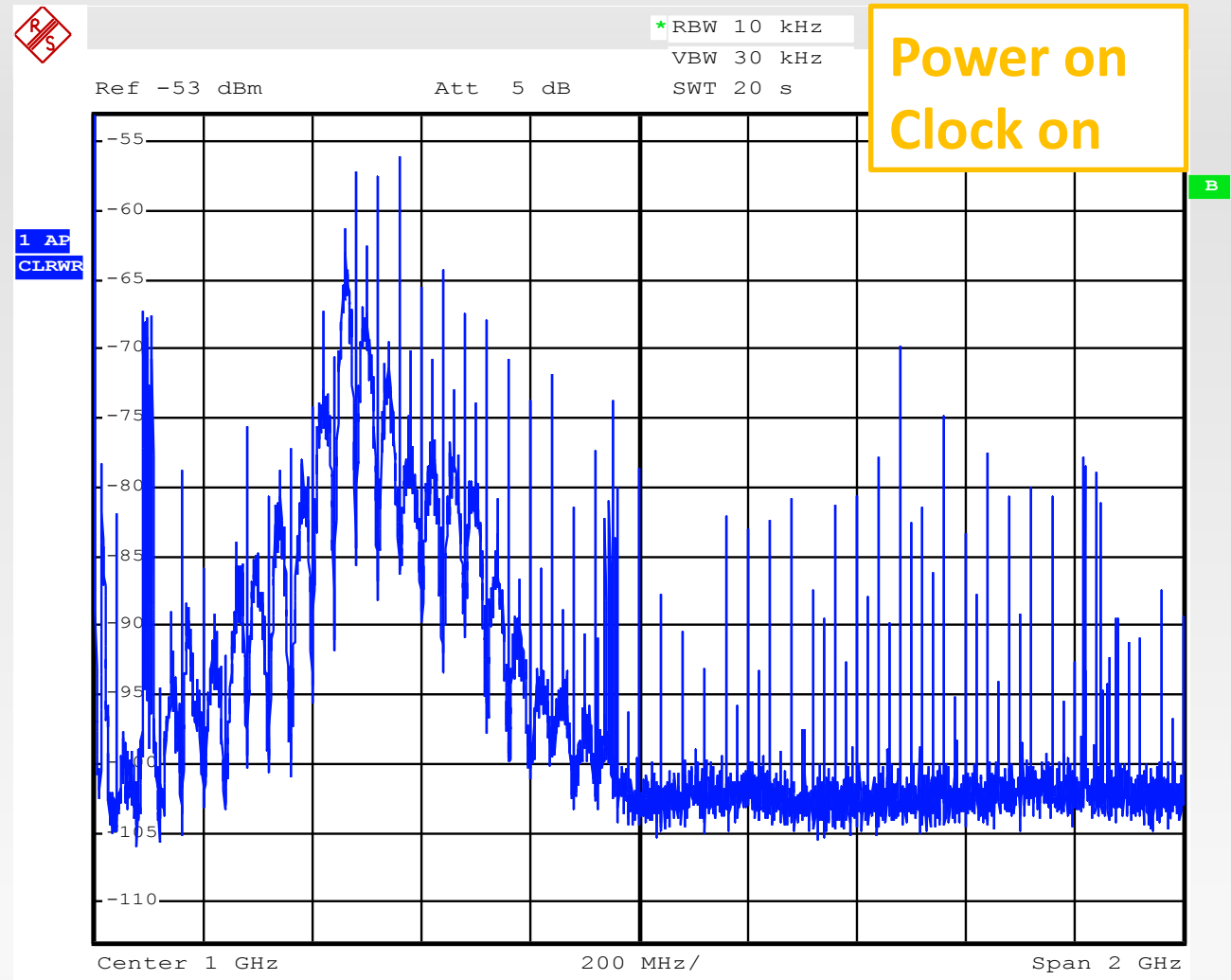   1. Radio
    2. TV
    3. Mobile phone

Analog power supply

Clock drivers' rise time ~500ps -> High frequency harmonics couple to analog supply.
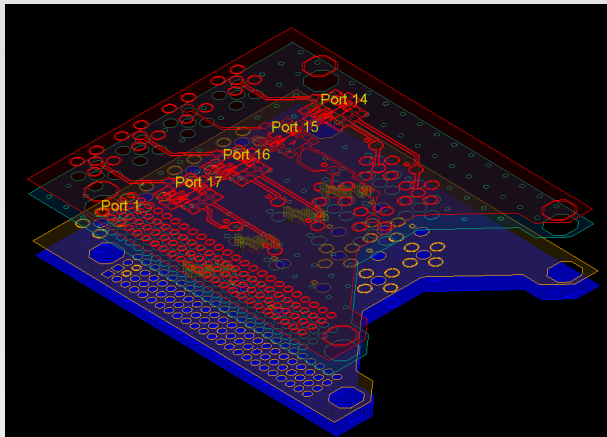
Effect disappears without clock.

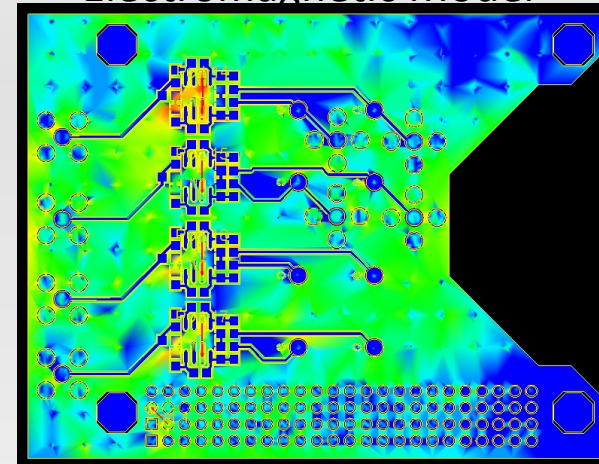Should study if digital switching could be a relevant noise source.

Power on Clock on

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Board level simulation

- Beginning Agilent's ADS simulation
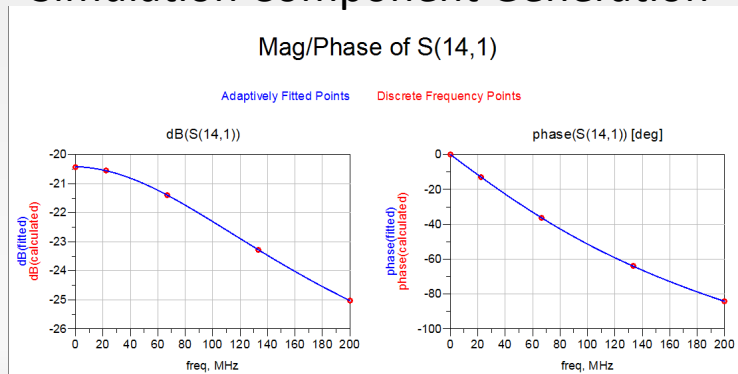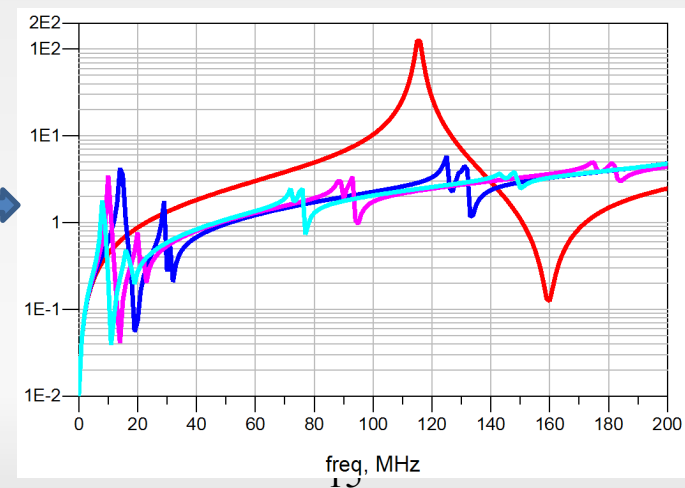
To do

- ADC test with CAT (now capturing with scope)
- In depth study of analog proposal:
    - Noise
    - Linearity
    - Pulse Shape: Planarity, Baseline,...
    - Radhard qualification
- Power integrity study (already started)
- Verify signal integrity issues (already taken into account)

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Backup Slides

First Set of Prototypes

- Schematic view