Digital Electronics and DAQ

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On behalf of the calorimeter upgrade group

LAL, Orsay

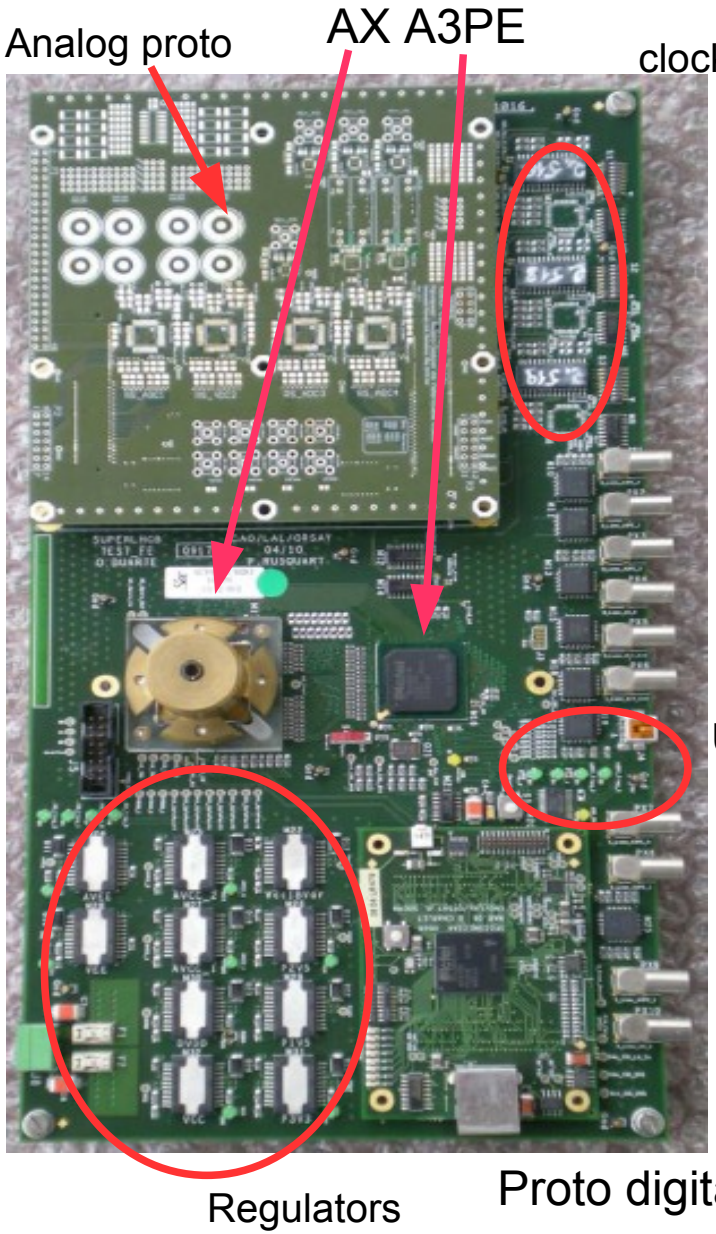
- The calorimeter electronics upgrade
  - Pending question on the SPD/PRS
    - No decision yet, but a large fraction of what is done may be used for PS/SPD
  - In order to keep the PMT alive during the upgrade period
    - Reduce the PMT gain by a factor 5
    - Need to compensate on the electronics
      - New analog part on the front-end will do it (Barcelona)
      - Noise should not be increased in the operation
      - 2 solutions
        - ASIC (David and Edu's talks)
        - Discrete (Carlos' talk)
  - Move to a 40MHz readout : change the digital part (Orsay → this talk)
    - Perform a packing in order to reduce the bandwidth needed
      - No loss of information
        - Small ADC values coded on less bits
          - Gain on the number of bits sent
          - Pay an overall format word
        - Global gain
      - 32 channels per board, 4 optical links per board→ GBT

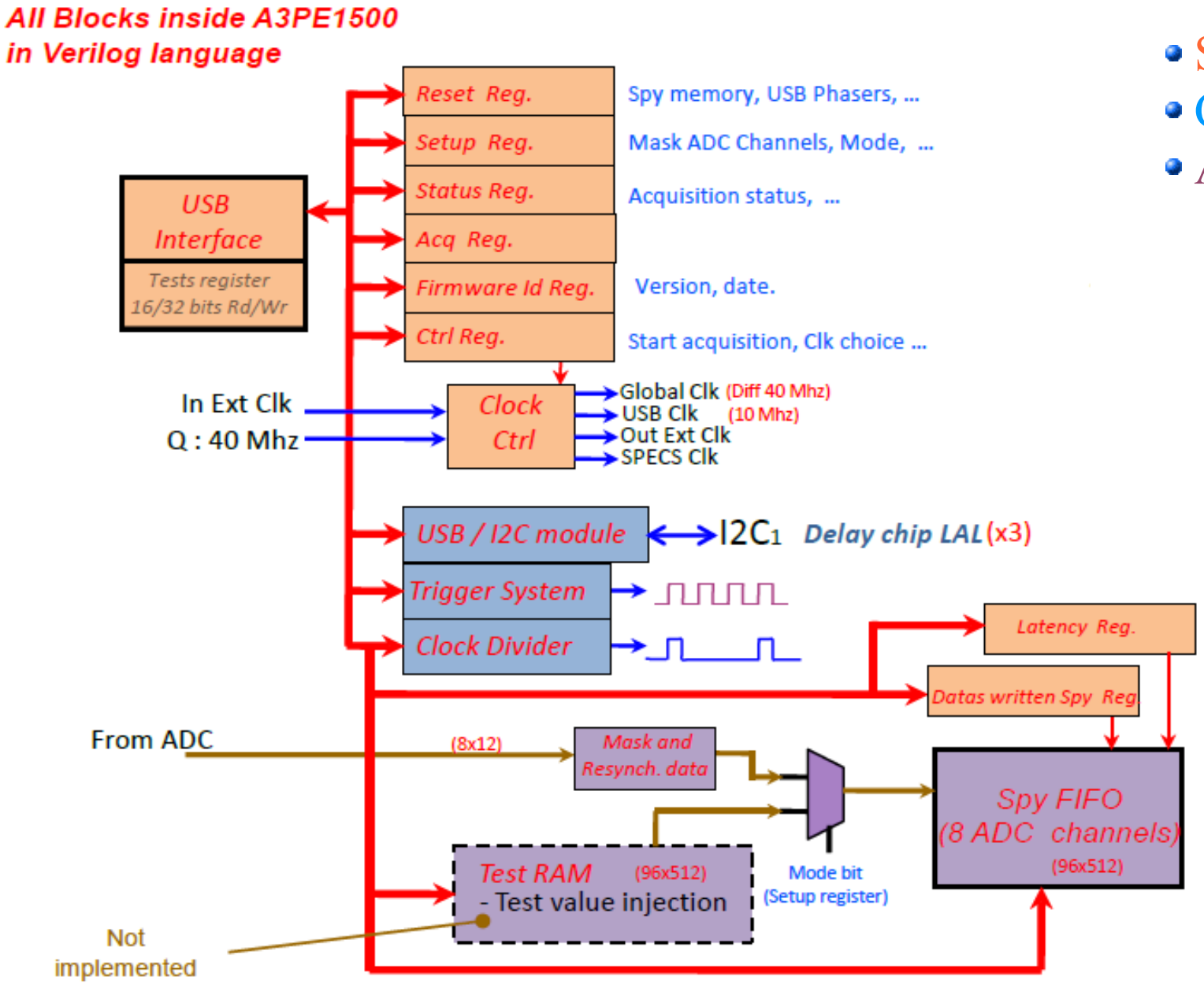
- Would like to “externalise” the fast signal part of the new FEB
  - A mezzanine plugged on the FEB would receive the 40MHz signals
    - Fast signal and GBT on the mezzanine
  - This was done with the present detector and the GOL → successful
- L0 mainly kept and replaced by Low Level Trigger → Cyril Drancourt (Annecy)
  - Send (more than) the “old” L0 information to a board similar to a TELL40
  - Information is not anymore sorted by the selection board
    - Need for an interface between TVB (cavern) and “TRIG40”
      - TVB (GOL) → TRIG40 (GBT)
- A new control board is needed in central slot to replace the CROC
- ECS : several solutions envisaged
  - Keep SPECS would be easier for us... unless we are alone
  - Another solution would be to change the firmware of the SPECS FPGA
    - SPECS → I2C would become I2C(GBT) → I2C
  - A GBT mezzanine would replace the SPECS mezzanine
  - This looks feasible but no real work on this field yet
- Power
  - We think of keeping the present power supplies (Marathon) → ok
  - We would try to replace the present regulators by DC-DC converters
    - Should be ok → to be tested

- Analog prototype
  - Supports the analog part and the ADC
  - May be powered independently
- Digital prototype
  - may receive the analog prototype as a mezzanine
  - Provides power to the mezzanine (+ trigger, ECS, clocks, ...)
  - Read the ADC output through the connector
  - Main purposes
    - Test the firmware of the digital electronics
      - pedestal subtraction, packing, ...
    - Test the viability of the A3PE solution in terms of Bit flip rate, number of I/Os
      - Previous generation of flash ACTEL was not very reliable for
        - Fast and numerous flipping I/Os
      - Hosts an AX to test A3PE
        - many I/Os of the two are interconnected
      - AX could also be thought as a backup solution
        - optimistics : ressources limited
    - Helps in the analog testing → provides an acquisition tool
    - Possibility to perform radiation tests in beams
    - Test power scheme (DC-DC converters)

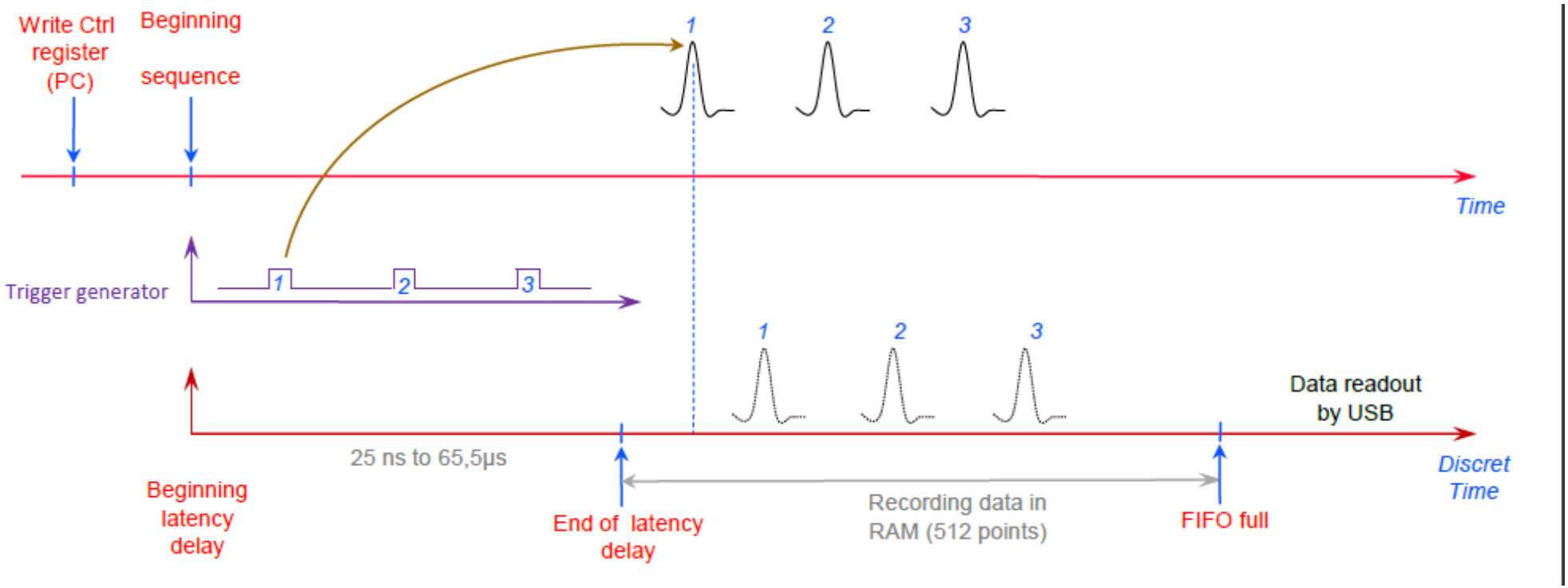
- The prototype exits
- Main things to do
  1) Have an acquisition system for the analog (USB)
  2) Implement/Test digital functionalities (packing)
  3) Test the A3PE FPGA
- What has been done
  - 1) is mostly OK, need integration with Barcelona analog part. A prototype has been given.

  - 2) is not fully written (firmware) but is well advanced
  - 3) nothing has been done yet
- Power supply is also an issue → tests have to be done



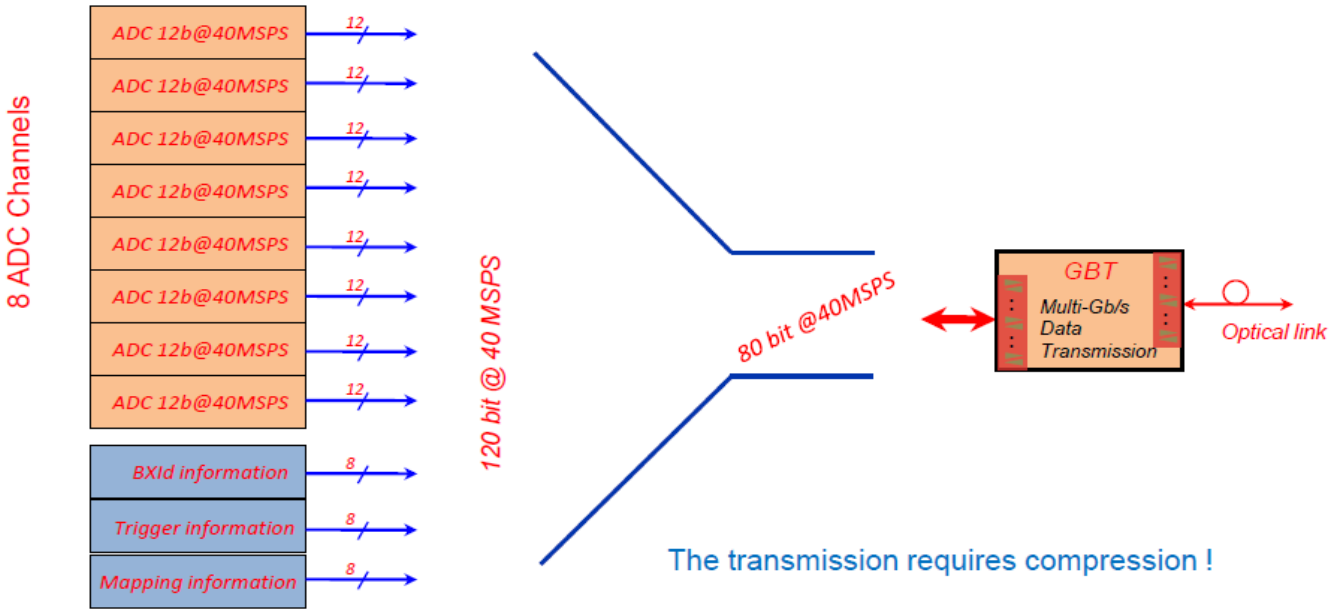


- Slow control
- Clock, trigger
- Acquisition



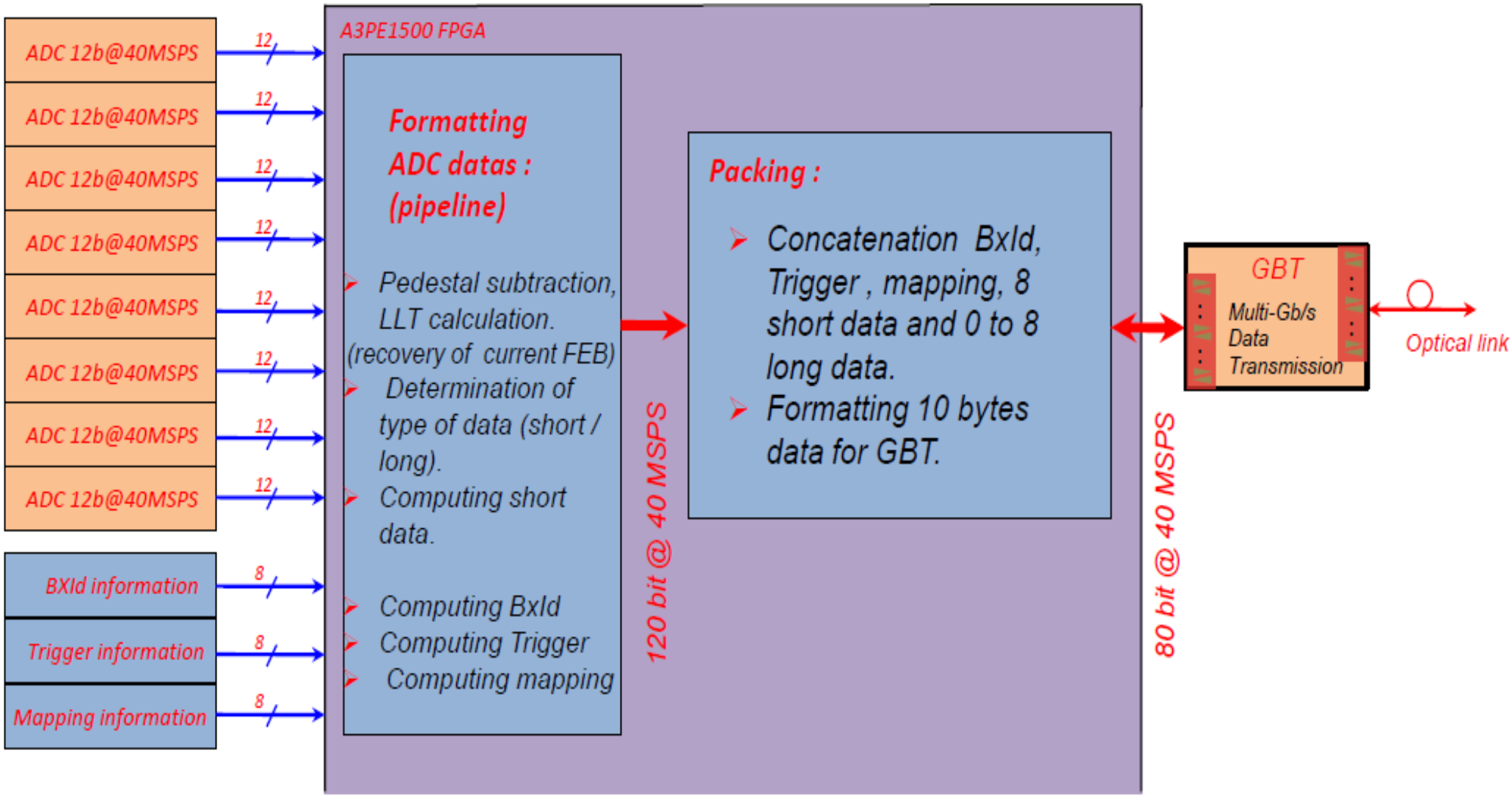
- PC write in a register (USB)
- Preprogrammed sequence of Triggers starts (sent to NIM output)
- NIM connected to a pulse generator. Analog treatment of the pulses
- After a preprogrammed latency the acquisition (RAM) starts.
- An “end acquisition” bit is flagged when the data are stored
- The PC read the bit until it is flagged and download the data through USB

- The present design of the GBT is such that we can send 80 bits @40MHz
  - Either have a lot of optical fibres (cost) or reduce the bandwith →packing
  - The optimum number of fibres is 4 → 8 channels share 80 bits
- First ideas of packing from Jacques. When realisation of the firmware had to be done, new ideas from electronics engineers
  - Thierry Caceres, Ronic Chiche and Olivier Duarte

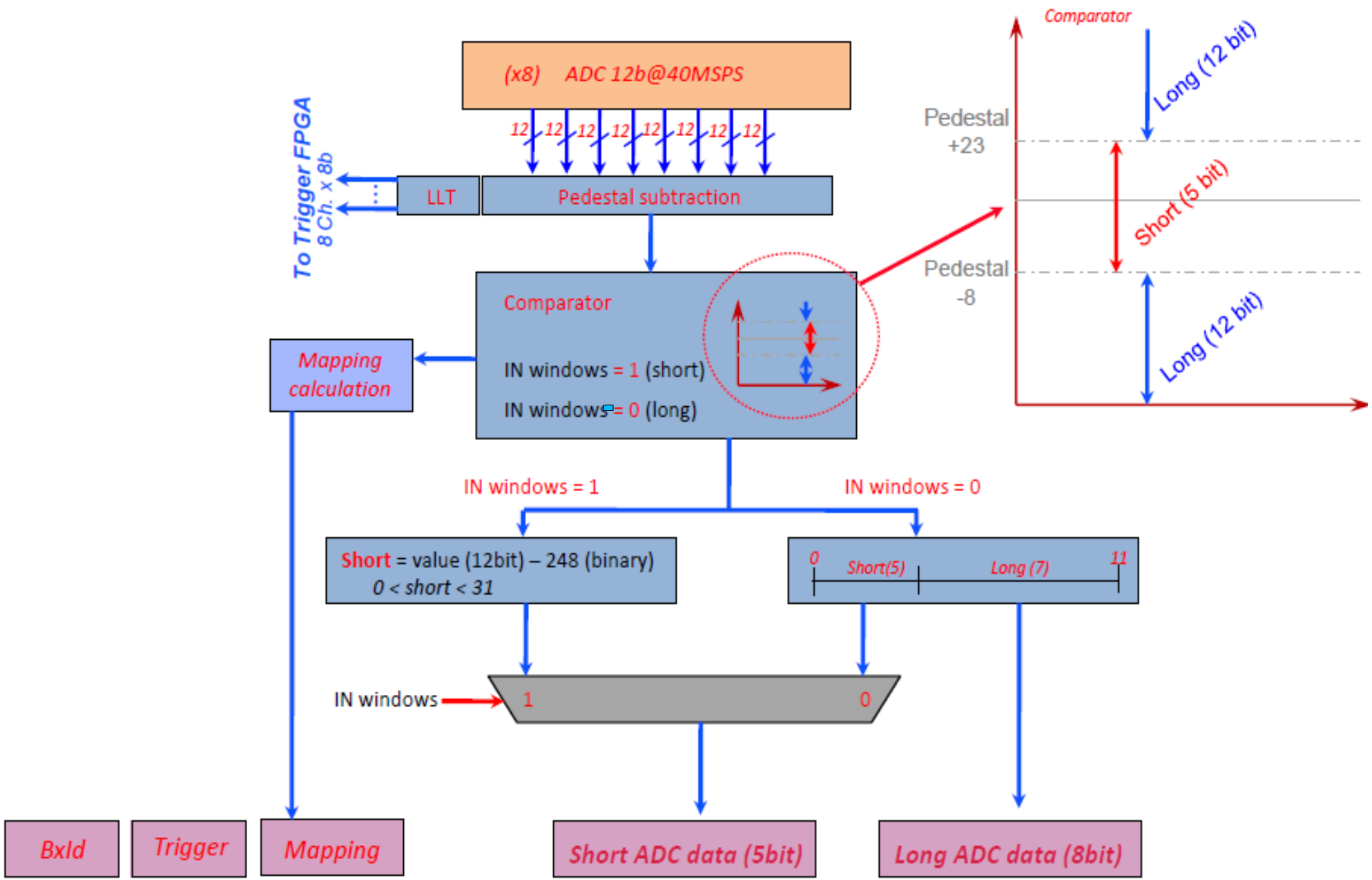


  - https://indico.cern.ch/conferenceDisplay.py?confId=117792, see Olivier's talk
- There was the question whether the GBT format could be extended to 112 bits
  - We are very interested → no packing needed anymore

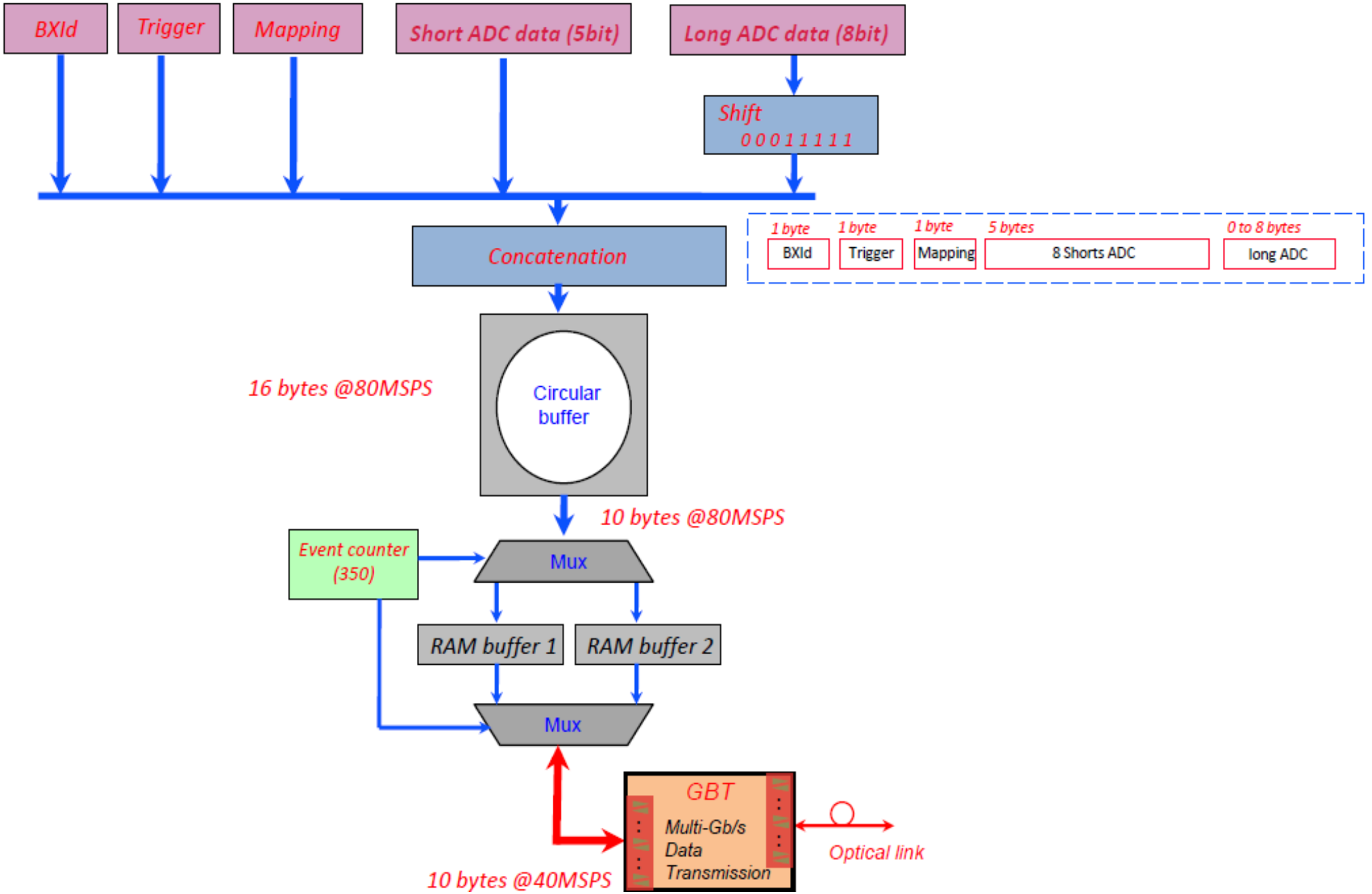
Packing (II)

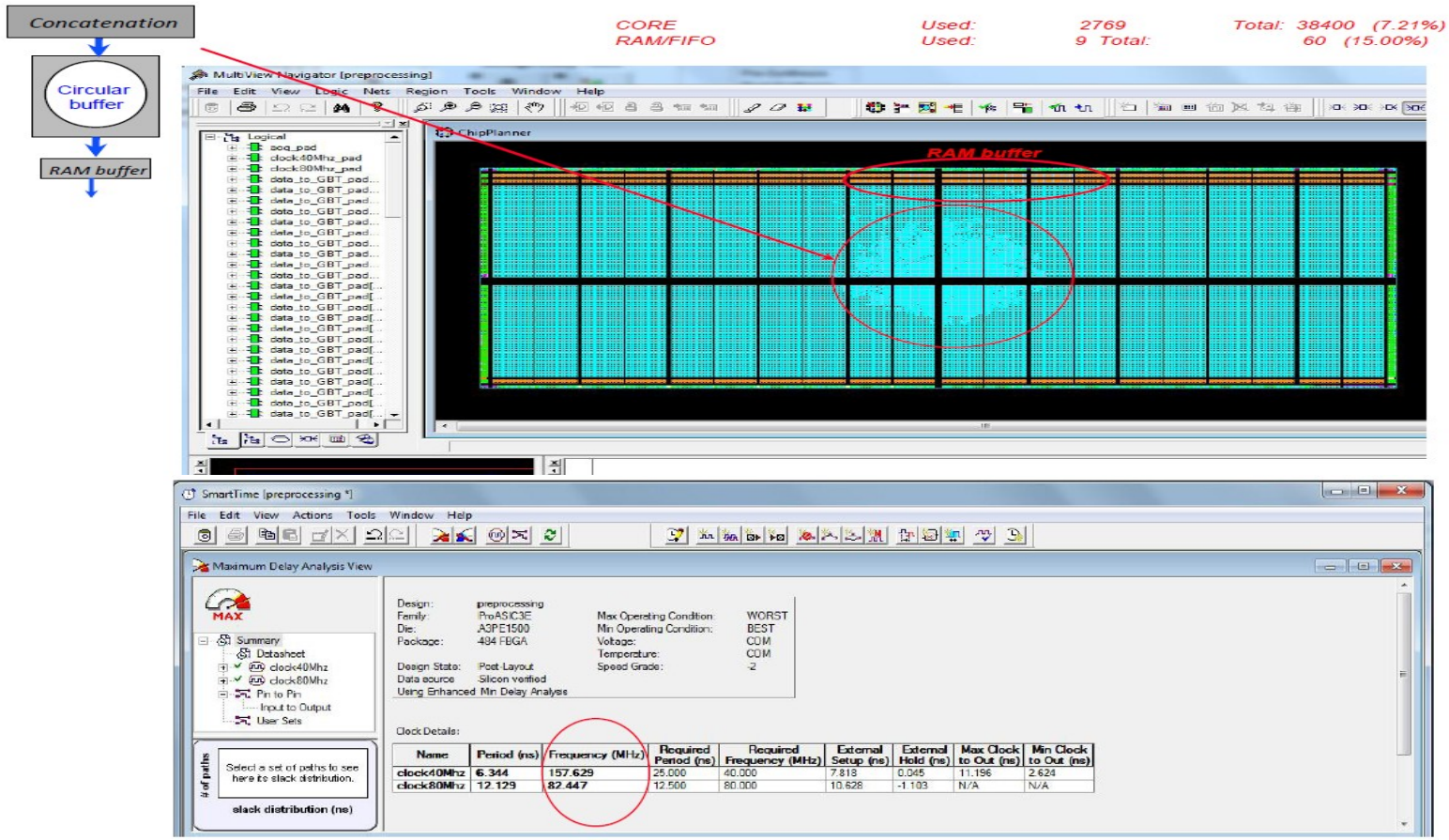


Data format (GBT input) :

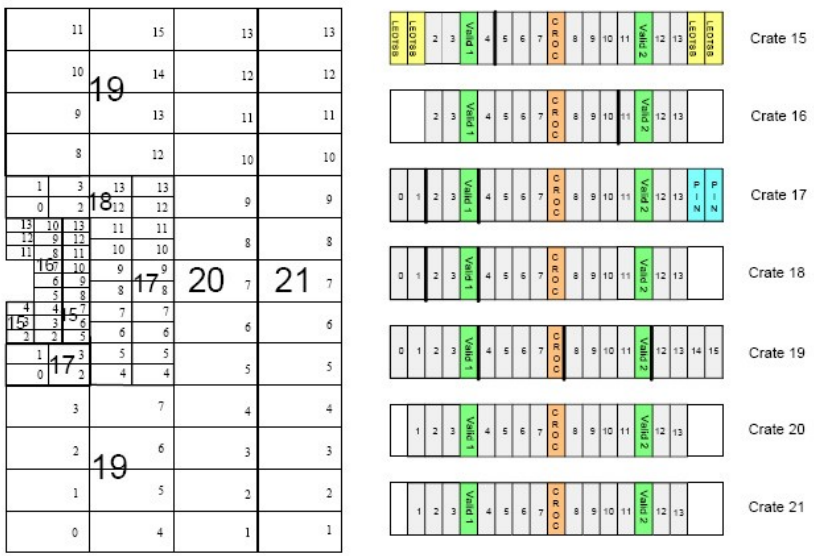

(x8) ADC 12b@40MSPS
12 12 12 12 12 12 12 12
To Trigger FPGA
8 Ch. x 8b
LLT
Pedestal subtraction
Comparator
IN windows = 1 (short)
IN windows = 0 (long)
Mapping calculation
IN windows = 1
IN windows = 0
Short = value (12bit) – 248 (binary)
0 < short < 31
0
Short(5)
Long (7)
11
IN windows
1
0
BxId
Trigger
Mapping
Short ADC data (5bit)
Long ADC data (8bit)
Comparator
Pedestal
+23
Long (12 bit)
Short (5 bit)
Pedestal
-8
Long (12 bit)

Packing (IV)


BXId
Trigger
Mapping
Short ADC data (5bit)
Long ADC data (8bit)
Shift
0 0 0 1 1 1 1 1
Concatenation
1 byte
BXId
1 byte
Trigger
1 byte
Mapping
5 bytes
8 Shorts ADC
0 to 8 bytes
long ADC
16 bytes @80MSPS
Circular buffer
10 bytes @80MSPS
Event counter (350)
Mux
RAM buffer 1
RAM buffer 2
Mux
GBT
Multi-Gb/s Data Transmission
Optical link
10 bytes @40MSPS

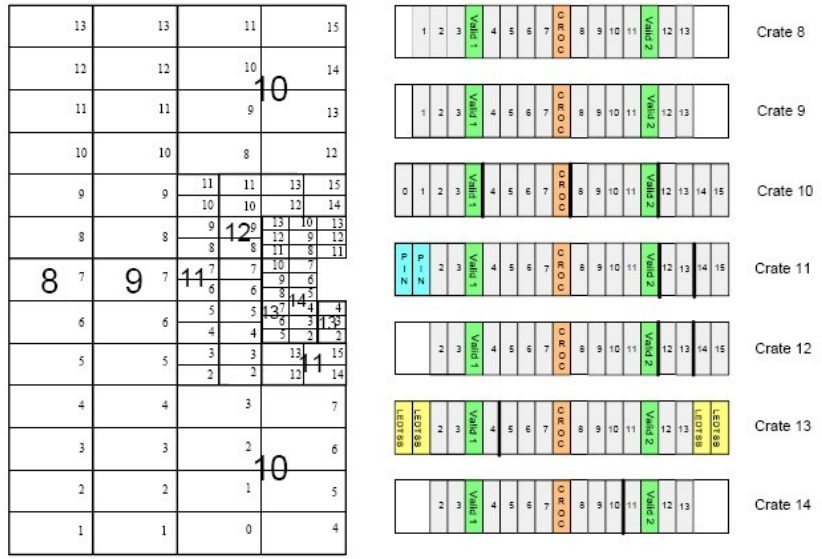


- Preliminary implementation of part of the packing into an A3PE FPGA
  - Ressources occupied are ok
  - Main problems comes from the timing
    - At present, no margin (circular buffer runs @ 80 MHz)
    - Need to understand the time analyzers and to use optimisation techniques
      - Good hope to improve significantly the time margins



last change : 20 January 2006

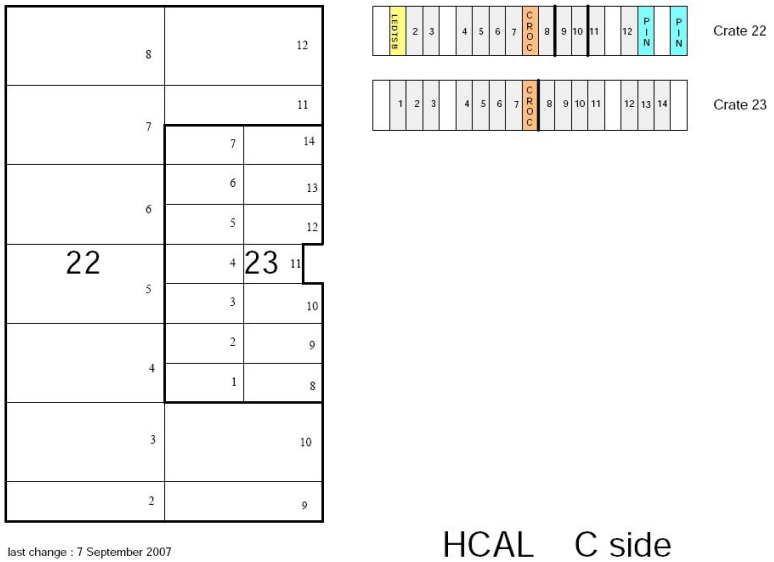
ECAL A side



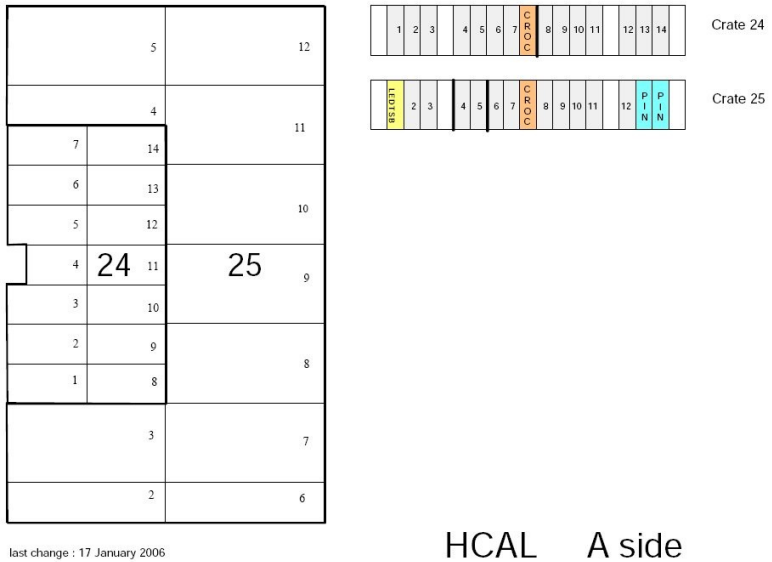
last change : 17 January 2006

ECAL C side

- 96 boards on each side
  - Includes 2 pin-diode FEB for monitoring
  - A FEB is
    - 32 channels
    - 4 optical links (GBT)

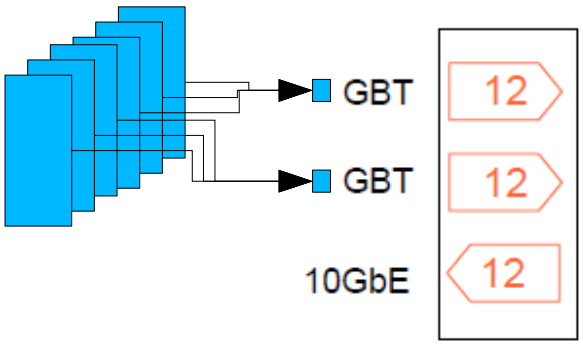


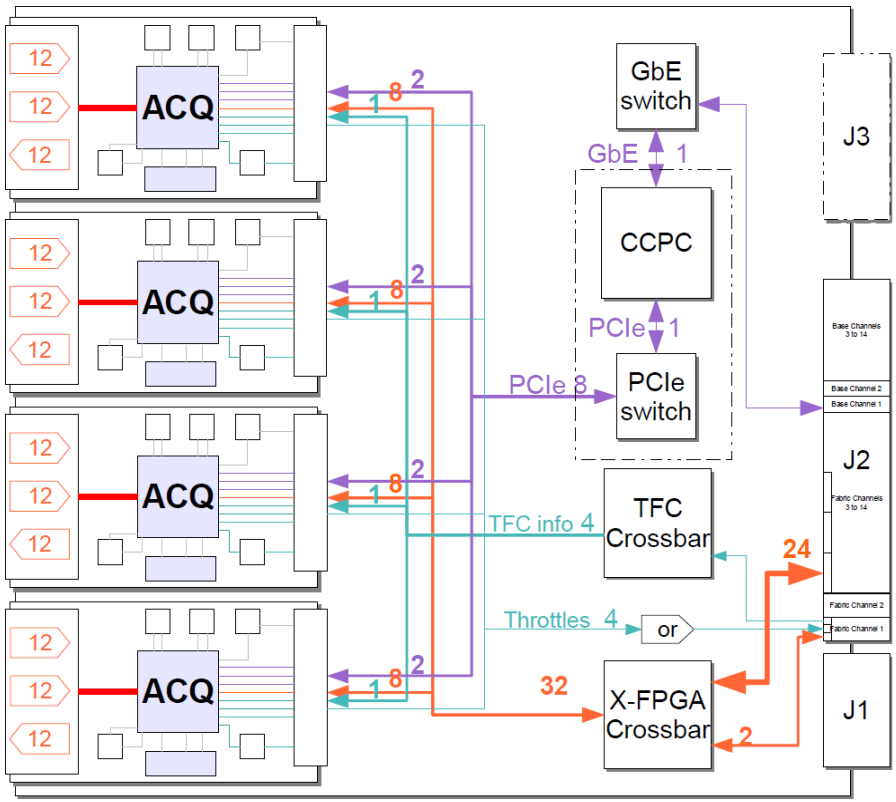
HCAL C side



HCAL A side

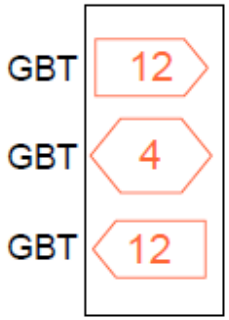
- 27 boards on each side
  - Includes 2 pin-diode FEB for monitoring
  - A FEB is
    - 32 channels
    - 4 optical links (GBT)

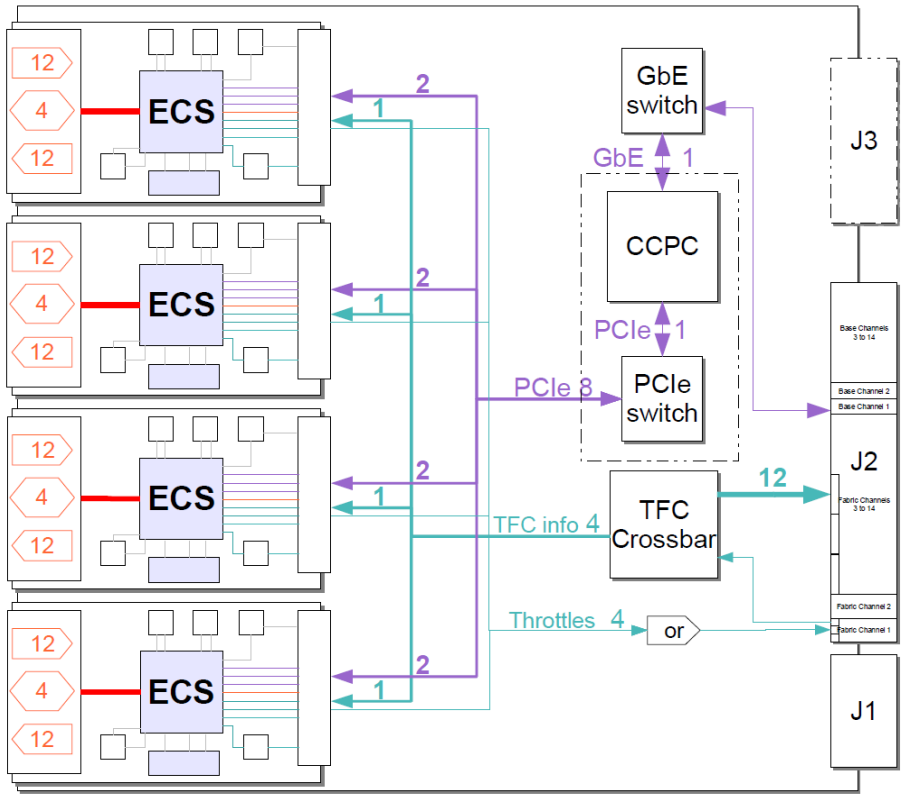




- ECAL (total of 8 ATCA – 8x4 AMC)
  - 96 FEB per side
    - 4 link per FEB
  - 4 ATCA per side
    - 4 mezzanines AMC/ATCA
    - 6 FEB per mezzanine
  - Total of 4 ATCA/side
  - Optimisation vs crate splitting
- HCAL (total of 3 ATCA – 4+2x3 AMC)
  - 27 boards per side (incl. 4 pin-diode)
  - Read full inner in 1 ATCA board
    - 2 crates for 2 sides
    - 11+11=22 FEB inner
    - 2(2) AMC for side C(A)
  - Read outer (2x14 FEB) in 2 ATCA
    - 4 Pin-diode read out with outer
    - Pin-diode side corresponds to outer ATCA side

- A new board plugged in central slot of the ECAL/HCAL crates
  - Receives
    - Clock
    - Slow control
    - Commands
  - Propagates signals to the FEB
  - ~CROC without
    - DAQ, debugging
  - (7+2)+(7+2) = 18 crates → 2 ECS mezz.
- ECAL/HCAL integrators
  - SPECS mezza → GBT mezzanines
  - 2+4 are needed → 1 ECS mezz.
    - In FEB ECS40
- ECAL/HCAL HV_DAC boards
  - GBT mezzanines
    - 32+8 → 3+1 ECS mezz.
- Calibration source
  - CAN Bus → keep it





- Front-end electronics is progressing well
  - Analog
  - Digital
  - LLT

- Still several fields not covered
  - Simulations
  - PS/SPD
  - ECS (SPECS replacement ?)
    - GBT mezzanines for the ECS
    - Modification of the firmware of the SPECS FPGA (on board FPGA)
  - GBT mezzanines for the DAQ ?
  - Control board (clock, channel B, ECS, …)

    … do not mention what will come soon (TELL40 firmware, PVSS, ...)

- Digital electronics is progressing
  - First prototype firmware includes acquisition
  - Packing is mostly coded : seems to be ok but not tested with signals !
    - Do we need it ?

- ECAL
  - 8 ATCA
    - 4 for side A (max load → 4x4 mezz.)
    - 4 for side C (max load → 4x4 mezz.)
- HCAL
  - 3 ATCA
    - 1 for inner (both sides in same ATCA, 2 mezz. per side)
    - 2 for outer (A and C splitting) and pin-diodes (also split in A and C Sides)

- ECS is 2 ATCA
    - 1 for FEB + Integrator readout (3 mezz)
    - 1 for HV control (3+1 mezz. For ECAL and HCAL respectively)
  - Is the ECS (PVSS) load acceptable for a single ECS40 ?
    - Had to split the calo ECS to have an acceptable response in current design

- 13 ATCA in total
  - Maximum number of slots in an ATCA crate is 12
  - 13 required → prefer to have an experiment dedicated ECS crate !