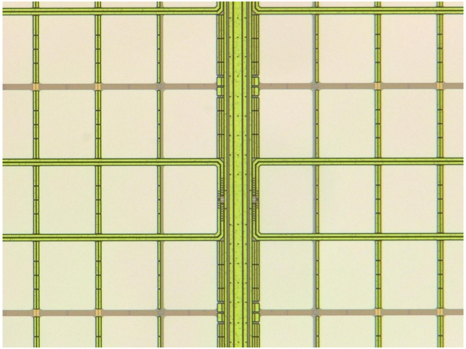
Digital SiPM Chip with High Fill Factor and Fully Integrated Serial Readout for Rare Photon Detection



6th International Workshop on New Photo-Detectors, Vancouver, 19-22.11.2024

Peter Fischer, Michael Keller, Michael Ritzert, ZITI, Heidelberg University

Overview

- Motivation
- 1st Generation Test Chip
  - Design
  - Results
- 2nd Generation Chip
  - Design
  - Results
- Next Steps

My answer to Fabrice's question raised in the introduction

'Are we going to see more DSiPM soon' ?

:

We should!

Motivation: Dark Matter Search with Liquid Scintillators

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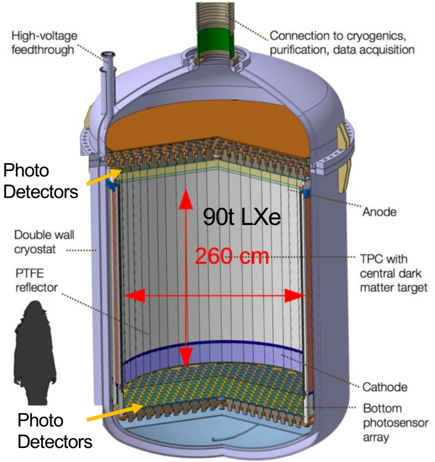
- Many physics experiments search for rare events (proton decay, dark matter, neutinos) by detecting optical photons generated in a ‘scintillator’.
- Often the scintillator is a liquified noble gas (Xenon@165K, Argon@87K) in a tank.
  Photo detectors require cold operation
  → need low power dissipation.
- Only few photons with short wavelength are created. Detectors must have a low dark count rate (DCR)
- Need to cover a large area (>10 m^2).
- Gold standard are PMTs, many groups aim for SiPMs
- We want to study the feasibility of Digital SiPMs in particular for DARWIN and XLZD



DARWIN concept

Motivation: Dark Matter Search with Liquid Scintillators

cold operation

low power dissipation

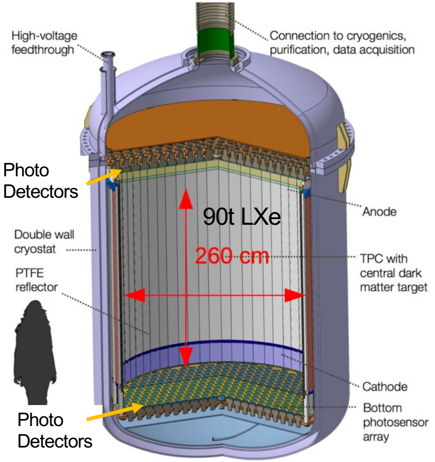
few photons

short wavelength

low dark count rate

large area

The Challenge

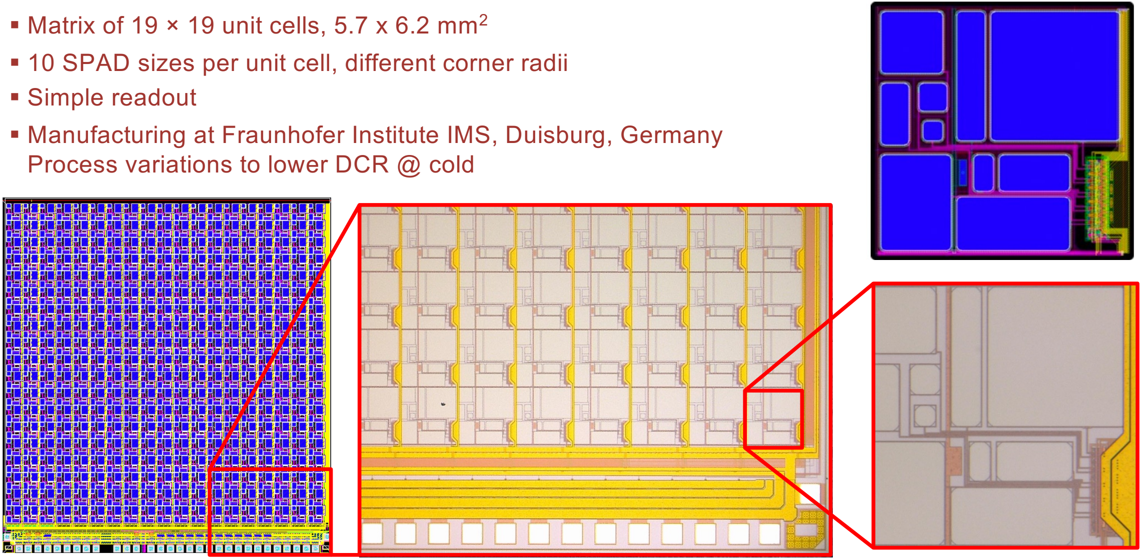


DARWIN concept

1st Generation Chip

1st Generation Chip (2020/21)

- Matrix of 19 × 19 unit cells, 5.7 x 6.2 mm^2
- 10 SPAD sizes per unit cell, different corner radii
- Simple readout
- Manufacturing at Fraunhofer Institute IMS, Duisburg, Germany
  Process variations to lower DCR @ cold



Operation down to Liquid Nitrogen Temperature

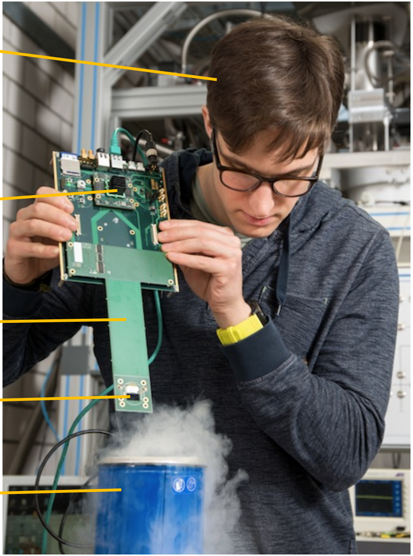
Postdoc Michael Keller

Readout FGPA

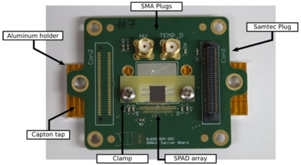
Long Arm

Chip

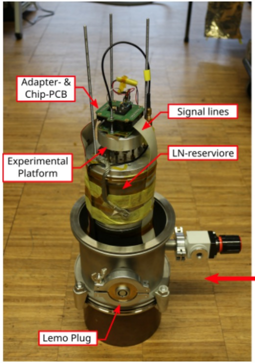
Liquid Nitrogen

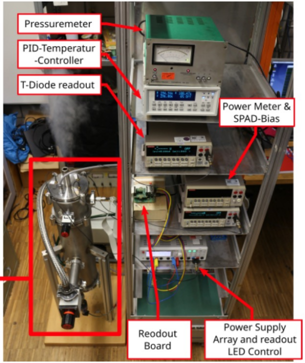


1st Setup for LN:

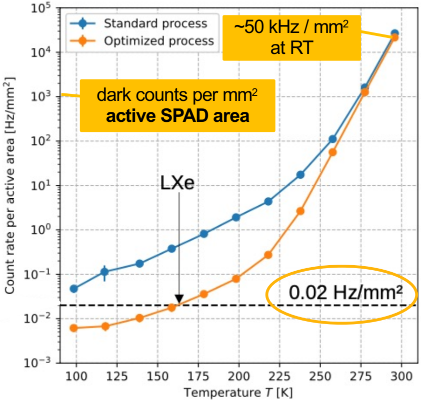


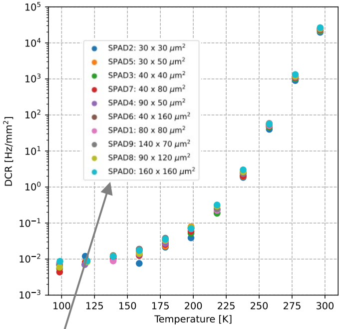
2nd Setup for continuous Temperatures:

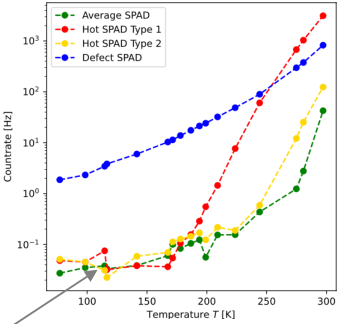




Dark Count Rate vs. Temperature



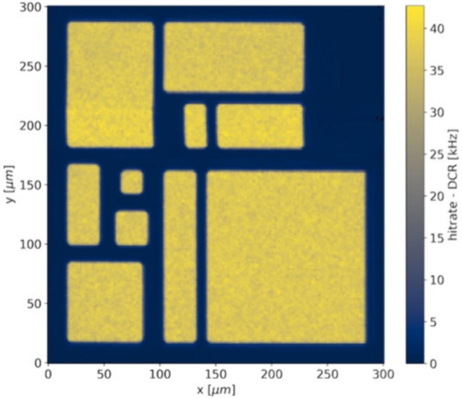


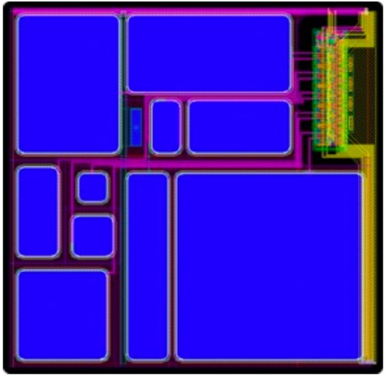


- Reduced tunneling noise @ cold by technology variation @ IMS: **~ 0.02 Hz / mm² @ LXe**
- No dependency of DCR from SPAD shape or corner radii – just area!
- Many SPADs that are ‘hot’ at RT become good @ cold!

Spatial Sensitivity

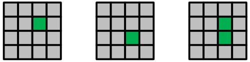
- Scan over active area with ~1µm laser spot
- **Very homogeneous**
- Measured sensitive area matches design value very well



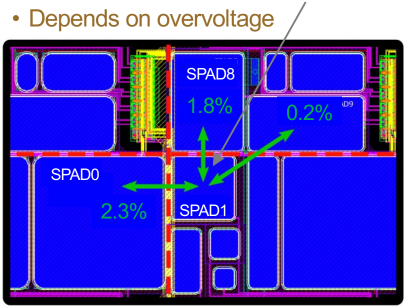


Crosstalk

- We read every pixel → Can identify crosstalk events as adjacent hits

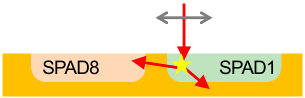


- Measure ~2% for a (70µm wide) SPAD
  - Depends on overvoltage

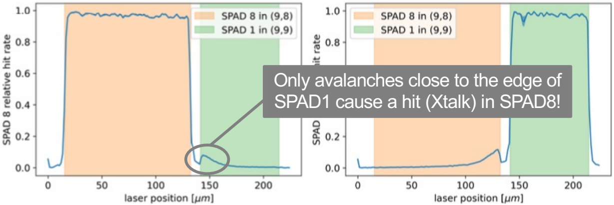


PhD Michael Keller

- More insight: Force a SPAD avalanche by light injection at known position



- Crosstalk occurs if avalanche is at SPAD edge:



Hits **in left SPAD8** vs. position   Hits **in right SPAD1** vs. position

- Crosstalk 0→1 (3%) is larger than 1→0 (2%)

MSc Robert Zimmermann

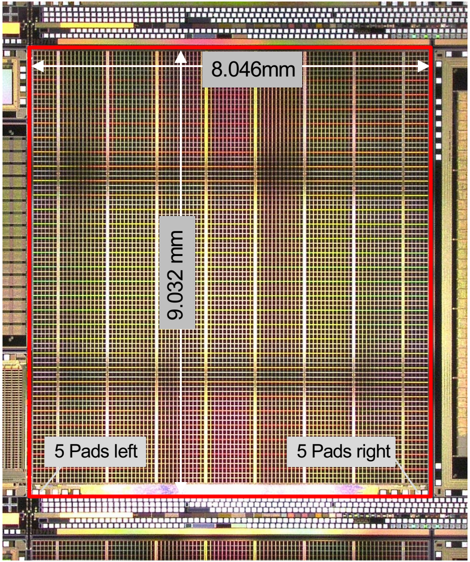
2^{nd} Generation Chip

2nd Generation Chip (2023/24)

- Chip size: ~8 × 9 mm^2
- 32 × 30 pixels with 8640 SPADs
- SPAD Fill factor ~72%
  (including periphery, before pixel masking)

- Noisy SPADs can be switched off

- Only 4 logical signals:
  - Clk / Command / SerIn, SerOut
- 3 supplies (Pads duplicated)
  - GND, VDD, HV



Choice of SPAD / Pixel Size

- High spatial resolution not required.
- Could use **large SPADs** for **good fill factor**
- But: Noisy SPADs are **switched off** → significant **area loss** for large SPADs
- If defect density is known (@ cold!) → **optimal** SPAD size for maximal fill factor **after** masking!

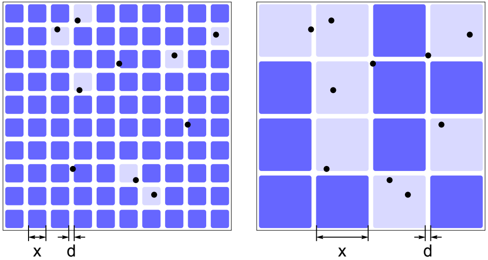
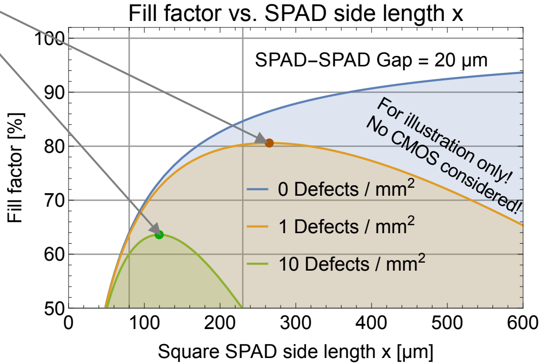
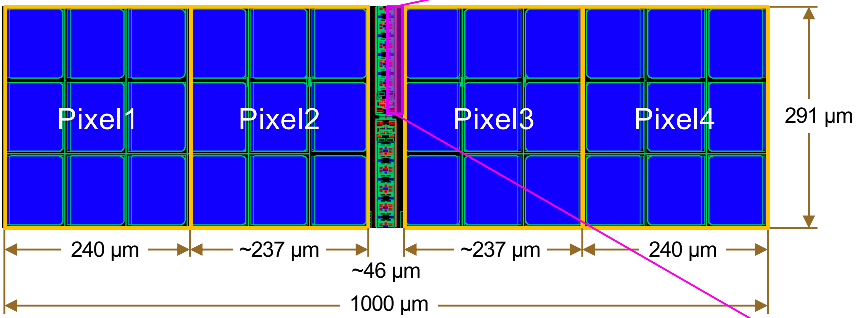


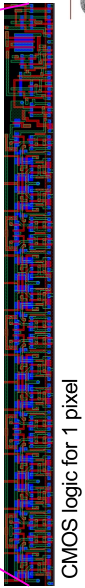
Illustration of area loss by point defects for small/large SPADs



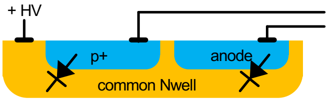
Pixel Geometry

- Decided to groups 9 SPADs to one '*pixel*' to save CMOS circuitry
- 4 pixels form one unit, with common circuit in the center



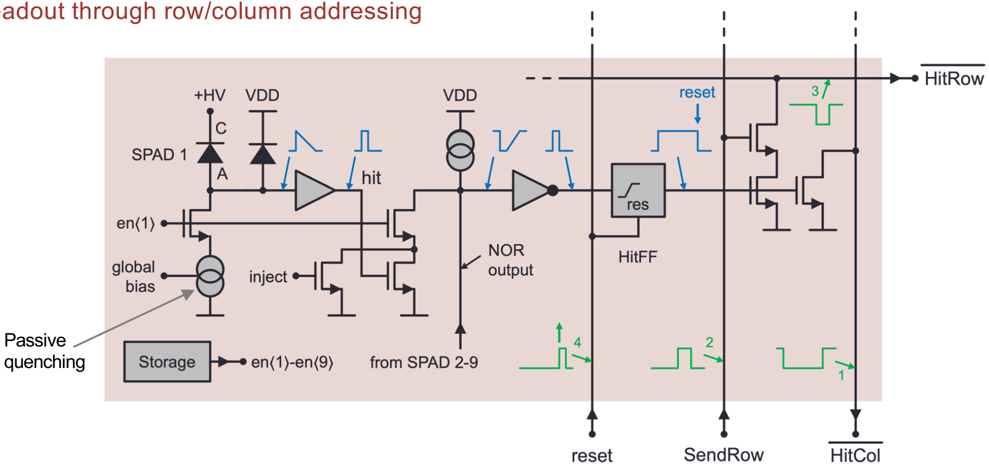


- SPADs share one NWELL
- Can be switched off by changing anode voltage



Pixel Architecture

- 9 SPADs per pixel, each SPAD can be disabled
- Hits of 9 SPADs are OR-ed and set a flipflop (which must be readout, i.e. hits cannot get lost)
- Readout through row/column addressing



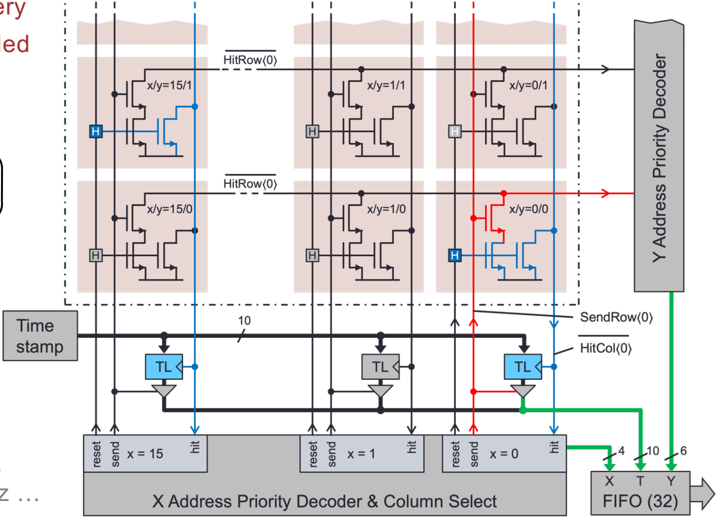
Matrix Readout

- Hit in a column is flagged to periphery
- A **timestamp** per columns is recorded
  - Timestamps for further hits are wrong

- Global scanner selects a column
- Hit rows (→ x/y) are determined
- Hit FFs in the column are cleared

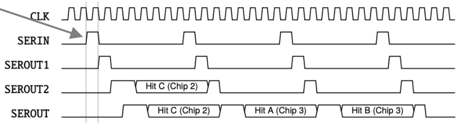
- Hits are stored in a FIFO, waiting there for readout (32 words)

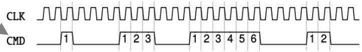
- Transferring one hit from matrix to FIFO takes 7 clock cycles.
  → Can transfer 7 Mhits/s @ 50 MHz …

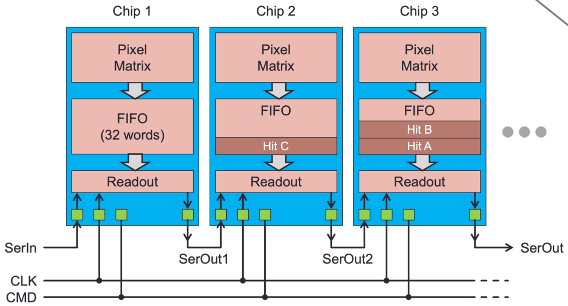


Hit Readout to DAQ

- Chips are daisy chained (Serin / SerOut / Clk)
  - 'Data packets' in the stream are defined by injecting '1' pulse to first chip
- Chip operation is controlled by a global CMD signal
  - Commands are pulse-width encoded
  - Chips are addressed with address/data packets through SerIn
  - Chip addresses and configuration are programmed this way



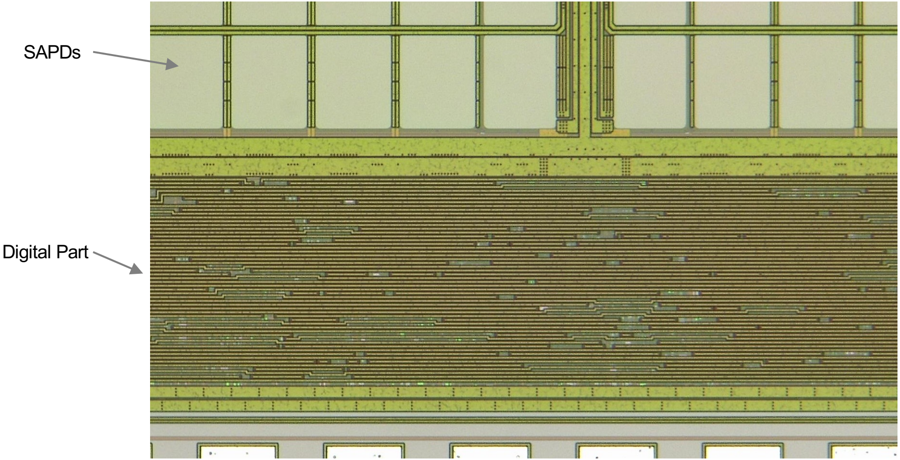




CMD width	Name	Action
1	ResetAll	Reset State machines, FIFO, time counter and hits
2	ResetTime	Reset only time counter
3	ResetMatrix	Reset only hits in matrix
4	ReadoutSimple	Start readout of only one hit
5	StartReadout	Start continuous hit readout
6	StopReadout	Stop continuous hit readout
7	WriteConfig	Write configuration register
8	ReadConfig	Read configuration register
9	WriteID	Write chip IDs
10	InjectMatrix	Inject hits into the matrix, depending on the programmed enable pattern
11	InjectFIFO	Inject test data pattern to FIFO
12	InjectSerializer	Inject test data pattern to serializer (behind FIFO)

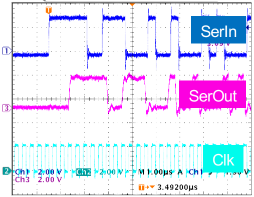
(Digital Layout)

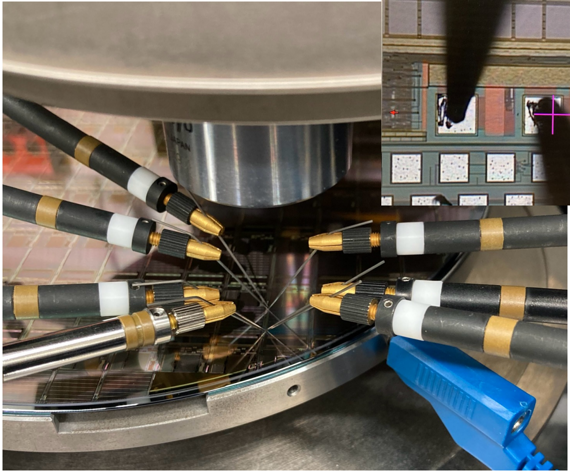
- A 'simple' logic is required to keep the global digital part small
- Limiting factor are routing resources (350 nm technology, 4 metal layers)

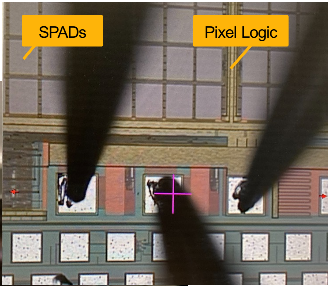


First Chip Tests

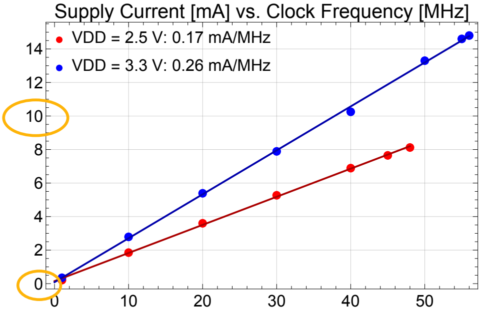
- Chips (wafers) back since 1 week!
- No diced chips yet → test on wafer prober
  - Need only 7 needles (4 signal + 3 power)
  - Bad signal integrity…
- All digital tests work!
  - SerIn / SerOut
  - Write Chip ID
  - FIFO test
  - Select pixels
  - Inject
  - Read data
  - …
  - 😀

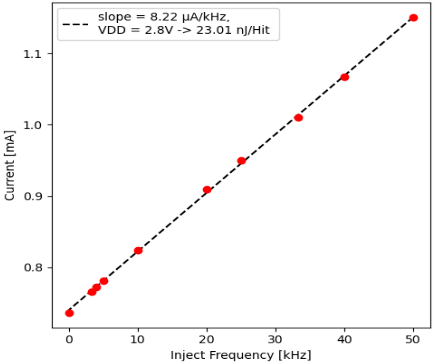






- Pixel / matrix design is fully static, has no clock.



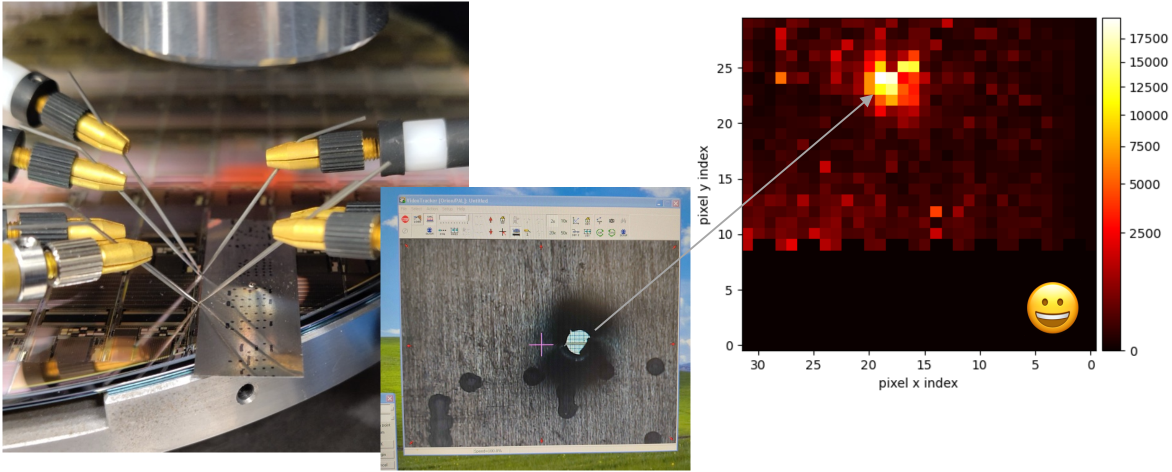


- **Permanent supply current** from digital periphery / readout part:
  - proportional to clock frequency
  - Consume ~10 mA @ 50 MHz @ 3V
  - 'nothing' if clock is off…

\+ **Hit dependent energy** for each processed hit:
  - Measured by injecting hits at varying rate and reading them out
  - For expected hit rates @cold → negligible

SPAD Hits – A *very* first test

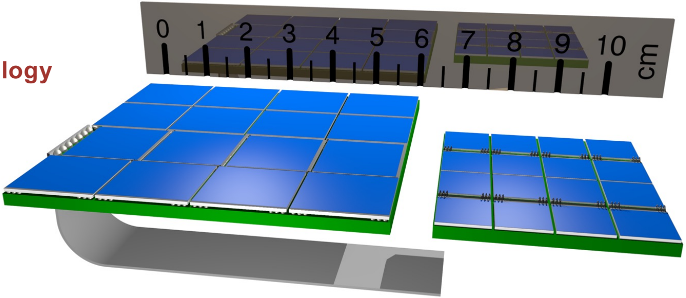
- ‘Cover’ chip with metal mask with a hole
- Too much stray light on needle side → must mask off bottom part

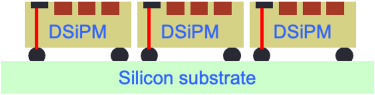


Next Steps

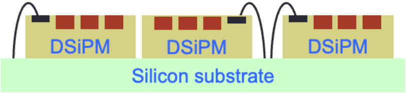
- Will operate chip in **LXe test** setup at Freiburg University (within DARWIN)
- Will develop **next chip** for **3D technology**
- Will develop **multi-chip modules.** Silicon substrate (1 routing layer) for
  - perfect CTE matching and
  - high radio-purity.

  - Version 1 will use wire bonds
  - Advanced version 2 will use TSVs under IO pads and bump bonding





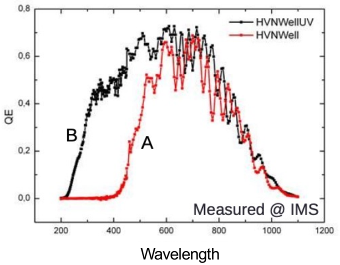
Version 2: Chip backside contacts (after postprocessing of wafers)



Version 1 : Wire bonds

Some Chip Parameters

- Chip size: ~ 8 × 9 mm^2 — limited by space available in run. Could be 20 × 20 mm^2
- Pixel size: ~ 240 × 290 μm^2 — 9 SPADs per pixel
- Pixels: 32 × 30
- DCR: ~ 0.02 Hz / mm^2 @ 165 K
- QE: ~ 50% (500..800 nm) — process ‘B’ not available in run
- SPAD Xtalk: ~ 3% (extrapolated)
- Power: ~ 40mW / cm^2 — @50 MHz, proportional



- Disable: each SPAD
- Readout: each hit
- Clock: ~ 50 MHz
- Time stamp res.: 10 ns — @50 MHz, double edge clocking. SPADs are much better!
- Clocks / Hit: 28 bit — bits in serial data word (10 bit time stamp, 6 bit chip ID)
- Max. link rate: 1.8 Mhits / s — @50 MHz
- Chips / Chain: ≤ 64 — with present 6 bit chip ID

Summary

- DSiPMs can have excellent DCR and high fill factor!

- Advantages of DSiPM are:
  - Application-specific readout architectures
  - High spatial and time resolution
  - Very simple system (detection and readout on one piece of silicon)
  - Low Power dissipation (no amplifiers!) – (but depending on time stamp resolution, readout speed…)
  - Low intrinsic radioactivity,….

- Open issues:
  - UV sensitivity (→ use 'PureB' process) or use WLS
  - Emission of photons from circuitry. Is that an issue in our data-driven design?
  - Radiation hardness ? (No issue for DARWIN)
  - …
  - Availability of more vendors with very good quality SPADs

Thank you for your attention!

… sorry that I could not come in person …

Contact: peter.fischer@ziti.uni-heidelberg.de