Ultra-Low Resource Time-to-Digital Converter for PET TOF Systems Achieving Sub-10 ps Resolution Using LUT-Based Counter on FPGA

Daehee Lee[1], Ian Hwang[2], Sun Il Kwon[1]

1. *Department of Biomedical Engineering, UC Davis, California, USA*
2. *Baskin School of Engineering, UC Santa Cruz, California, USA*

November 21, 2024

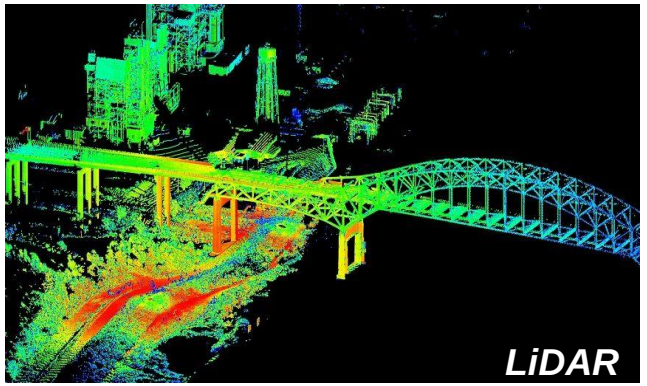
1. Time-to-Digital Converter

Time-to-Digital Converters (TDCs)

are electronic circuits that digitize continuous time values into discrete digital values.

Medical Field

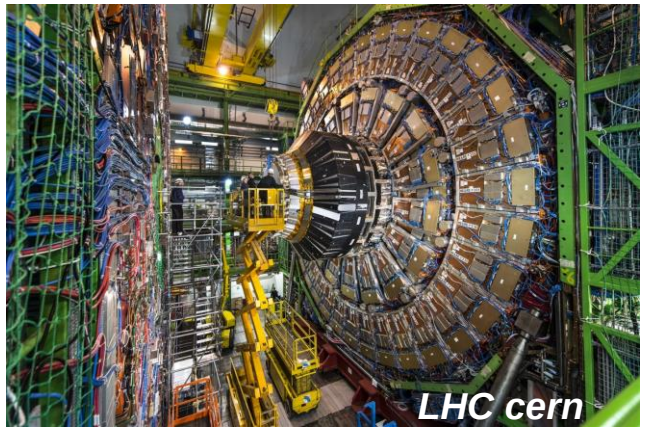
Total-body TOF PET, uExplorer



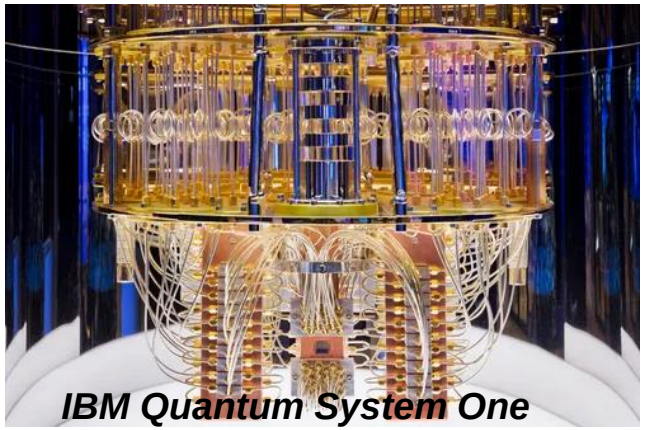
LiDAR

Industry

Physics



LHC cern



IBM Quantum System One

Computing

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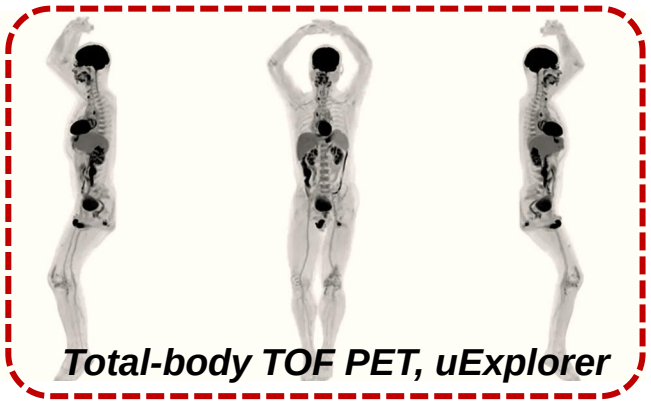
TDC applications

Medical Field



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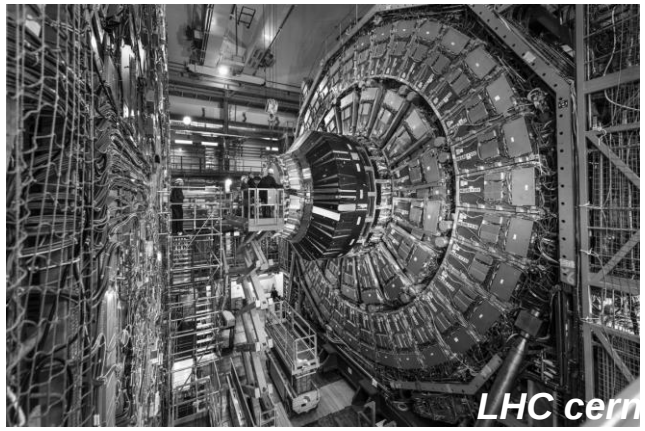
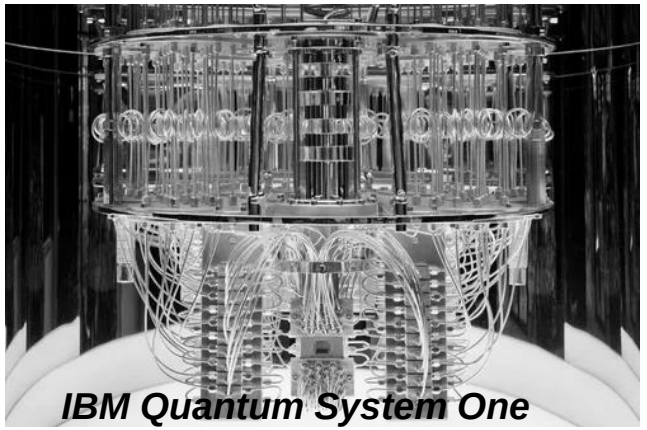


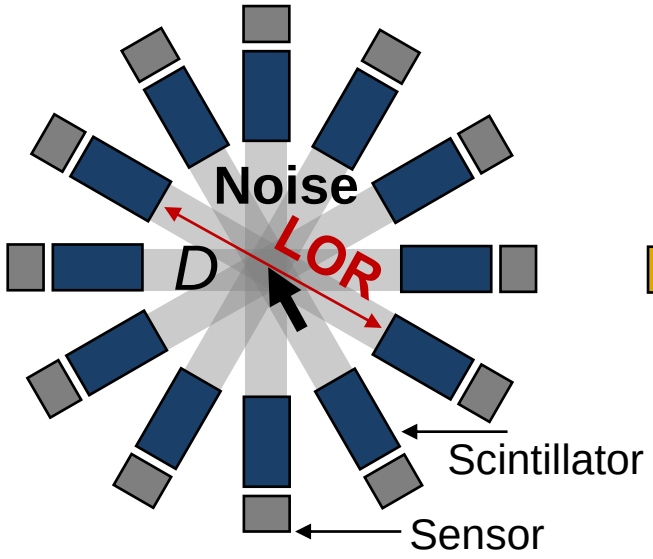


Computing

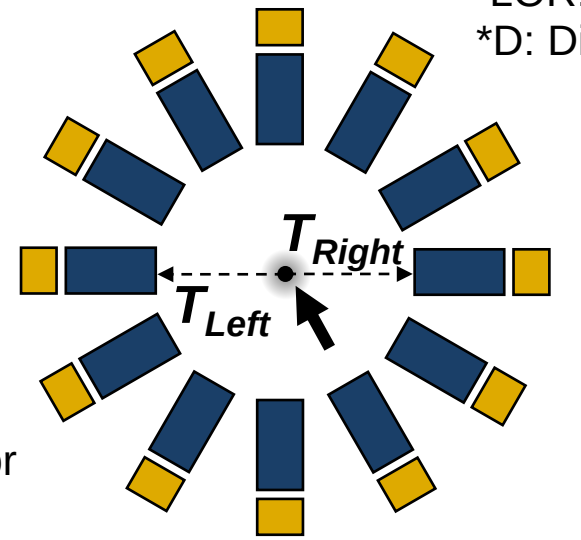
1. Time-to-Digital Converter

Time-of-flight Positron Emission Tomography

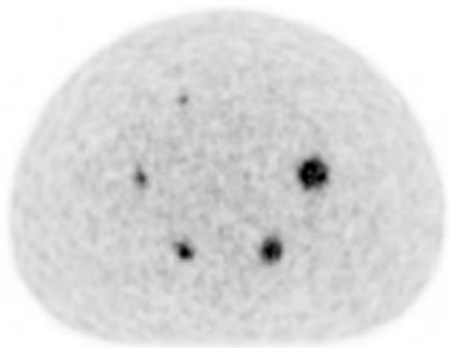
NON-TOF PET

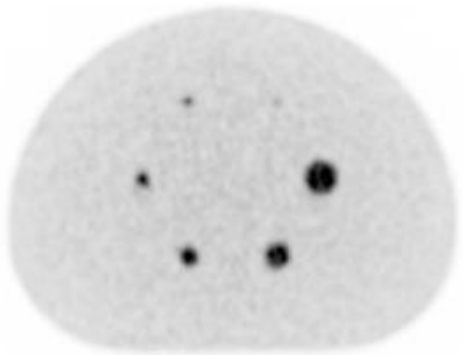


TOF PET



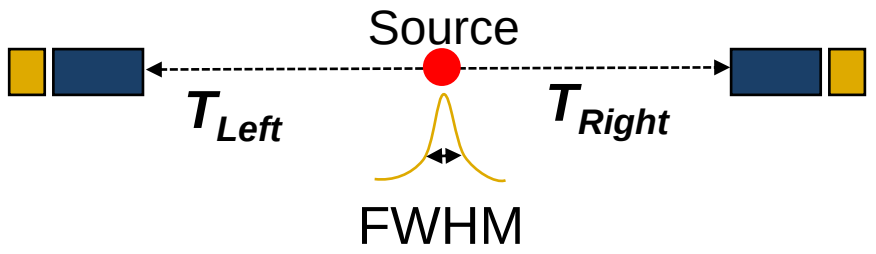
*LOR: Line of Response
*D: Diameter





Siemens Biograph mCT (PET/CT), 2019

Coincidence Time Resolution (*CTR*)

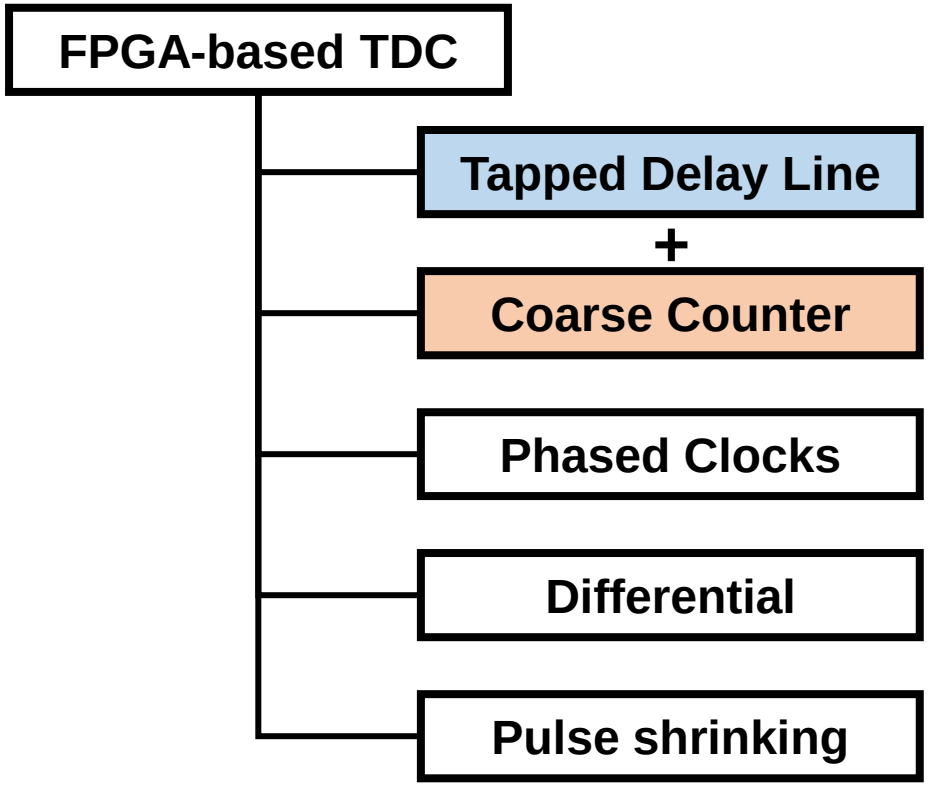


$$\Delta x = \frac{c \times CTR}{2}$$

1. Time-to-Digital Converter

Application-specific Integrated Circuit **(ASIC)** vs. Field-programmable Gate Array **(FPGA)**

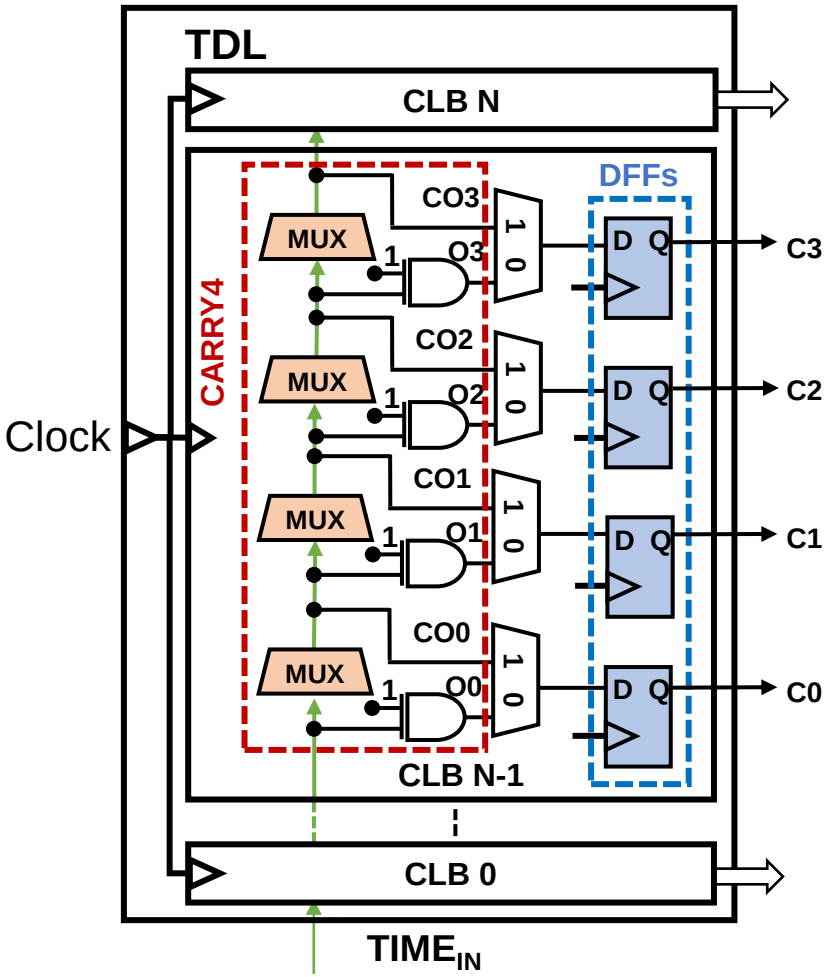
Feature	ASIC	FPGA
Purpose	Fixed function	**Reconfigurable**
Performance	High	Moderate
Power	Low	High
Flexibility	Low	**High**
Development cost	High	Low
Unit cost	Low	High
Time to market	Long	**Short**
Logic density	High	Moderate



Rui Machado et al., (2019)

1. Time-to-Digital Converter

Tapped Delay Line (TDL) with **CARRY4**



A CLB is crucial for fast signal propagation and TDL implementation.

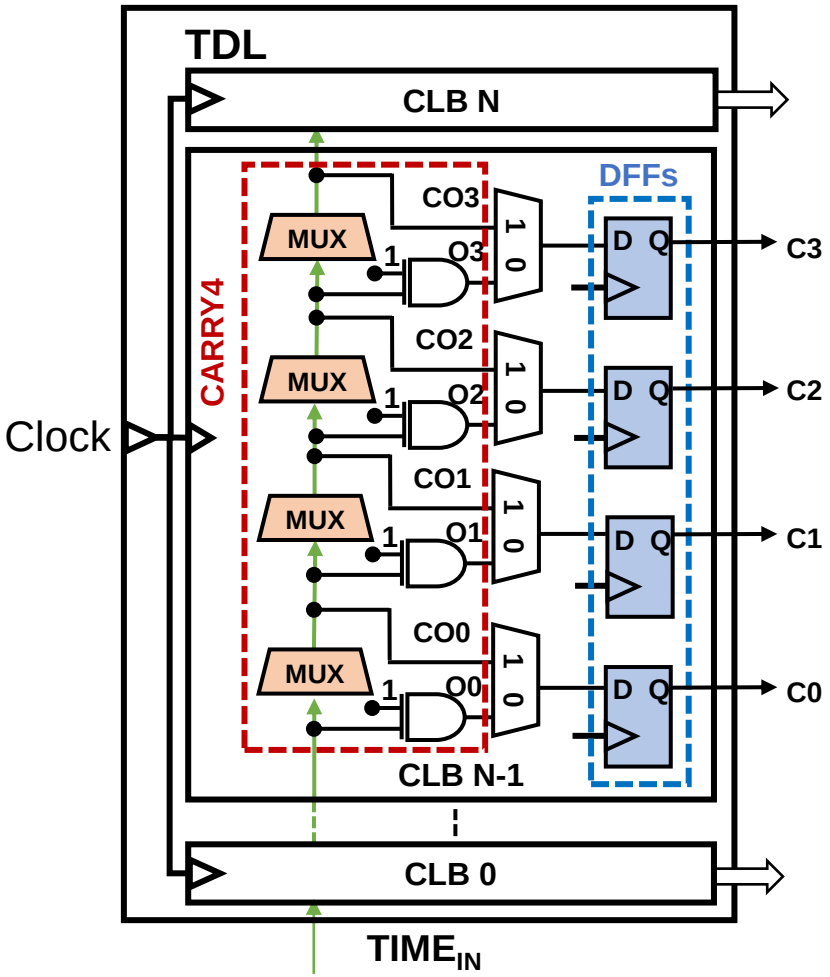
Thermometer codes

C0 - C1 - C2 - C3 - C4 …

1 - 0 - 0 - 0 - 0 …

1. Time-to-Digital Converter

Tapped Delay Line (TDL) with **CARRY4**



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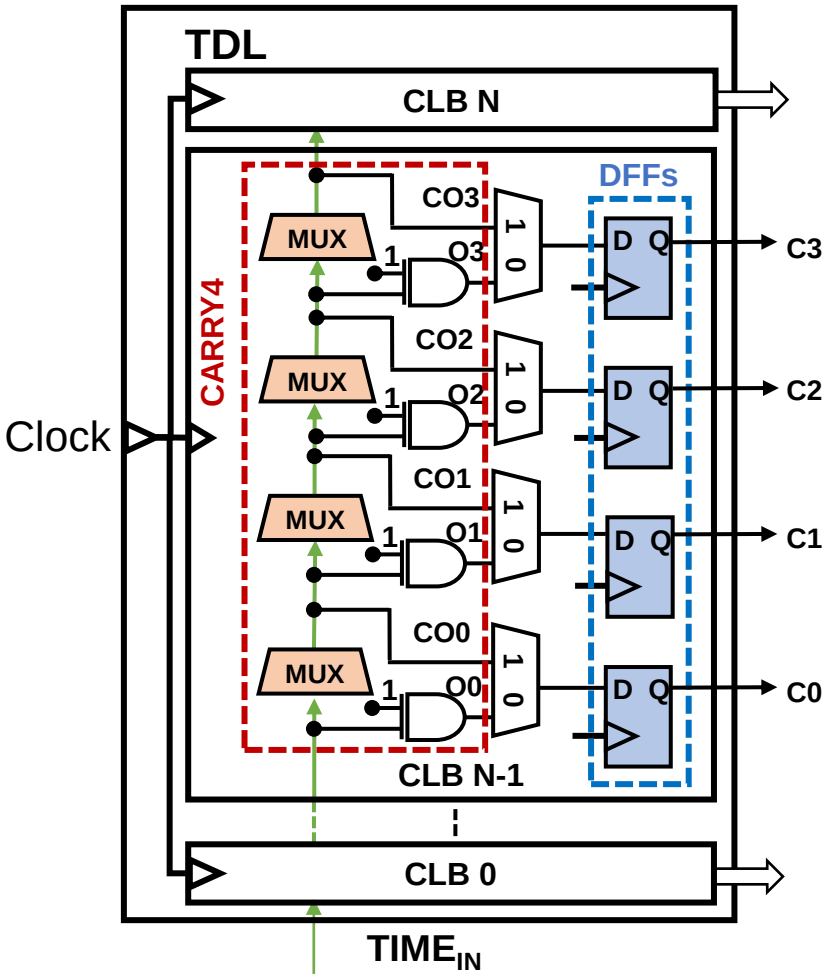

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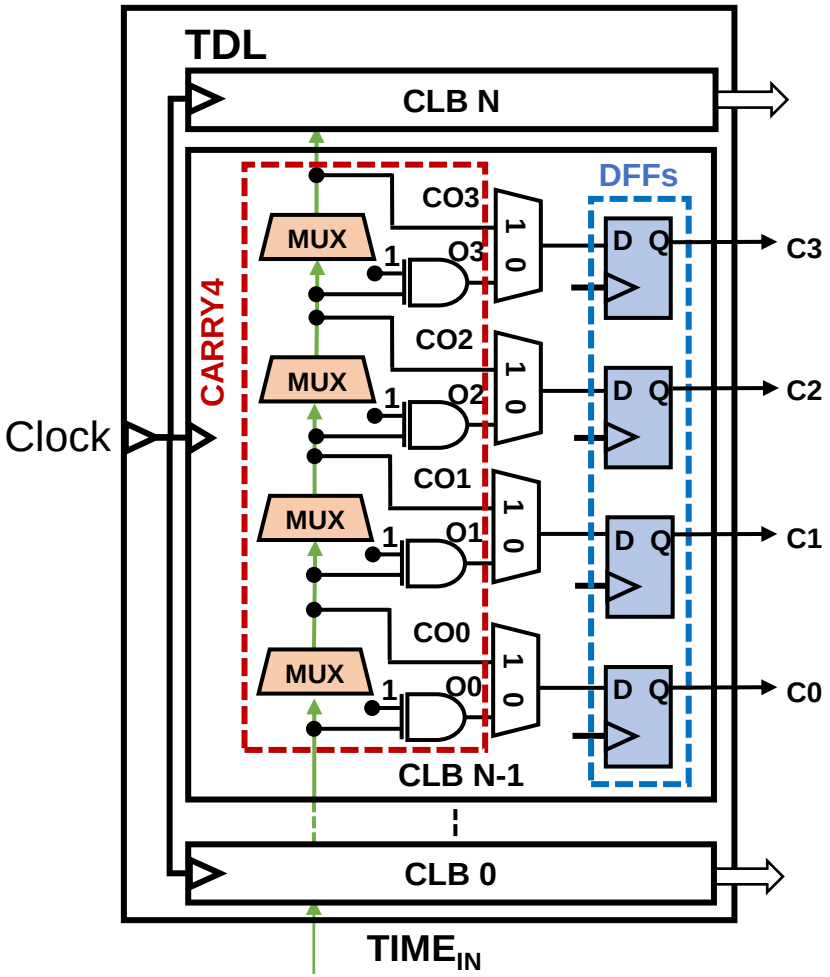

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C0	C1	C2	C3	C4	…
1	0	0	0	0	…
1	1	0	0	0	…
1	1	1	0	0	…
1	1	1	1	0	…
1	1	1	1	1	…

Average timing resolution with CARRY4 is **~10 ps** (Virtex-7 series, Xilinx).

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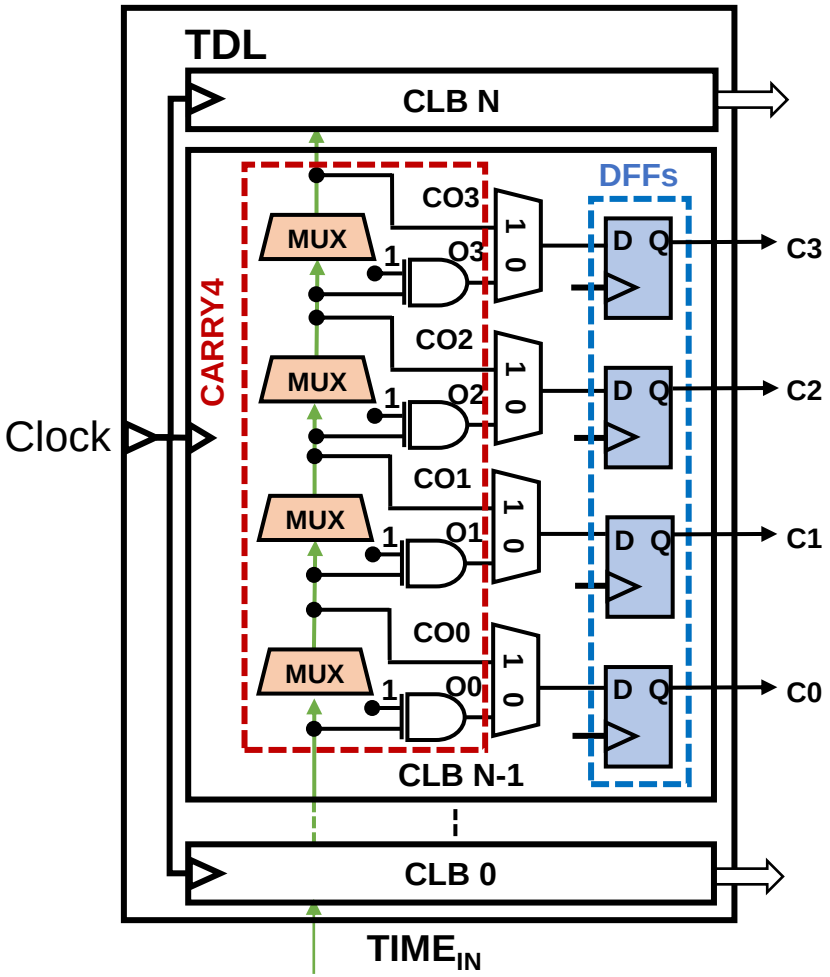


A CLB is crucial for fast signal propagation and TDL implementation.

Thermometer codes

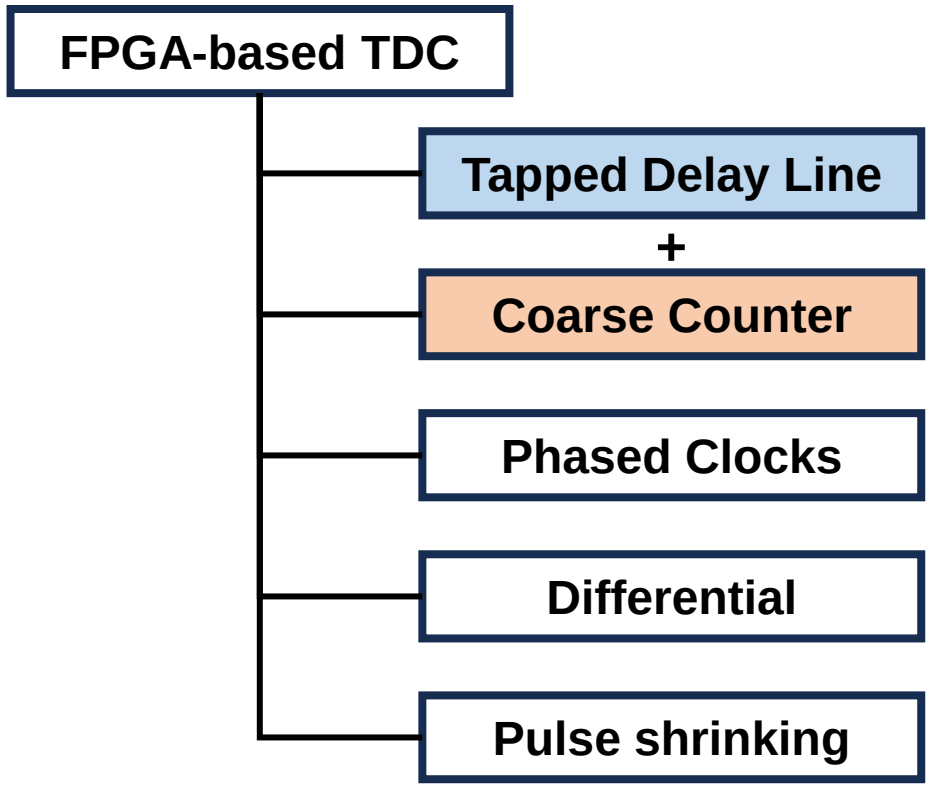
C0	C1	C2	C3	C4 …
1	0	0	0	0 …
1	1	0	0	0 …
1	1	1	0	0 …
1	1	1	1	0 …
1	1	1	1	1 …

Average timing resolution with CARRY4 is **~10 ps** (Virtex-7 series, Xilinx).

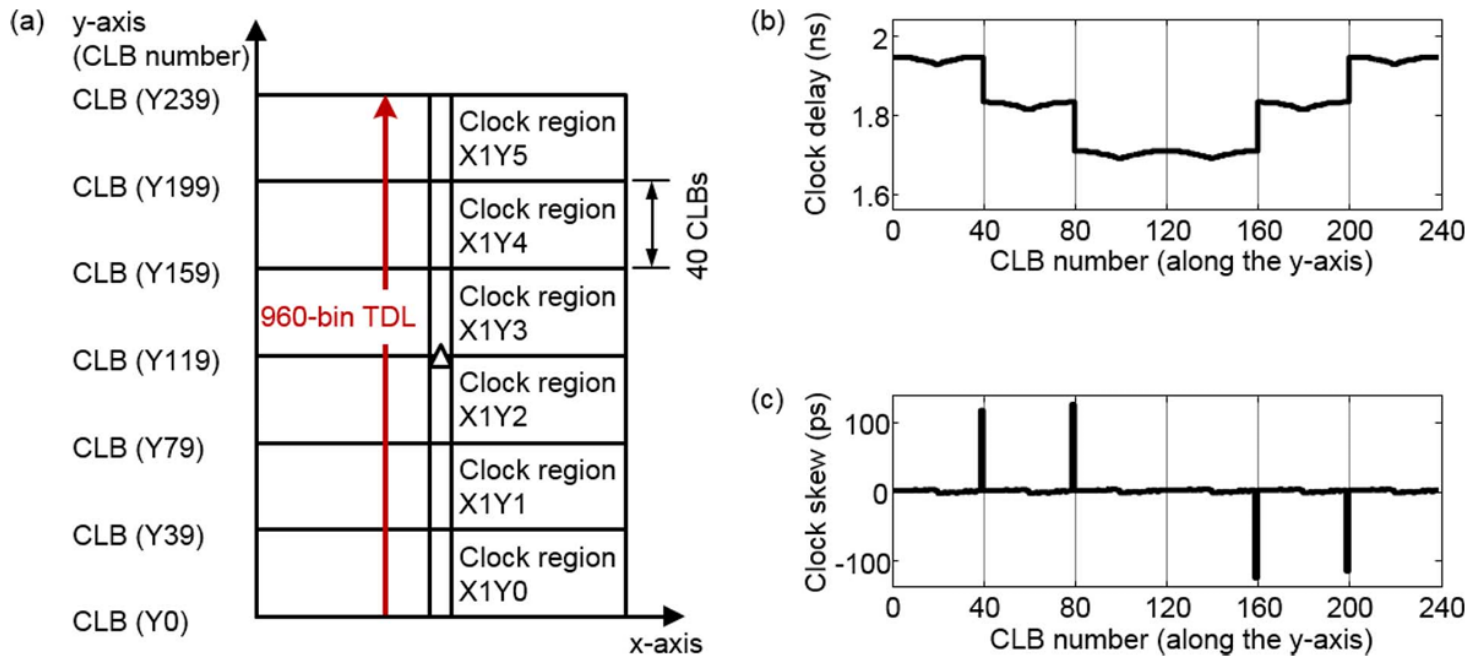
Average timing resolution with CARRY8 is **~5 ps** (Ultrascale series, Xilinx).

1. Time-to-Digital Converter

Tapped Delay Line (TDL) with **CARRY4**



Jun Yeon Won *et al,* 2016



Ultra bins are unavoidable due to clock region changes.

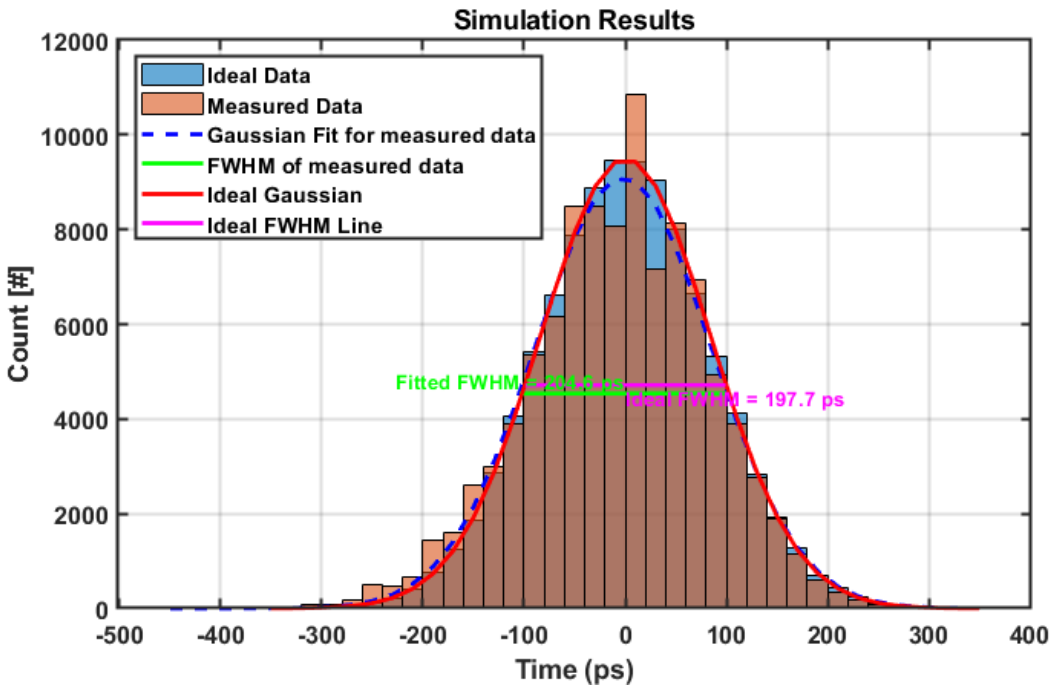
FPGA resources are limited.

➔ The smaller the resource usage, the more TDC implementations can be accommodated.

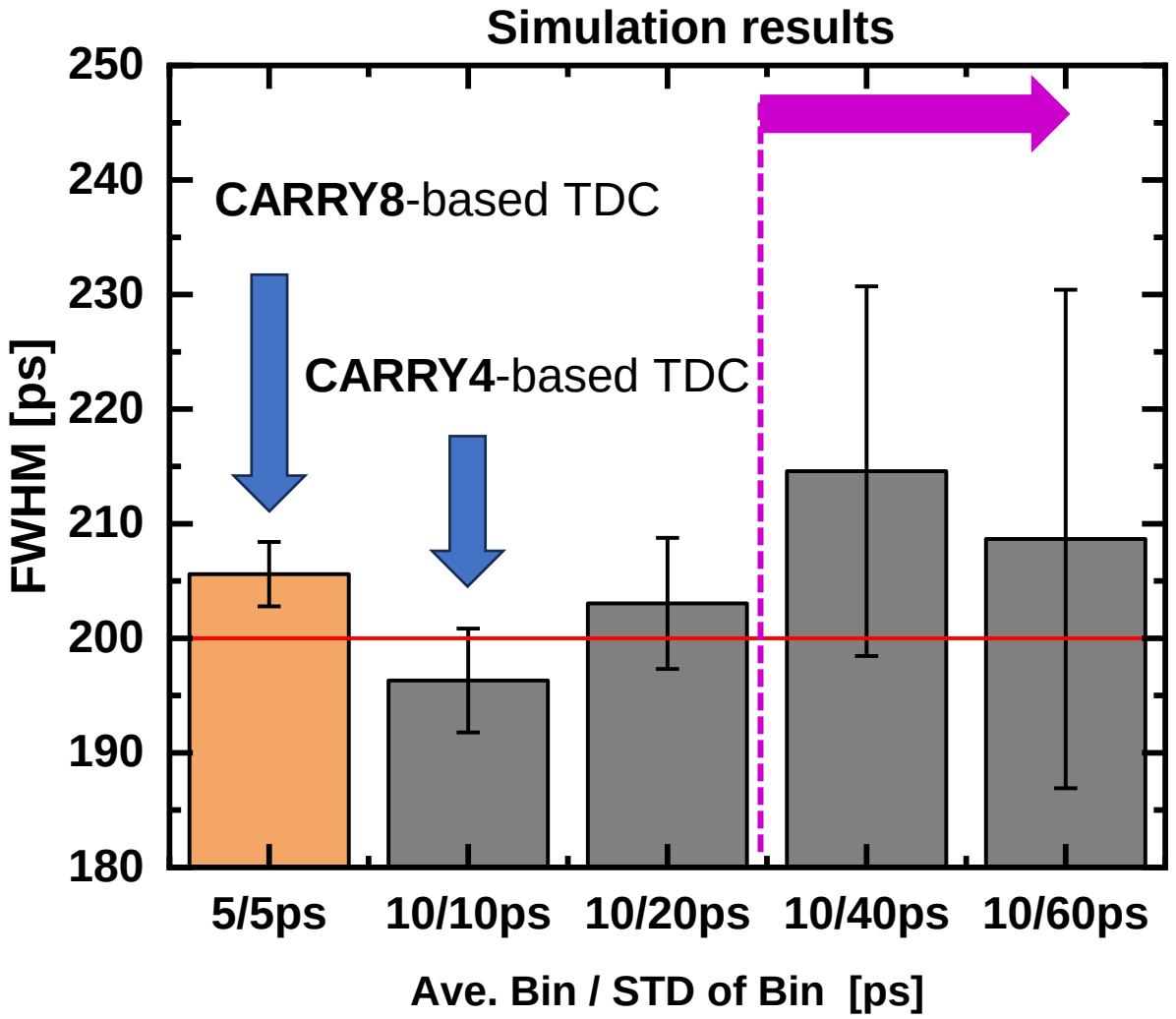
1. Time-to-Digital Converter

Tapped Delay Line (TDL) with **CARRY4**

Simulation
Average bin size **5** ps
Std **5** ps

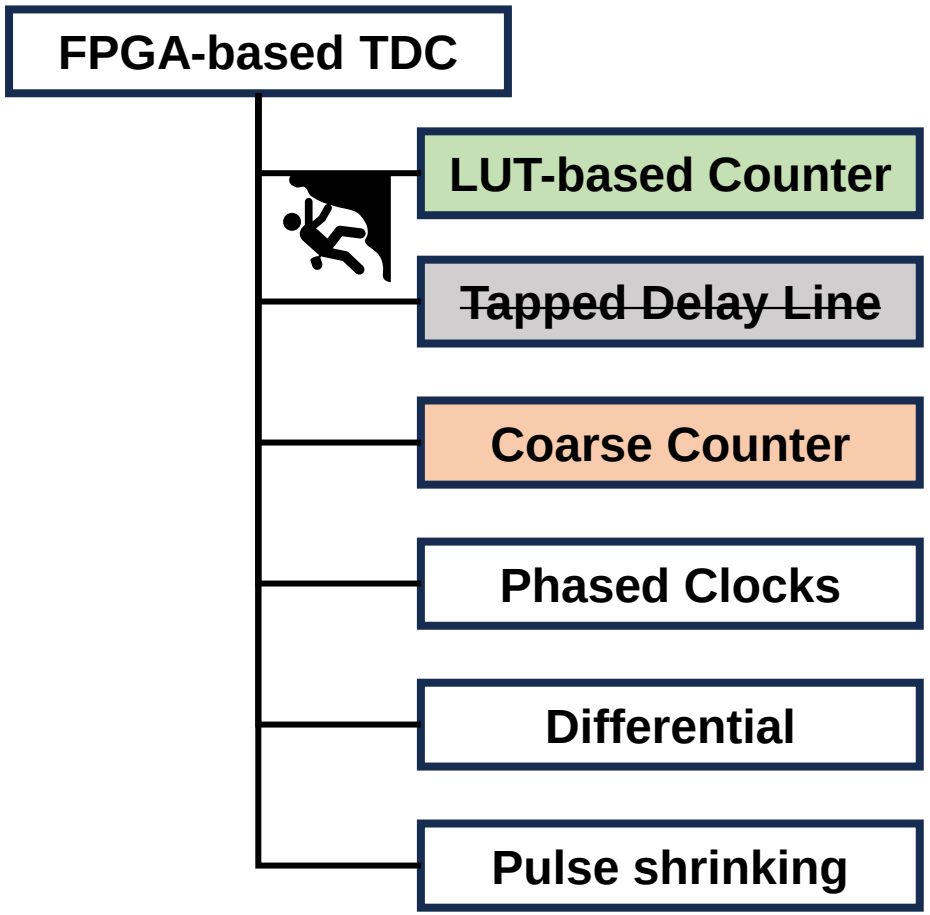


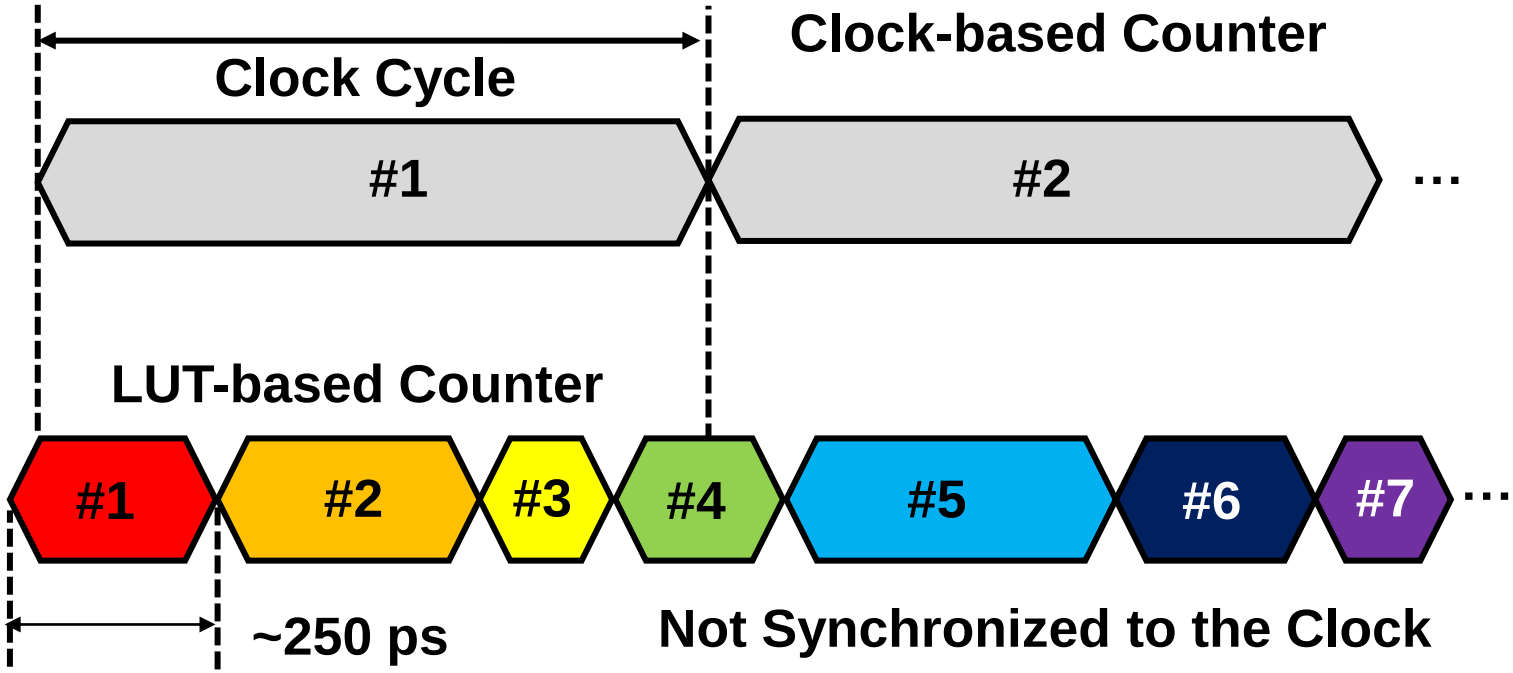
Ideal FWHM: **198 ps**
Measured FWHM: **205 ps**



2. Proposed LUT-based TDC

Proposed **LUT-based** TDC





Low resource is required for LUT-based counter
But the average bin size is ~250 ps

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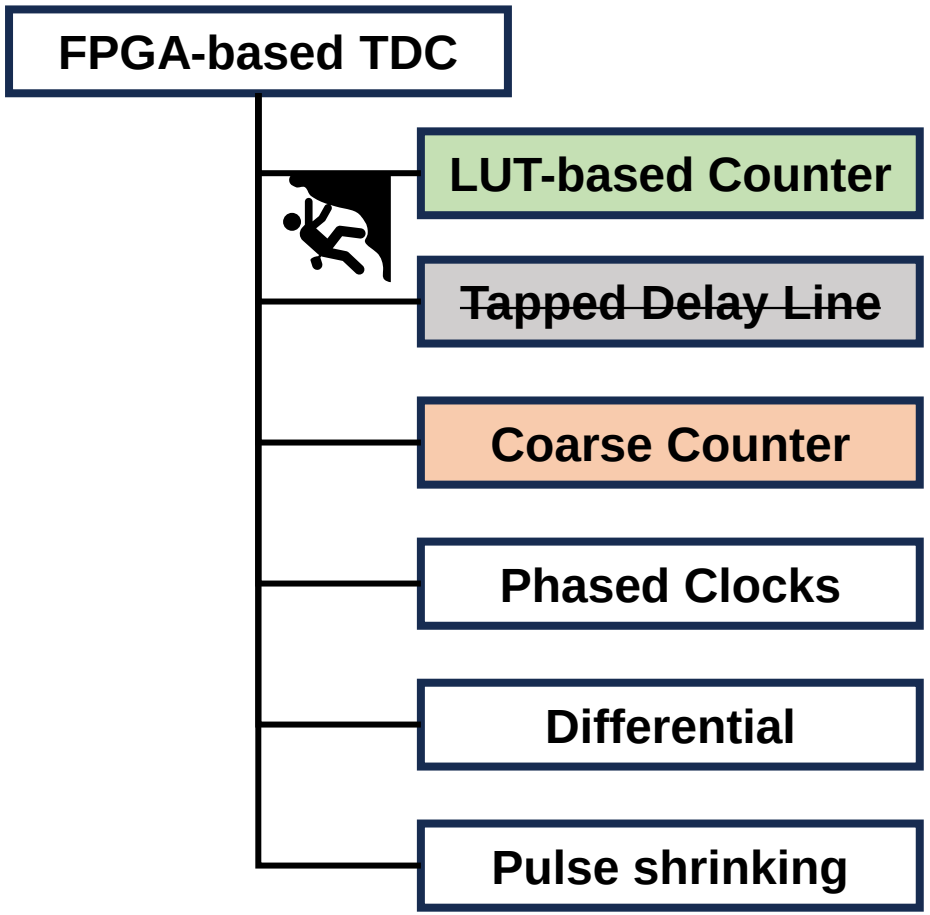
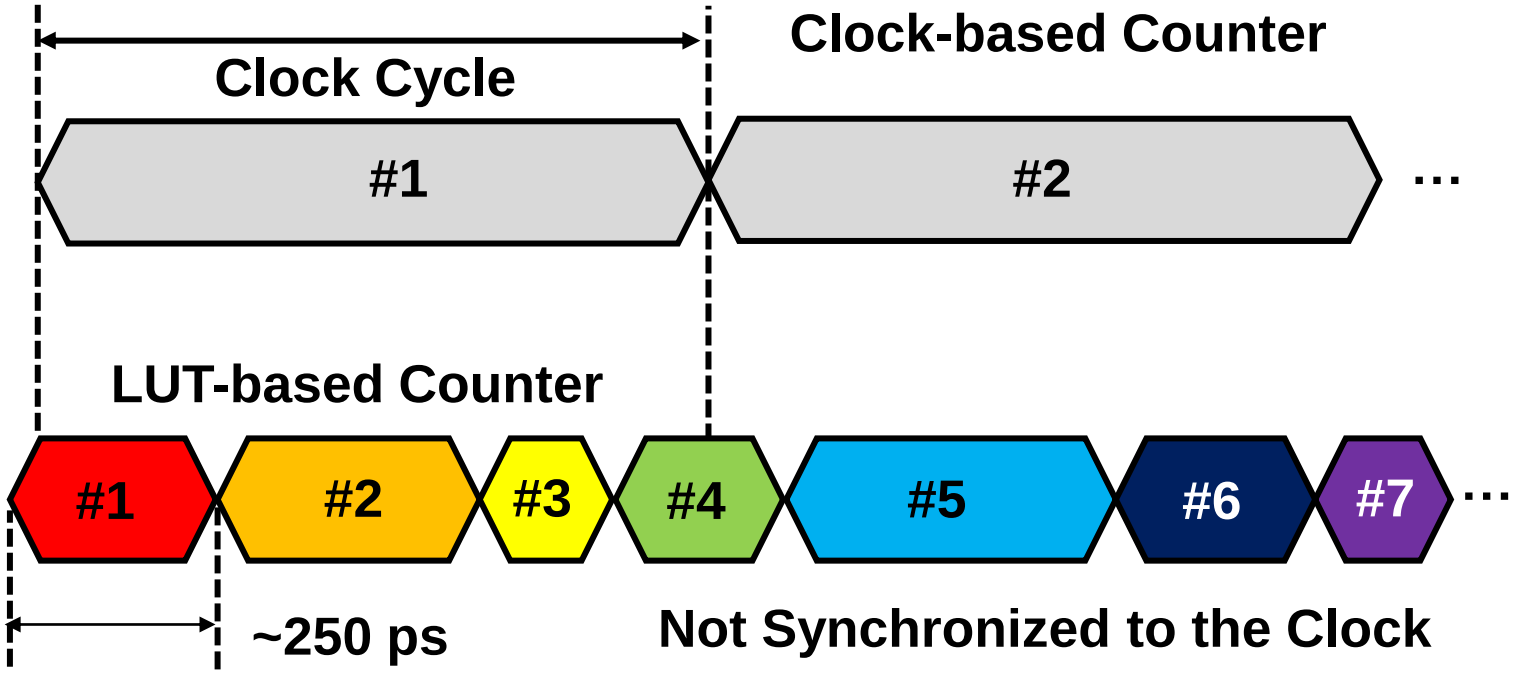
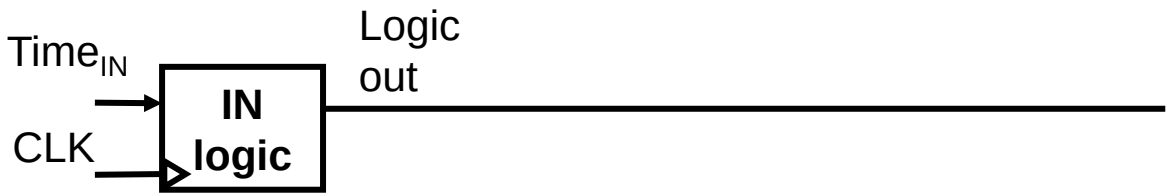


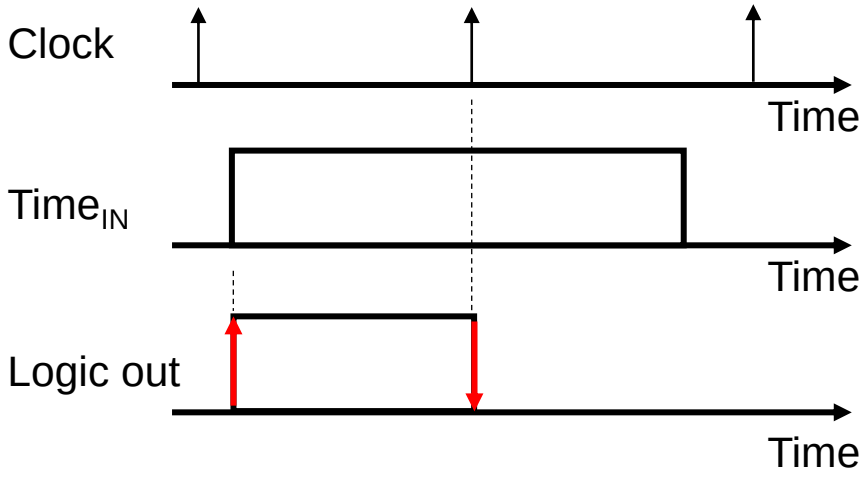


Low resource is required for LUT-based counter
But the average bin size is ~250 ps ➔ 10 ps

2. Proposed LUT-based TDC

Schematic of the proposed **LUT-based** TDC





The input logic generates a pulse when the TimeIN is enqueued and terminates the pulse at the next clock edge.

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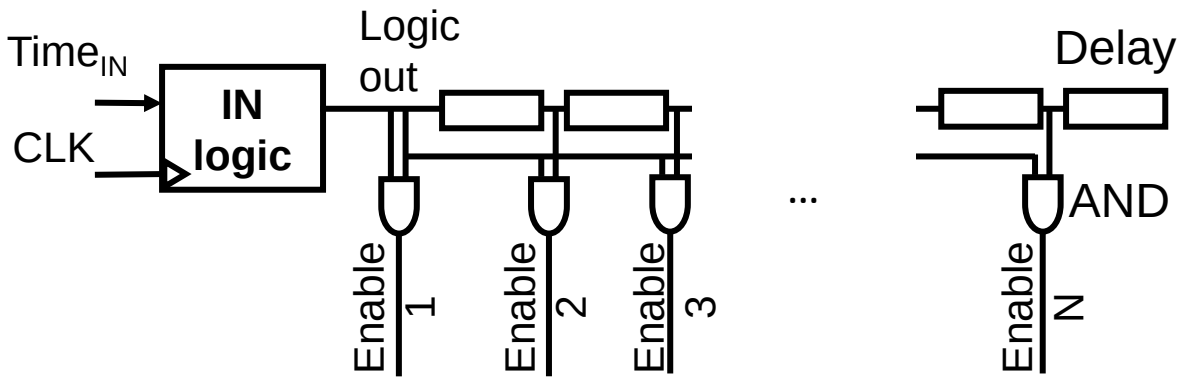
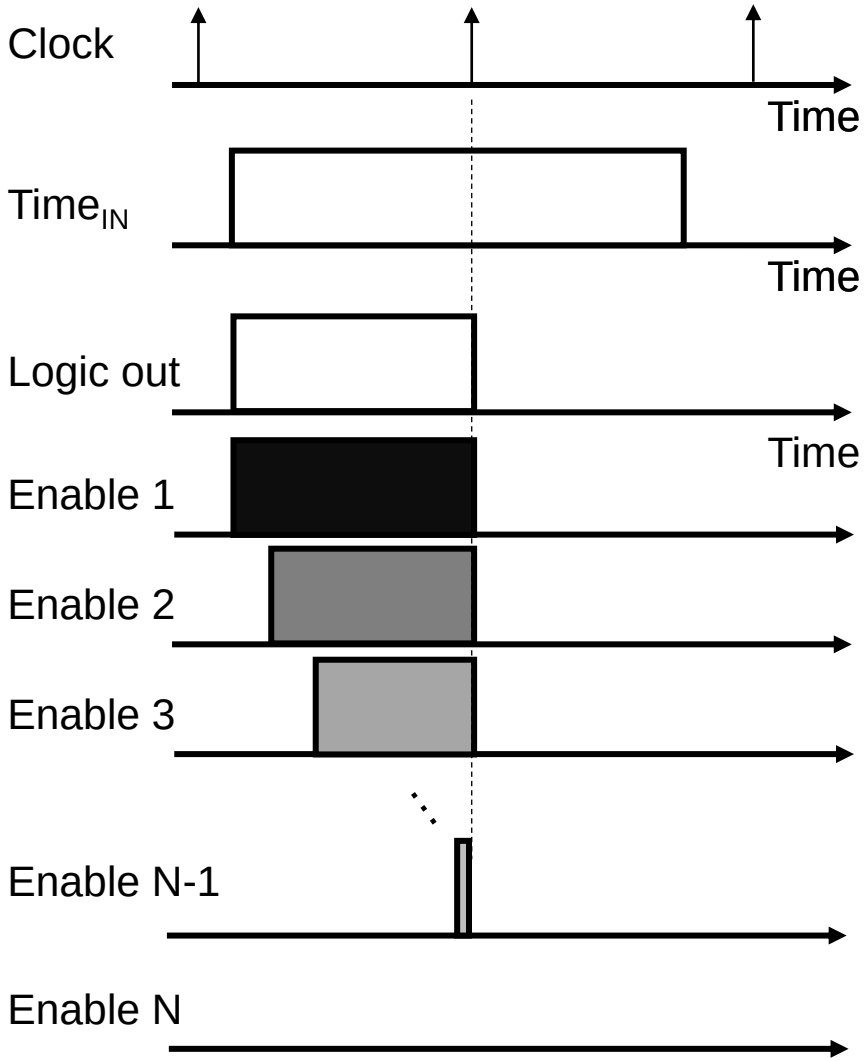


Enable signals are gradually shorten from Enable 1 to Enable N.



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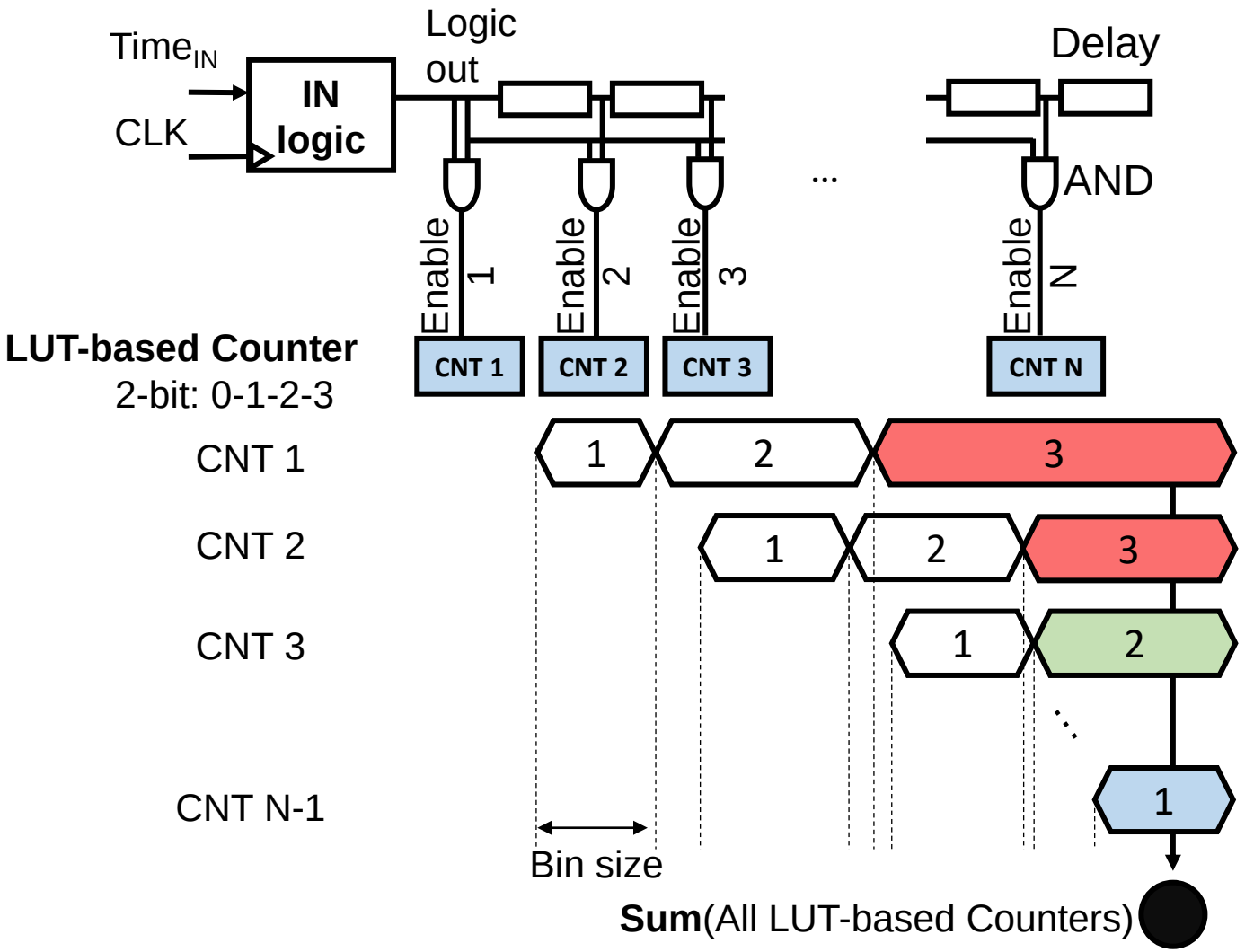

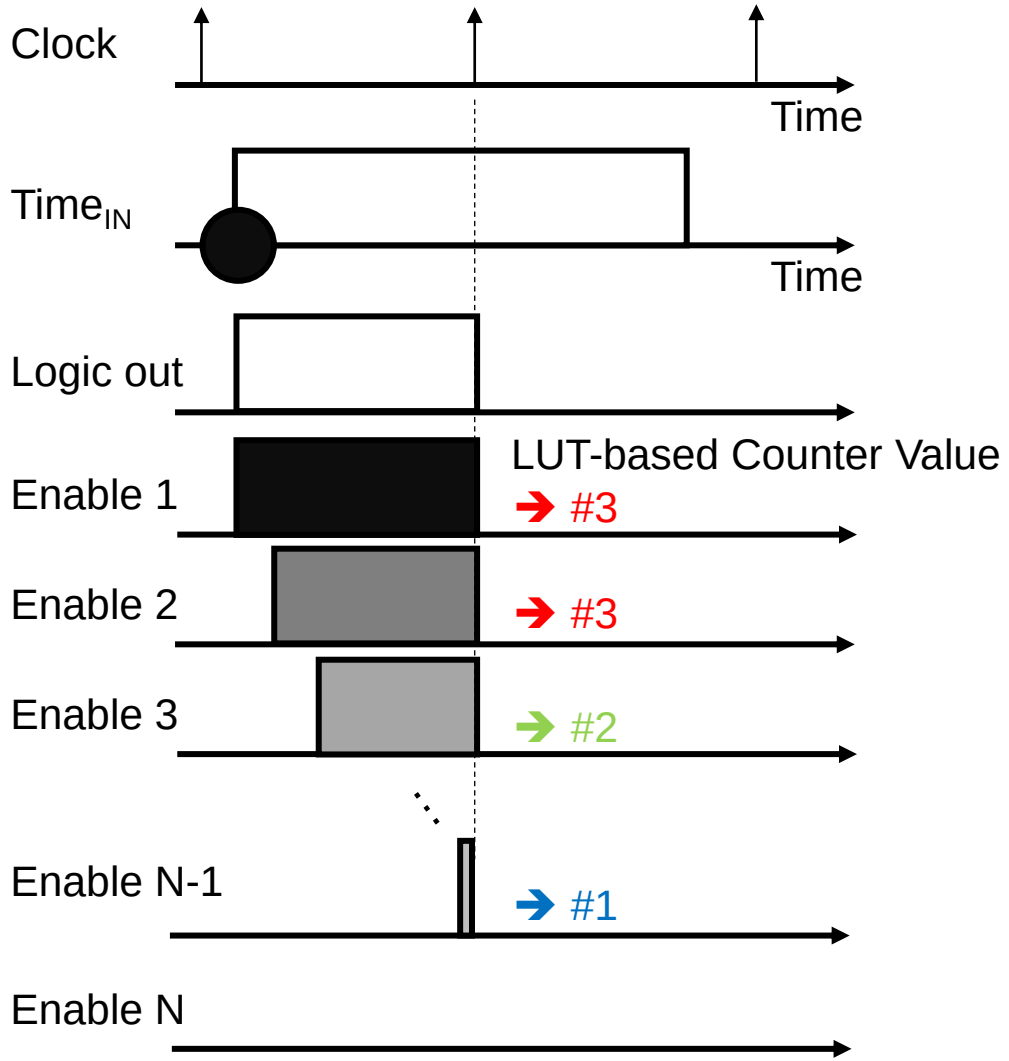

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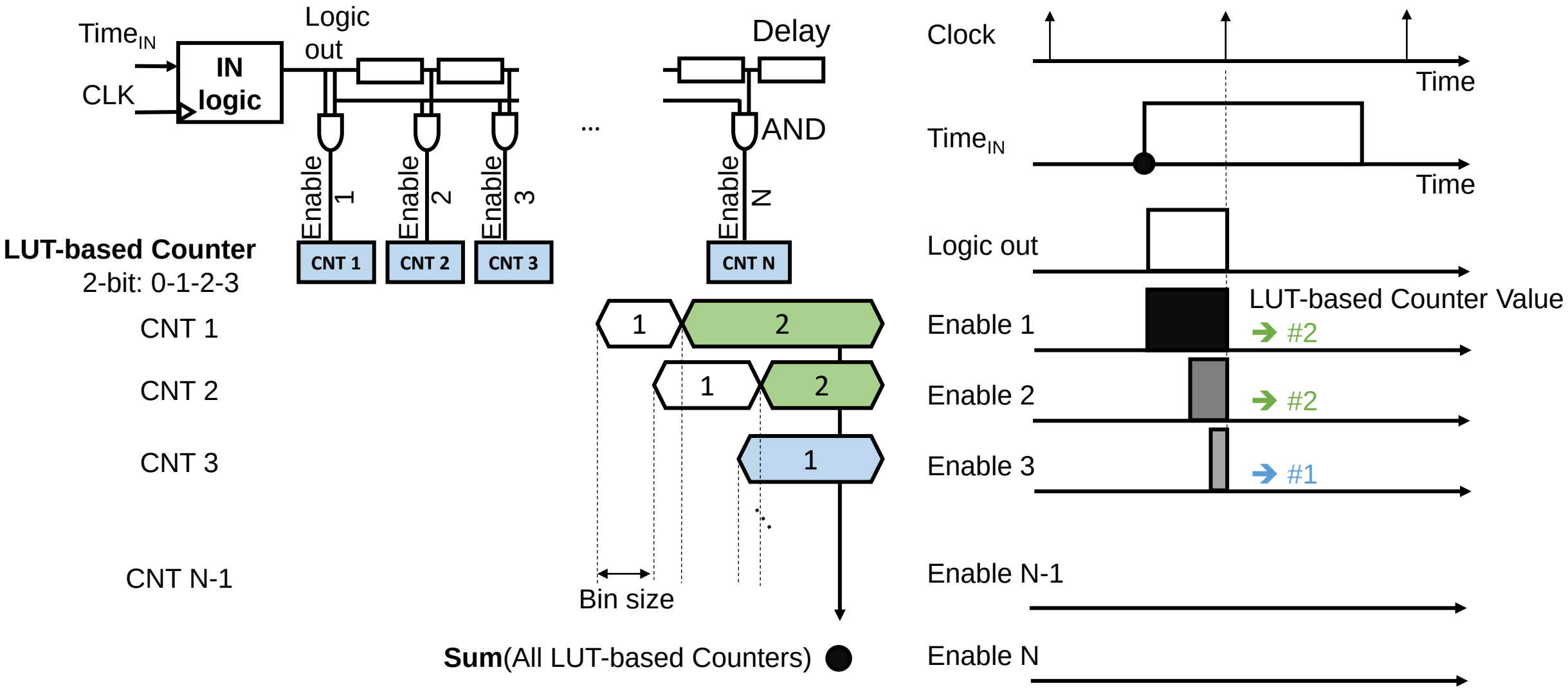

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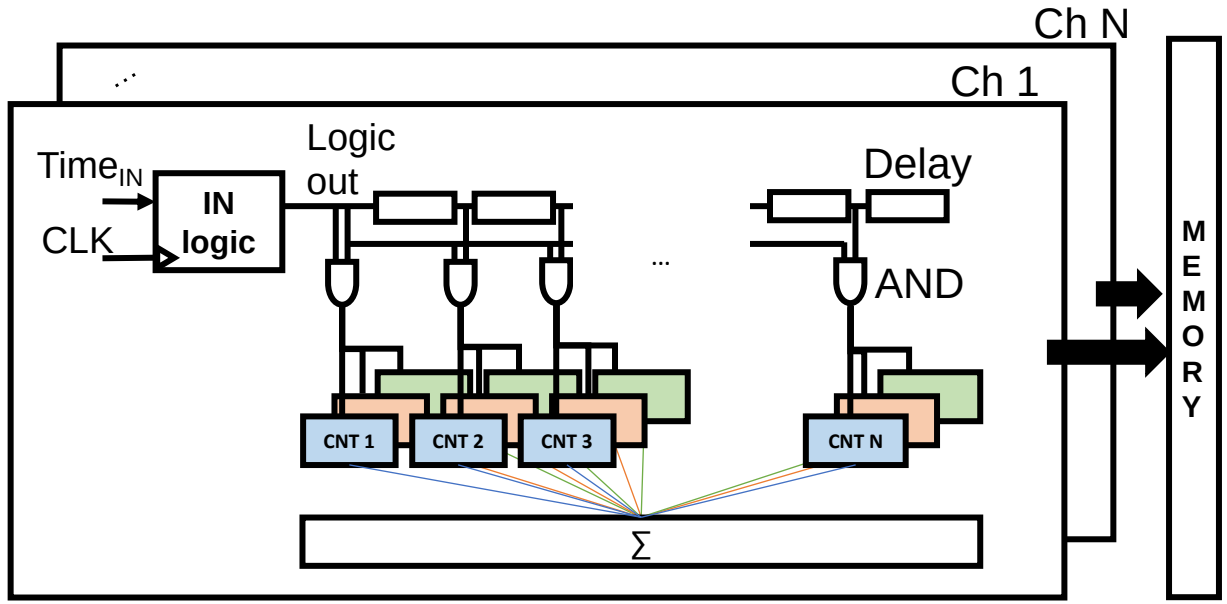
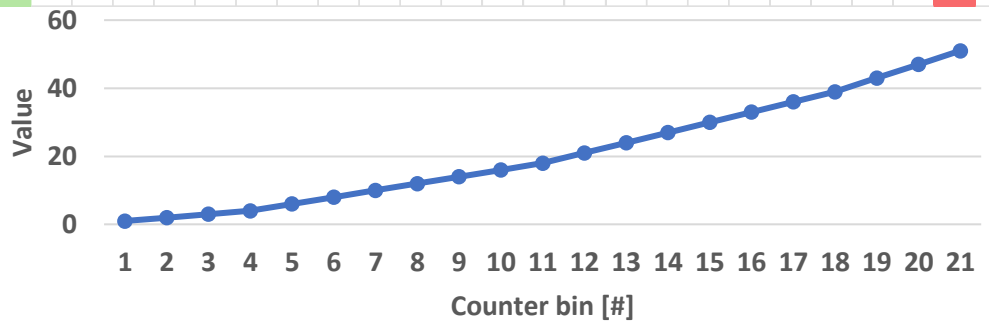
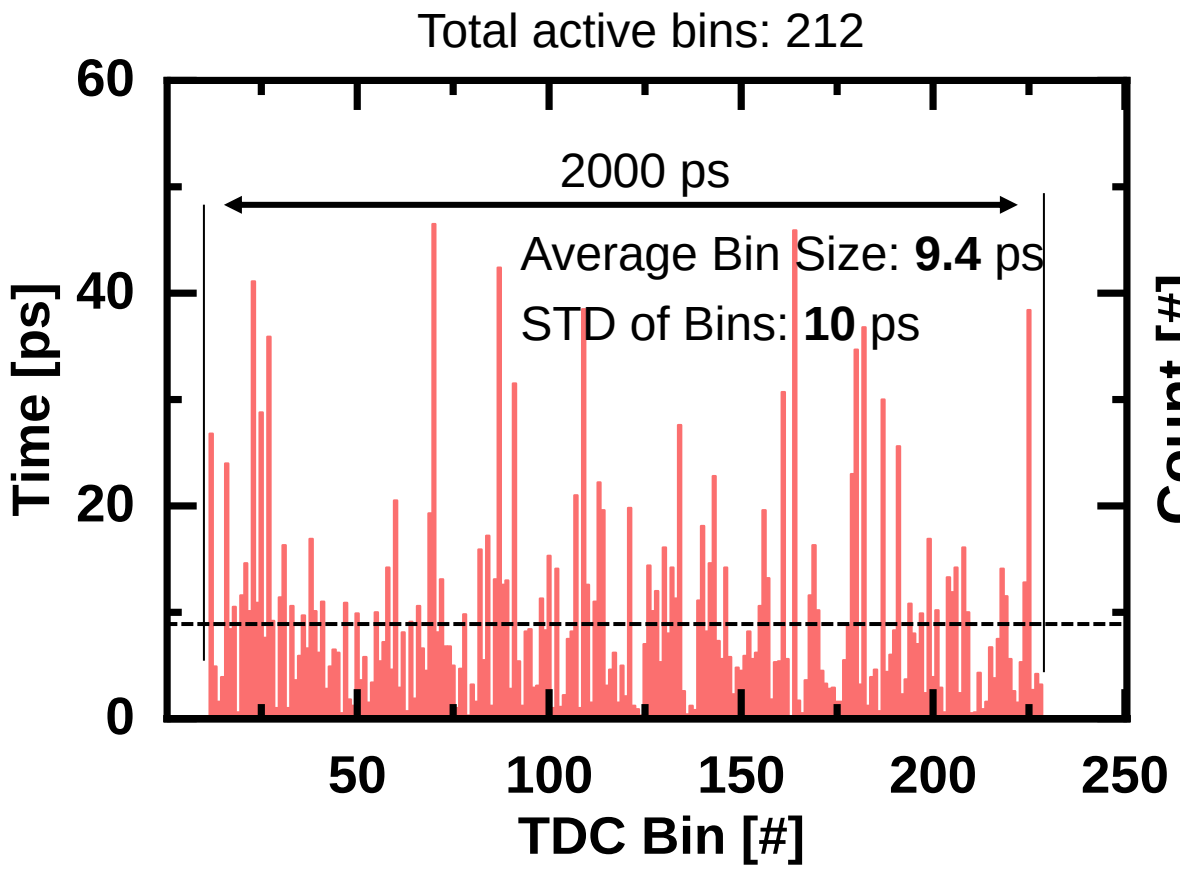


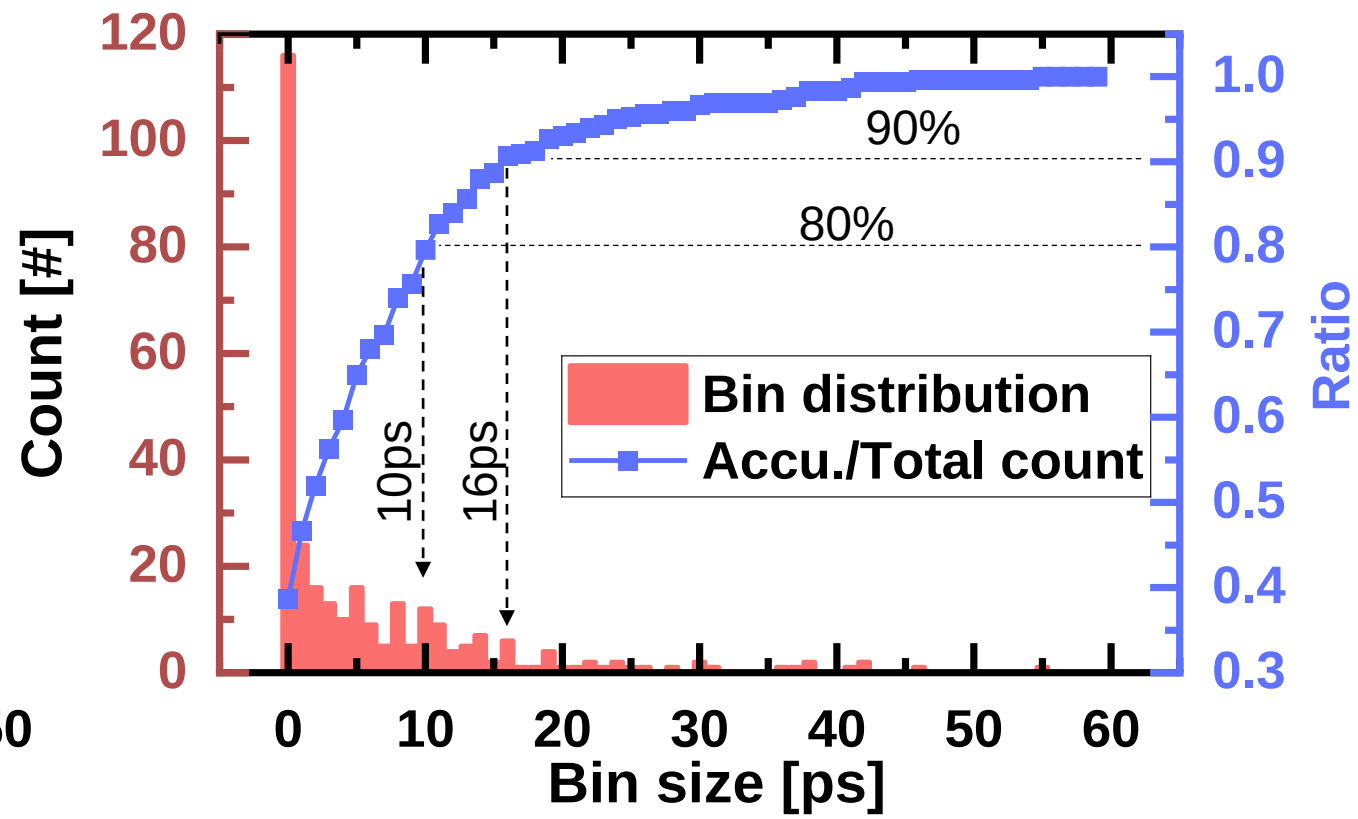
Counter name	Counter values
LUT-based counter 1	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3 3 3 4 4 4
LUT-based counter 2	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3 3 3 4 4
LUT-based counter 3	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3 3 3 4
LUT-based counter 4	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3 3 3
LUT-based counter 5	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3 3
LUT-based counter 6	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3 3
LUT-based counter 7	1 1 1 1 2 2 2 2 2 2 2 3 3 3 3
LUT-based counter 8	1 1 1 1 2 2 2 2 2 2 2 3 3 3
LUT-based counter 9	1 1 1 1 2 2 2 2 2 2 2 3 3
LUT-based counter 10	1 1 1 1 2 2 2 2 2 2 2 3
LUT-based counter 11	1 1 1 1 2 2 2 2 2 2 2
LUT-based counter 12	1 1 1 1 2 2 2 2 2 2
LUT-based counter 13	1 1 1 1 2 2 2 2 2
LUT-based counter 14	1 1 1 1 2 2 2 2
LUT-based counter 15	1 1 1 1 2 2 2
LUT-based counter 16	1 1 1 1 2 2
LUT-based counter 17	1 1 1 1 2
LUT-based counter 18	1 1 1 1
LUT-based counter 19	1 1 1
LUT-based counter 20	1 1
LUT-based counter 21	1



3. Experiment Results

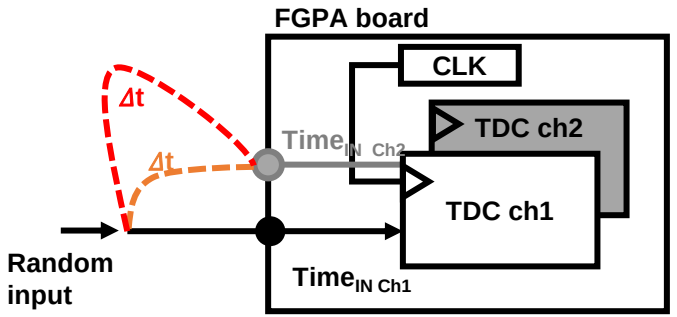
Single channel test

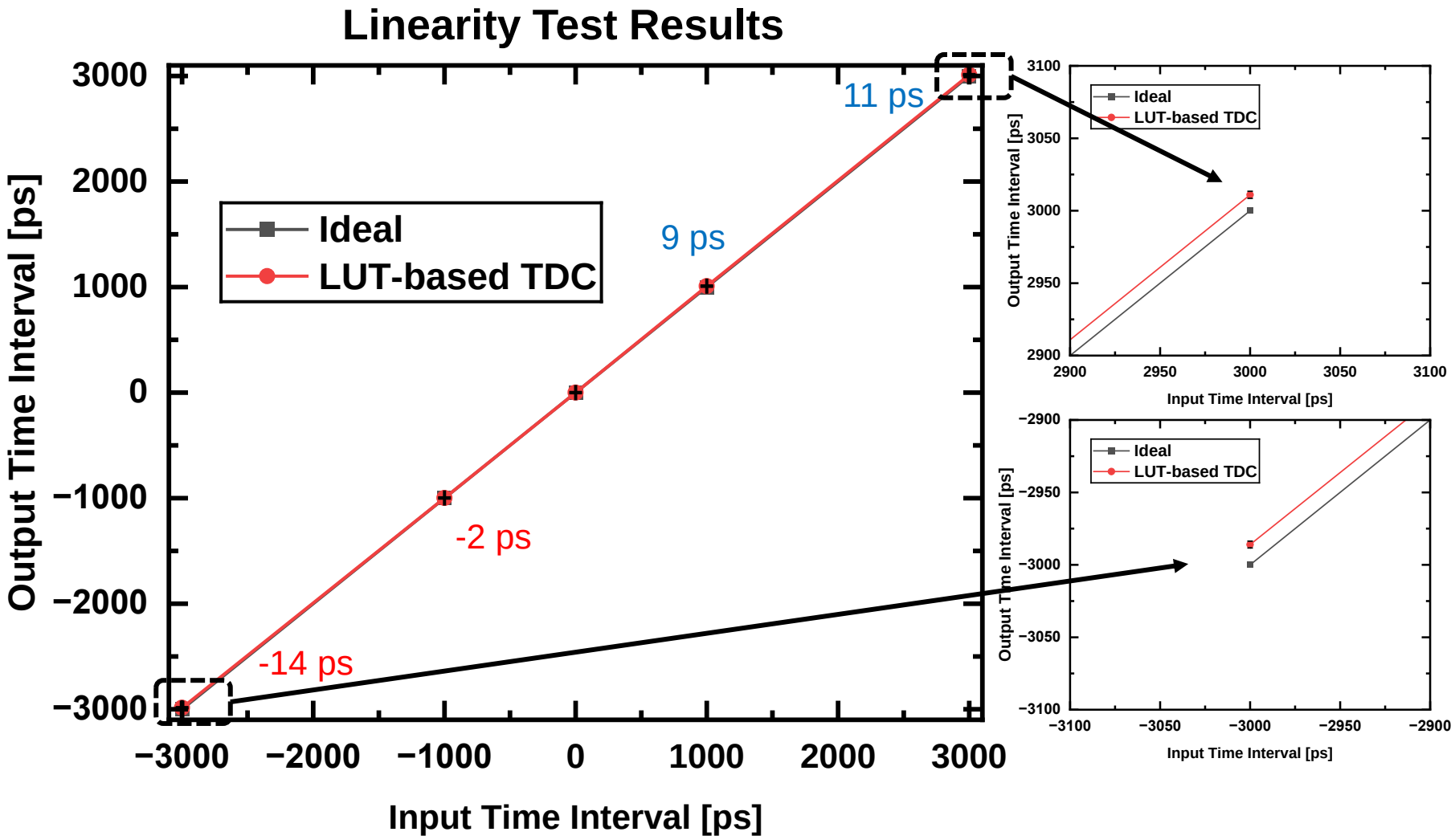




3. Experiment Results

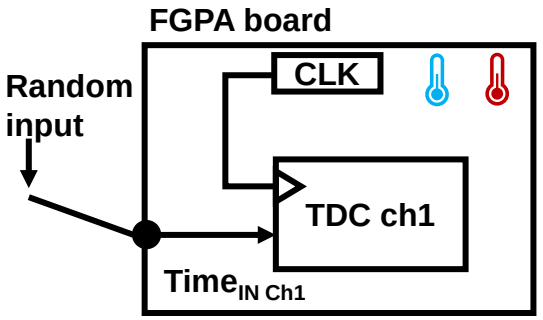
Multi-channel Test



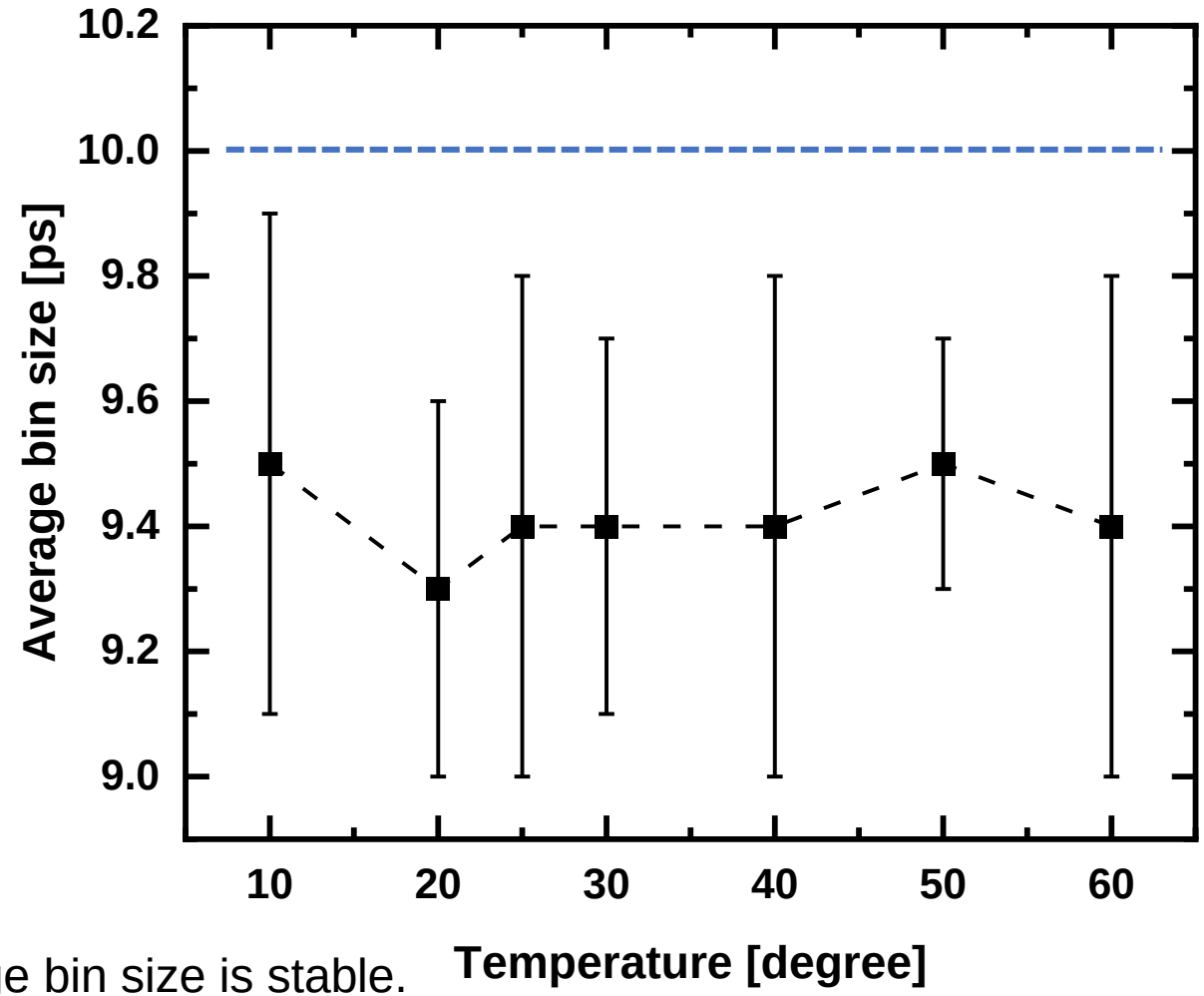


3. Experiment Results

Temperature Test



Average bin sizes depending on temperature changes

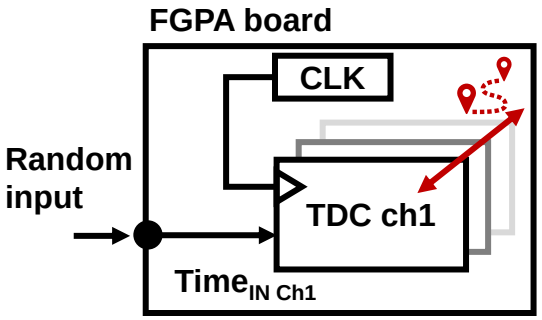


Average bin size is stable.

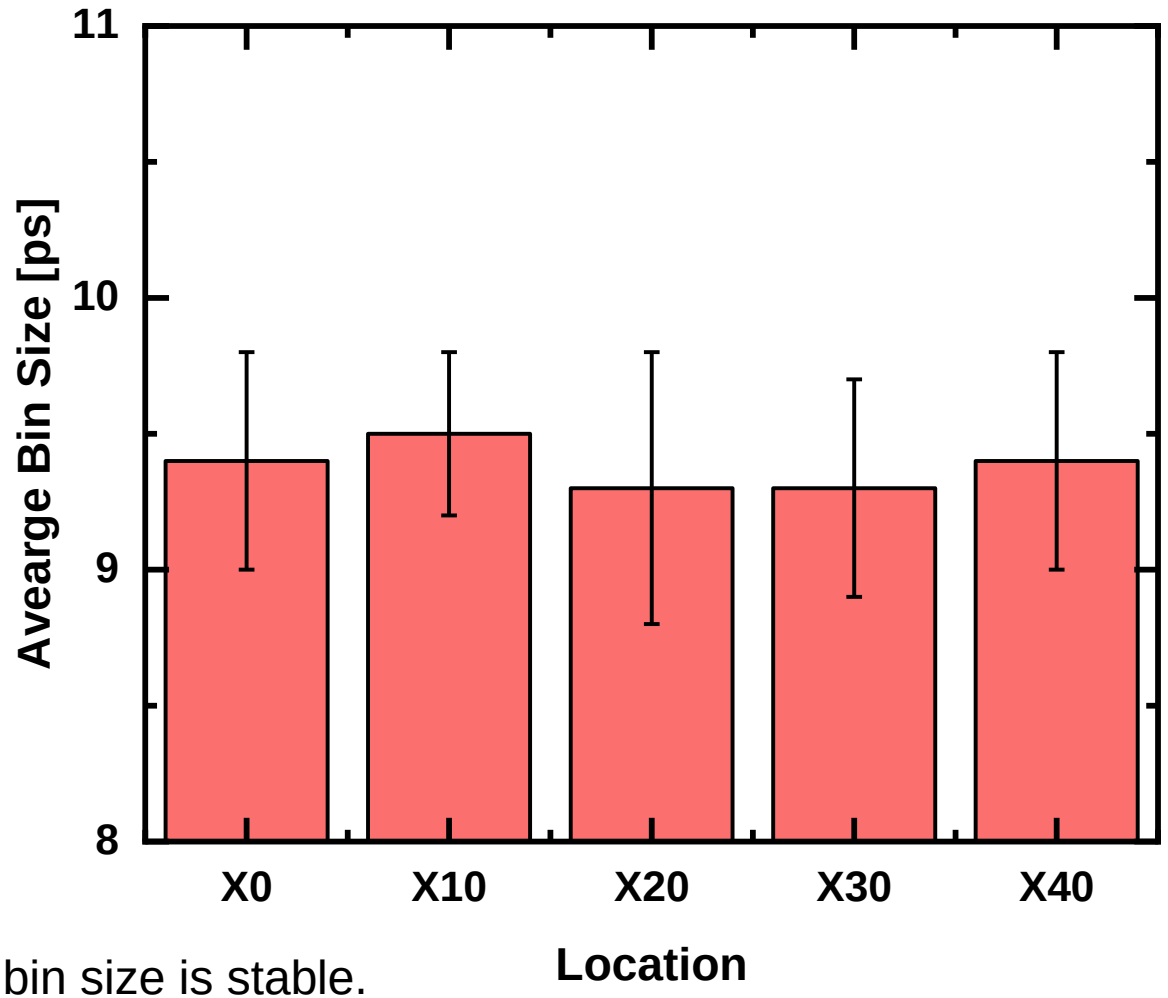
➔ No temperature correction circuit, which requires a huge resource, is needed.

3. Experiment Results

Location Test



Average bin sizes depending on location changes



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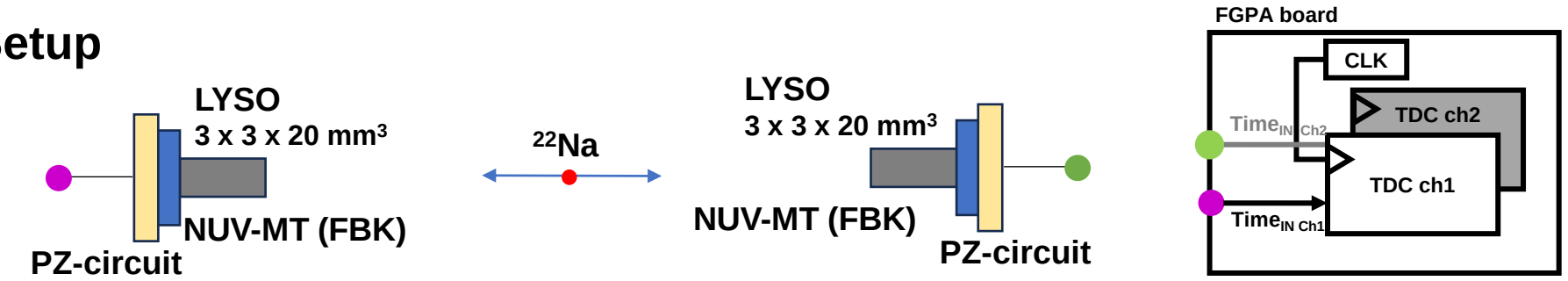
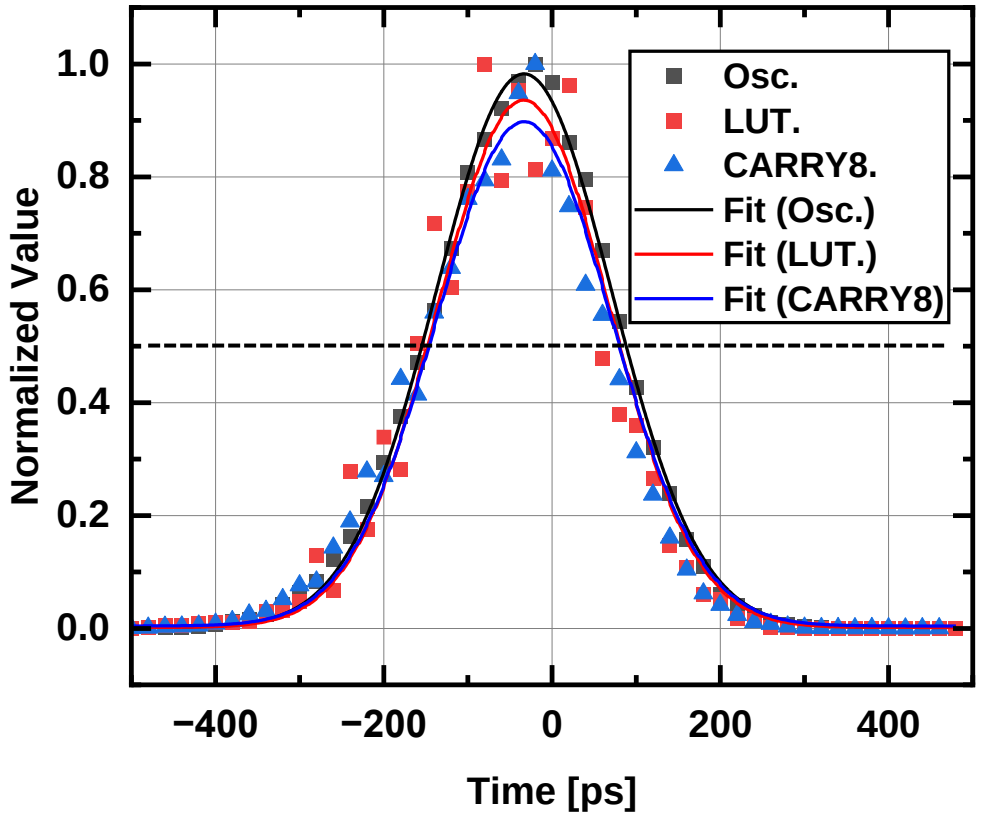
3. Experiment Results

Experimental Setup





Calculated FWHM

	Ave. / STD	
Osc. (sampling 40ps, interpolation)		**245 ps**
LUT-based TDC	**(10ps/10ps)**	**240 ps**
CARRY8-based TDC	**(5ps/5ps)**	**241 ps**

4. Conclusion

- **Resource use comparison**

Utilization		CARRY8-based TDC	LUT-based TDC	Differences
	CARRY8	102	2	-100 (▼**98%**)
	CLB LUTs	837	404	-432(▼**52%**)
	CLB Registers	1110	807	-303(▼**27%**)

- **Power consumption comparison**

Power consumption	CARRY8-based TDC	LUT-based TDC	Differences
Ch	0.109 W	0.006W	-0.103W(▼**94%**)

Reduced resource usage and lower power consumption enable the implementation of more TDC channels within a limited area.

4. Conclusion

- **LUT-based Time-to-Digital Converter**
  is successfully implemented with dramatically reduced resources

  Average bin size 9.4 ps ← Sub-10 ps Bin Size

  is internally free from location and temperature variation

  The clock-asynchronized LUT-based TDC operates in a random sequence, minimizing the impact of temperature and location variations on performance. As a result, there is no need to implement correction circuits, which would otherwise require a significantly large amount of resources.

- **Next step**

  The LUT-based TDC still exhibits large bins (>40ps).
  ➔ It will be investigated to make bin size more even

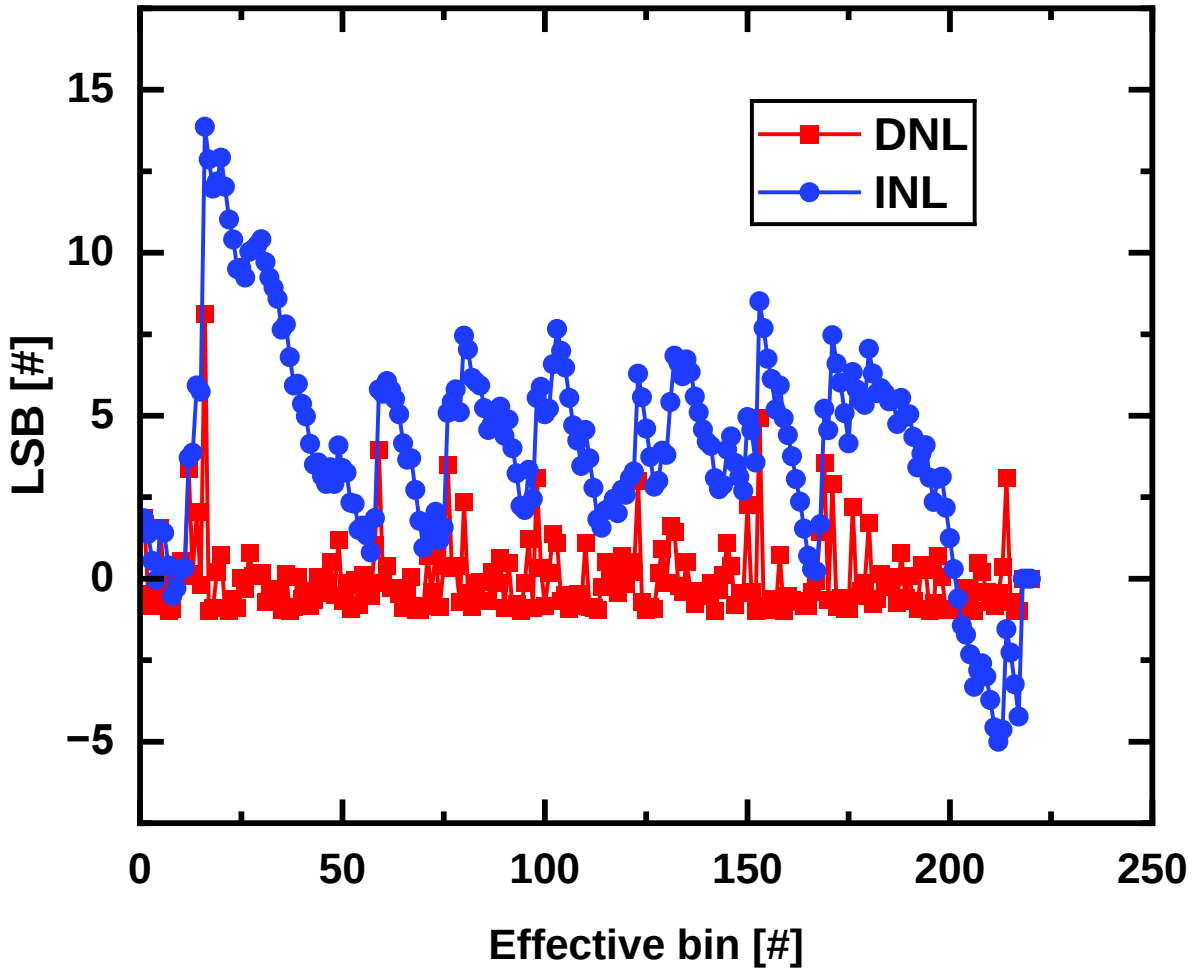
Q & A

Thank you for your attention.

3. Experiment Results

Single channel test

Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)



3. Experiment Results